

Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

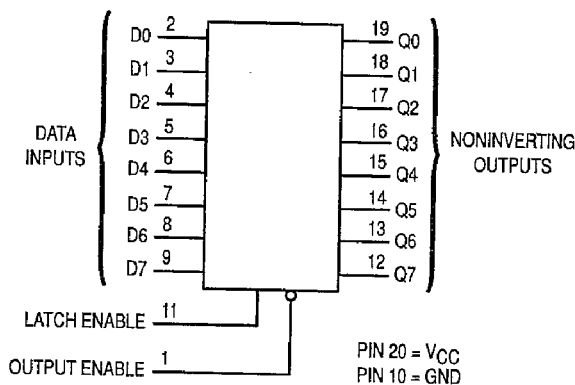
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HCT573A is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
 - Improved Propagation Delays
 - 50% Lower Quiescent Power

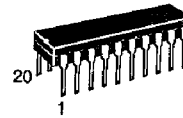
LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	58.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	0.0075	pJ

* Equivalent to a two-input NAND gate.

MC74HCT573A



N SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
SOIC PACKAGE
CASE 751D-04

ORDERING INFORMATION

MC74HCTXXXAN Plastic
MC74HCTXXXADW SOIC

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	VCC
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

3



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package‡	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 † Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C
 For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

3

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.7	V
			5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	4.5	0.1	0.1	0.1	μA
			5.5	0.1	0.1	0.1	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	4.5	± 0.1	± 1.0	± 1.0	μA
			5.5	± 0.5	± 5.0	± 10	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} ≤ 0 μA	4.5	4.0	40	160	μA
			5.5	4.0	40	160	
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ - 55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5)	30	38	45	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	30	38	45	ns
T_{PLZ} , T_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TZL} , t_{TZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

CPD	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		48		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

TIMING REQUIREMENTS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			-55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	10		13		15		ns
t_h	Minimum Hold Time, Latch Enable to Input D	4	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2	15		19		22		ns
t_r , t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

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SWITCHING WAVEFORMS

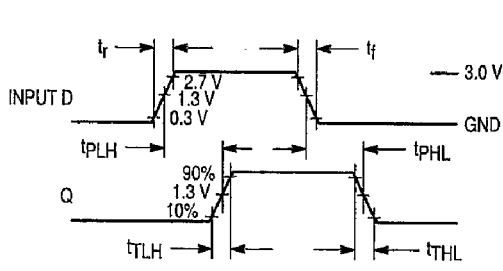


Figure 1.

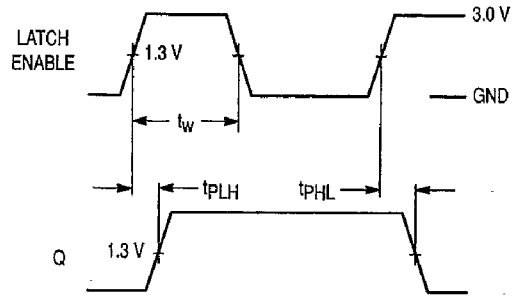


Figure 2.

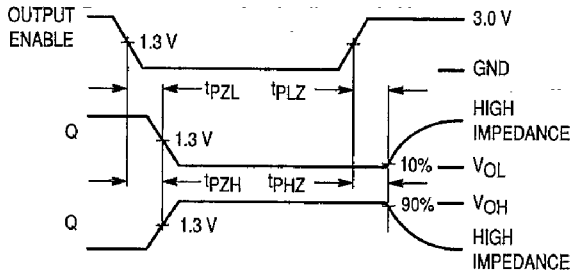


Figure 3.

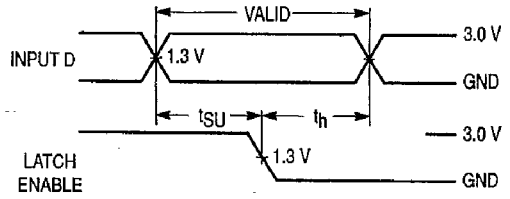
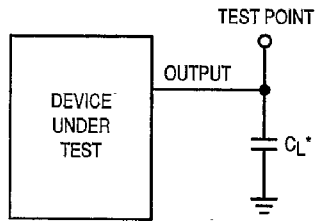


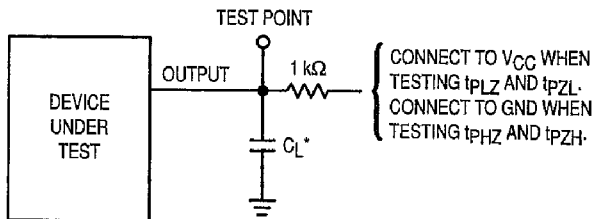
Figure 4.

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* Includes all probe and jig capacitance

Figure 5. Test Circuit



* Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM

