SAR10 Series
Angular Rate Sensor

The SAR10 and SAR10H contains a ButterflyGyro™ MEMS die and a BiCMOS mixed mode ASIC, housed in a custom SOIC package that can be efficiently handled by automated production lines. The sensor is factory calibrated and compensated for temperature effects to provide high-accuracy digital output over a broad temperature range. SAR10 has ± 250 °/s range and SAR10H has ± 100 °/s range.

Tuning of the excitation and detection frequency as well as perfect mechanical and electrical balancing the dual masses result in very low sensitivity to shock and vibrations.

By utilizing a unique sealed cavity technology, the vibrating masses are contained within the low-pressure hermetic environment needed for creating low dynamic damping and high Q factors, without any degradation over the lifetime of the device whatever tough environmental conditions.

A SPI interface enables an easy and effective communication between the application and the SAR10 or SAR10H. The angular rate data output is a 10-bit 2's complement format at a maximum rate of 2000 samples per second. A number of functions are available through the digital SPI interface including advanced self diagnostics.

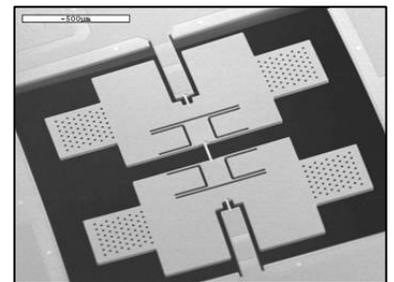**SAR10**
SAR10H

Table of Contents
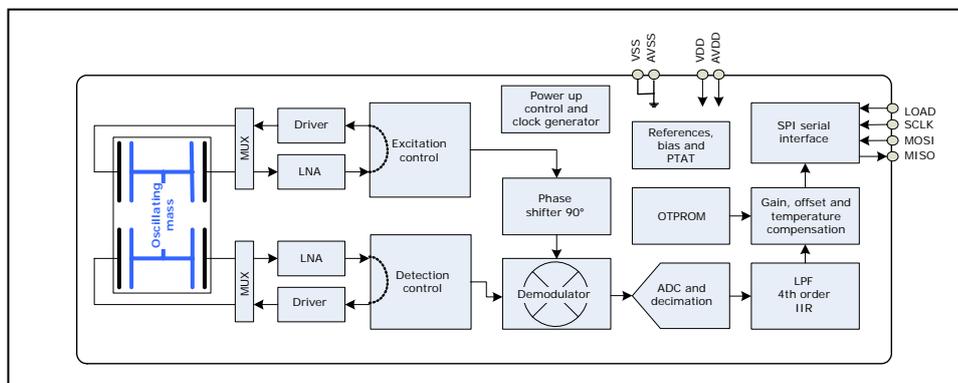
1 Product Description

1.1 Features

- High reliability and robustness over long lifetime
- Low vibration sensitivity
- High overload and shock capability (5000 g)
- Sensitive axis parallel to mounting plane
- Butterfly balanced design for high mechanical common mode rejection
- Closed-loop force feedback operation with electrostatic frequency tuning
- Ideal mono crystalline Si material
- Wafer level sealing with controlled Q-factor

- Low power
- Single supply +5 VDC
- Fully digital with SPI communication and on chip OTP calibration
- Digitally controlled sample rate up to 2000 SPS
- Bandwidth defined by built in 4th order digital LP filter
- Intrinsic continuous diagnostic monitoring
- No external components required

1.2 Overview

The SAR10(H) consists of a ButterflyGyro™ MEMS die and a BiCMOS ASIC housed in a miniature SOIC plastic package. The sensitive axis is parallel to the mounting plane. The function is based on the excitation of a reference motion in the butterfly structure. An angular rotation of the device will generate Coriolis forces, whose frequency equals that of the reference motion and whose resulting vibration amplitude is a measure for the angular rotation. By utilizing Sensonor's unique patented sealed cavity technology, the vibrating masses are contained within the low-pressure hermetic environment needed for creating low dynamic damping and high Q factors, without any degradation over the lifetime of the device. The gyro die is built as a triple stack consisting of a bottom glass die with metalized patterns defining excitation and detection electrodes, a middle micro machined mono crystalline silicon die with the oscillating masses, which also represent a common opposite electrode, and a third top cap glass die. A time

Figure 1.2 SAR10 Element structure

multiplexed, switched interface is used between the gyro die and the ASIC. This makes it possible to improve the symmetry by using the same electrodes for drive interface and sense interface. By the symmetric mechanical design and by connecting the electrodes cross-wise symmetric, the "butterfly" masses are operating in a balanced anti-phase movement. The balanced operation of both the excitation mode and the detection mode makes SAR10(H) almost insensitive to environmental vibrations, limiting effects causing bias drift as well as improving the Q-factors. A fine-tuning of the oscillation frequencies to allow for force-feedback operation is done during final test for each sensor by applying and programming an electrostatic bias to reduce mechanical stiffness and thereby

Figure 1.1 SAR10 Block diagram

calibrate detection mode frequency. Fixed algorithms use individually determined calibration coefficients stored in OTPROM poly fuse cells. Readings from the internal temperature sensor are used for accurate angular rate definitions. An SPI interface enables communication between application and SAR10(H). The angular rate data output is a 12-bit 2's complement format. A number of functions are available through the digital SPI interface.

2 Abbreviations and Definitions

2.1 Abbreviations

FSI	Full Scale Input
FSO	Full Scale Output
SPI	Serial Peripheral Interface
ASIC	Application Specific Integrated Circuit
ESD	Electro Static Discharge
MSB	Most Significant Bit
LSB	Least Significant Bit
OTPROM	One-Time Programmable Read Only Memory

2.2 Definitions

- o Specifications herein are over the complete temperature and supply voltage operating range unless otherwise is noted
- o Voltages are referenced to AVSS/VSS unless otherwise is specified

3 Recommended Operating Conditions

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Input range SAR10	ΩFSI			±250		°/s
SAR10H	ΩFSI			±100		°/s
Dynamic overload, angular rate	ΩOVL	1,5	±1200	±5000		°/s
Dynamic overload, shock		1,4,5	±500	±1500		g
Recovery time dynamic overload		1,5		30		ms
Supply voltage	VDD, AVDD	2	4.45	5.0	5.5	VDC
Current consumption		3			17	mA
Sensor oscillation frequency	fOSC			9.4		kHz
Internal master clock	fMCLK			8.0		MHz
Operating temperature	TOPER		-40		+90	°C

Note 1: The PRCEN command will have to be issued to revert to normal functionality.
Note 2: Both digital (V_{DD}) and analog (AV_{DD}) supply voltage.
Note 3: Total current consumption from both analog and digital supply.
Note 4: Shock below 500g/1ms will never result in an error condition.
Note 5: By design.

4 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may affect the performance and/or reliability of the device.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Supply voltage	VDD, AVDD		-0.5		7.0	VDC
Input voltage, any pin			-0.5		VDD +0.5	VDC
Input transient current, any pin					±100	mA
Short circuit immunity to VDD/AVDD or VSS/AVSS, any output					10	min
ESD voltage immunity, Human Body Model, any pin		1			2000	V
ESD voltage immunity, Charge Device Model, any pin		2			500	V
Mechanical shock		3			5000	g
Ambient temperature when operating			-40		+125	°C
Storage temperature			-55		+125	°C

Note 1: According to AEC-Q100-002 Rev. C or JESD22-A114 Rev. F
Note 2: According to AEC-Q100-011 Rev. B or JESD22-C101 Rev. D
Note 3: According to MIL-STD 883E.

5 SPI Serial Data Interface

Serial data communication with the application is through the SPI interface. The 8 MSBs of an angular rate data sample are mapped to the 8 bit response of the RARH (read angular rate high byte) command. The 2 LSBs of the sample are mapped to the 2 LSBs of the 8 bit response of the RARL (read angular rate low byte) command. The RARH command latches the 2 LSBs of a sample such that a RARH, RARL command sequence guarantees bits from the same angular rate sample. The 6 MSBs of the response from the RARL command is always a '010101' SPI error check bit pattern.

5.1 Signal Definitions and Characteristics

The SPI interface consists of the 4 signals MOSI, MISO, SCLK and LOAD.

Name	Signal Description
MOSI	**Master Out, Slave In.** After a negative edge on LOAD, 8-bit command is shifted in on MOSI, clocked by SCLK (MSB first).
MISO	**Master In, Slave Out.** Output from previous command is stored in a Data Register. At a negative edge on LOAD, the content of the Data Register is loaded to the Data Output Register. While command byte is shifted into the Command Register, Data Output is shifted out on MISO (MSB first).
LOAD	**Chip Select/Transfer Start Strobe.** As long as LOAD=1, the MISO output is in a high-Z mode (tri-stated). A negative edge on LOAD initiates an SPI transfer. The new command is executed after a positive edge on LOAD. If a positive edge occurs on LOAD before at least 8 bits are shifted in on MOSI, the command will be ignored.
SCLK	**Serial Data Clock.** MOSI is read on the positive edge of SCLK, and MISO is shifted out on the negative edge of SCLK.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
High ('1') level	VH	2	0.7VDD			V
Low ('0') level	VL	2			0.3VDD	V
Input rise time	trI	2			1/(20fSCLK)	s
Input fall time	tfI	2			1/(20fSCLK)	s
Output fall time	tPHL	1,2			8.5	ns
Output rise time	tPLH	1,2			8.6	ns
Output enable delay	tPHZ tPLZ tPZH tPZL	1,2			1.2 0.97 8.4 8.2	ns
Data rate	fSCLK	3			8.5	Mbits/s
Capacitive load, MISO	CMISO	2			100	pF

Note 1: With load of 100pF connected to V_{SS}.
Note 2: Characteristic is based on proven library I/O cell performance.
Note 3: By design.

5.2   SPI Commands

Name	Command	Address	Output	Description	Note
Read Commands					
RARH	10000000	-	dddd dddd	Read Angular Rate, High Byte	2
RARL	10001111	-	0101 01dd	Read Angular Rate, Low Byte	
RTMP	10110000	-	1000 0000	Read internal temperature	
RSR	10110100	-	Status byte	Read status register	
SafeGuard Commands					
SGDIS1	01001110	11010111	1000 0000	SafeGuard Disable Command 1	1
SGDIS2	01100011	01010000	1000 0000	SafeGuard Disable Command 2	
SGDIS3	00010010	10101000	1000 0000	SafeGuard Disable Command 3	
SGEN	01010101	-	1000 0000	SafeGuard Enable Command	
Error Handling Commands					
PRCEN	10101010	-	1000 0000	Re-enable signal processing after error condition	3

Note 1: The three SafeGuard disable commands MUST be issued in the -1,-2,-3 sequence, and with the addresses shown. Any in-between commands or incorrect addresses will reset the Safeguard Disable sequence. A single SGEN command re-enables the SafeGuard.

Note 2: The RARH command latches high and low bytes such that a sequence of RARH first followed by RARL guarantees bits from the same Angular Rate sample.

Note 3: In case of a recoverable error condition, issuing this command re-enables continued angular rate readout. Note that for this command to function the SafeGuard must be disabled. See chapter 8 for details.
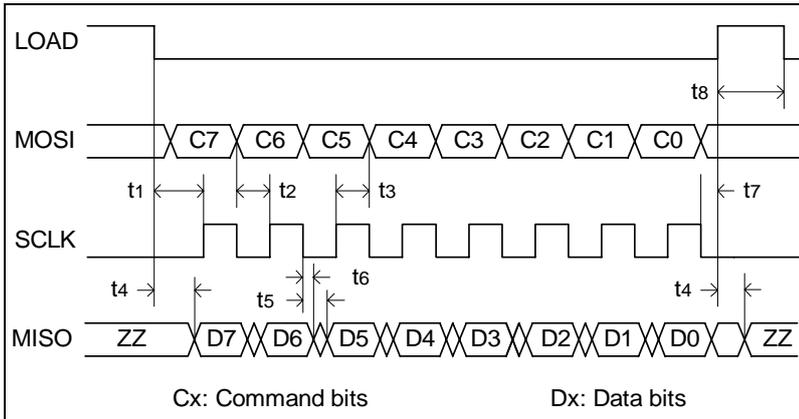
Figure 5.1 SPI interface signal timing diagram

For commands that need an address, the address byte is shifted in prior to the command byte.
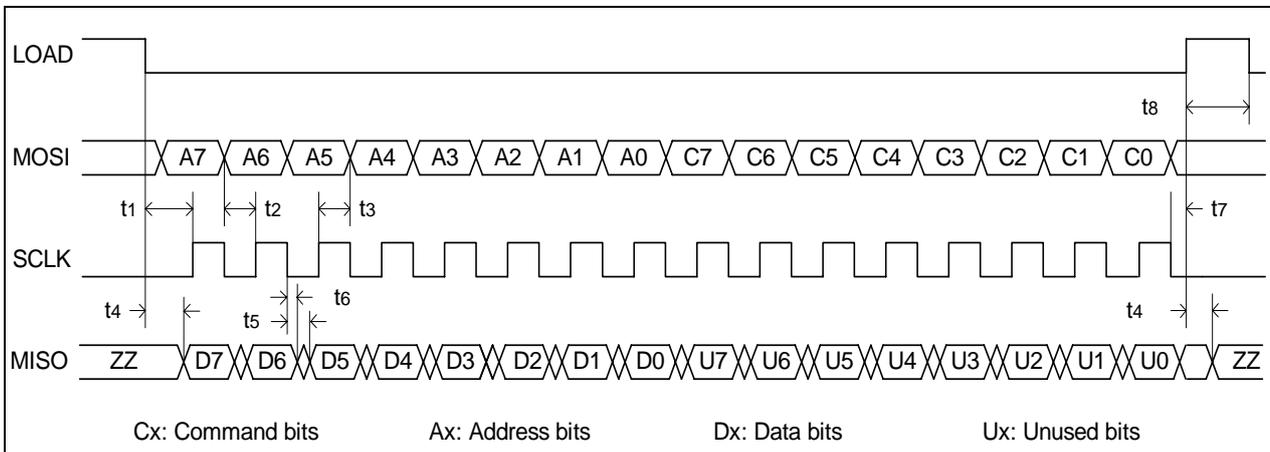
Figure 5.2 SPI interface signal timing diagram for command with address byte

Symbol	Parameter	Specification			Note
		Min	Max	Units	
t1	Delay from falling edge of LOAD to the first rising edge of SCLK	10		ns	2
t2	Delay from stable data at MOSI to rising edge of SCLK (MOSI data setup time)	10		ns	2
t3	Delay from rising edge of SCLK to new data at MOSI (MOSI data hold time)	10		ns	2
t4	Delay from falling edge or rising edge of LOAD to active or high-Z state of MISO		20	ns	2
t5	Delay from falling edge of SCLK to stable new data at MISO (MISO data output delay)		20	ns	2
t6	Delay from falling edge of SCLK to removal of old data at MISO (MISO data hold time)	0		ns	2
t7	Delay from last falling edge of SCLK to next rising edge of LOAD	20		ns	2
t8	Delay from rising edge of LOAD to falling edge of LOAD	527		ns	1,2

Note 1: Minimum 4 internal MCLK cycles = 4 * 1/7.6MHz.

Note 2: By design.

5.3 Error Code

The Error Code is a bit pattern defined as $1000\ 0000_2$. This Error Code is the SPI response during device startup, if an illegal or undefined SPI command is attempted executed, or if a RARH or RARLX command was executed while at the same time any one or more of the Status Register flags is a '0'. The RARH command accesses the 8 MSBs of the 12 bit 2's complement rate data. Negative angular rate data is limited (clamped) to -2032 (binary $1000\ 0001\ 0000_2$) since the 8 MSBs of rate data in the range -2048 to -2033 ($1000\ 0000\ 0000_2$ to $1000\ 0000\ 1111_2$) could otherwise be confused with the Error Code. For symmetry reasons positive angular rate data is likewise limited to 2032. Note that this angular rate data limiting does not affect any Status Register flags.

6 Angular Rate and Temperature Output

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Angular rate data format						
Word length				10		bit
Format				2's complement		
SPI command(s)				RARH RARL		
Scale factor SAR10				1.0		(°/s)/LSB
SAR10H				0.4		(°/s)/LSB
Full scale signal	$+\Omega$FSO $-\Omega$FSO	1	High byte 00111110 11000001	Low byte 01010110 01010110	(+250 °/s) (−250 °/s)	
Zero rate output			High byte 00000000	Low byte 01010100	(0 °/s)	
Error Code			High byte 10000000	Low byte 10000000		
Accuracy						
Sensitivity shift over temperature		1		±6		%
Non-linearity				±0.3		%FSO
Noise referred to input		2		1.5		°/s (rms)
Zero-rate accuracy SAR10				1.6	±	%FSO
SAR10H				±4.0		%FSO
Zero-rate drift over 100s		8		±1		°/s
Vibration sensitivity referred to input		6		±0.3		(°/s)/g
Cross-axis sensitivity referred to input		7		±0.04		(°/s)/ (°/s)
Frequency response		5				
Sampling rate	fS			2		kHz
Pass band ripple		4,9			0.2	dB
Group delay		9			13	ms
Lower passband cut-off frequency	fL	3,9		0.01		Hz
Roll-off for f < fL		9		20		dB/dec
Upper passband cut-off frequency	fH	3,9		50		Hz
Roll-off for f > fH		9		100		dB/dec
Attenuation for f > 310 Hz		9	60			dB

Note 1: Measured at f_Ω =2Hz
Note 2: Integrated over f_L to f_H
Note 3: -3dB frequency
Note 4: 1Hz < f < 39Hz
Note 5:

HP-filter transfer function: $H(z) = \dfrac{1 - z^{-1}}{1 - p_0 z^{-1}}, p_0 = \dfrac{1 - \dfrac{f_L}{2f_S}}{1 + \dfrac{f_L}{2f_S}}$ (with nominal f_L and f_S values)

LP-filter transfer function: $H(z) = \dfrac{b_{01} + b_{11} \cdot z^{-1} + b_{21} \cdot z^{-2}}{1 - a_{11} \cdot z^{-1} - a_{21} \cdot z^{-2}} \cdot \dfrac{b_{02} + b_{12} \cdot z^{-1} + b_{22} \cdot z^{-2}}{1 - a_{12} \cdot z^{-1} - a_{22} \cdot z^{-2}}$

a_{11}	1.91064453125E+00	a_{12}	1.829833984375E+00
a_{21}	-9.31640625E-01	a_{22}	-8.40087890625E-01
b_{01}	1.0498046875E-02	b_{02}	7.8125E-03
b_{11}	-1.0498046875E-02	b_{12}	4.8828125E-03
b_{21}	1.0498046875E-02	b_{22}	7.8125E-03

Note 6: Frequencies < 5.4 [kHz]. Stationary vibrations above 5.4 [kHz] hitting resonant modes may cause larger effects. This effect is highly nonlinear.
Note 7: Includes effects caused by mechanical misalignment due to package tolerances. See [1].
Note 8: By design.
Note 9: Guaranteed by theoretical digital filter design and verification (characteristics depends only on master clock frequency.

7   Power Supply and Start-up

The SAR10(H) is designed for a single +5 volt supply. The device has four pins for power connection: V_{DD}, AV_{DD}, V_{SS} and AV_{SS}. The V_{SS} and AV_{SS} pins shall be connected together on the printed circuit board as close to the device as possible. The same rule applies to V_{DD} and AV_{DD}. A simultaneous power-on of the two supplies is essential to prevent internal latch-up conditions. An external power supply decoupling capacitor is needed. This decoupling capacitor should be a low ESR 100nF capacitor connected to the supply line as close to the V_{DD} and V_{SS} pins as possible. An additional decoupling capacitor is needed between pin 6 (REFV) and V_{SS}. This should be a low ESR 10nF capacitor connected as close as possible to pin 6 and V_{SS} pin. The SAR10(H) has a supply voltage surveillance circuit which sets the Status Register flag PRNG_OK to '1' only if AV_{DD} is within specified range. If outside this range, the PRNG_OK flag is set to '0'.
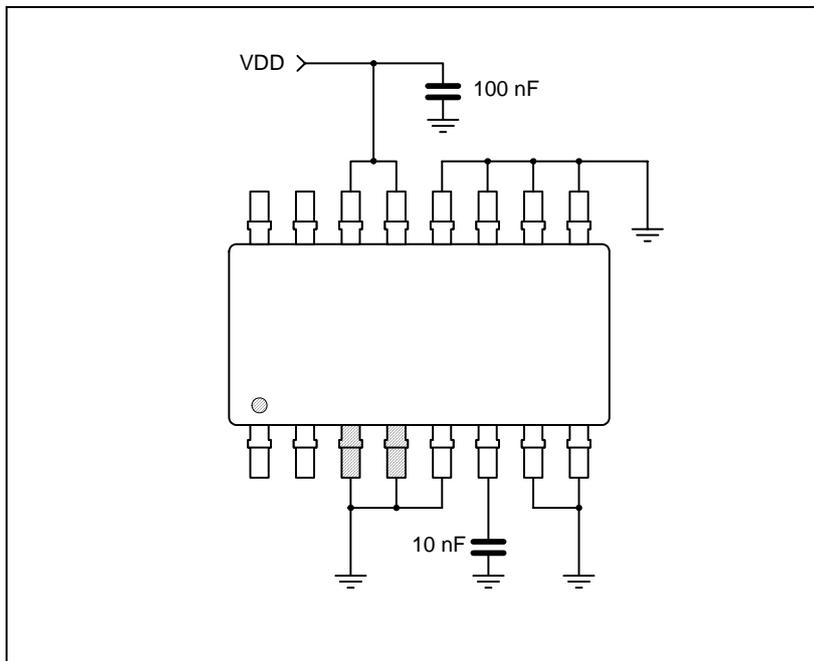

Figure 7.1 Power Supply and Decoupling (top view)

Characteristics	Symbol	Note	Specifications			
			Min	**Nom**	**Max**	**Units**
Supply voltage rise time to VDD-MIN	tD	1	0.001		10	ms
Start-up time	tINIT	2		90		ms
Time to rate data within full specifications	tSTABLE	2			500	ms
Minimum AVDD for internal RESET	VRU	3, 7			1.0	VDC
Detectable AVDD glitch	tG	7	10			ns
Reset threshold	VRESET	4	2.5		3.5	VDC
Status Register AVDD OK flag (PRNG_OK) threshold	VPRNGH	5	5.55		5.91	VDC
	VPRNGL		4.2		4.43	
Reset delay	tRSTN	6, 7	128		208	μs

Note 1: The voltage V_{DD-MIN} is the lower limit for V_{DD} and A_{VDD} as specified in 2.5.
Note 2: The startup time is defined as the time until the Status Register EXC_OK flag goes to '1' (sensor excitation has stabilized). Reading from the device during this time interval causes the device to respond with Error Code.
The time to stable data is defined as the time from the end of t_{INIT} until the angular rate data is within full specifications. Angular rate data can however be read from the device during this time interval.
Note 3: Internal reset signal is defined for supply voltage above V_{RU}.
Note 4: Internal reset is activated when the supply voltage passes V_{RESET}. The reset threshold has a small hysteresis (approx. 0.1V).
Note 5: The RARH and RARLX commands return the Error Code when $AV_{DD} \leq V_{PRNGL}$ or $AV_{DD} \geq V_{PRNGH}$.
Note 6: For correct OTP power-down a reset pulse width of minimum 50 μs is needed.
Note 7: By design.
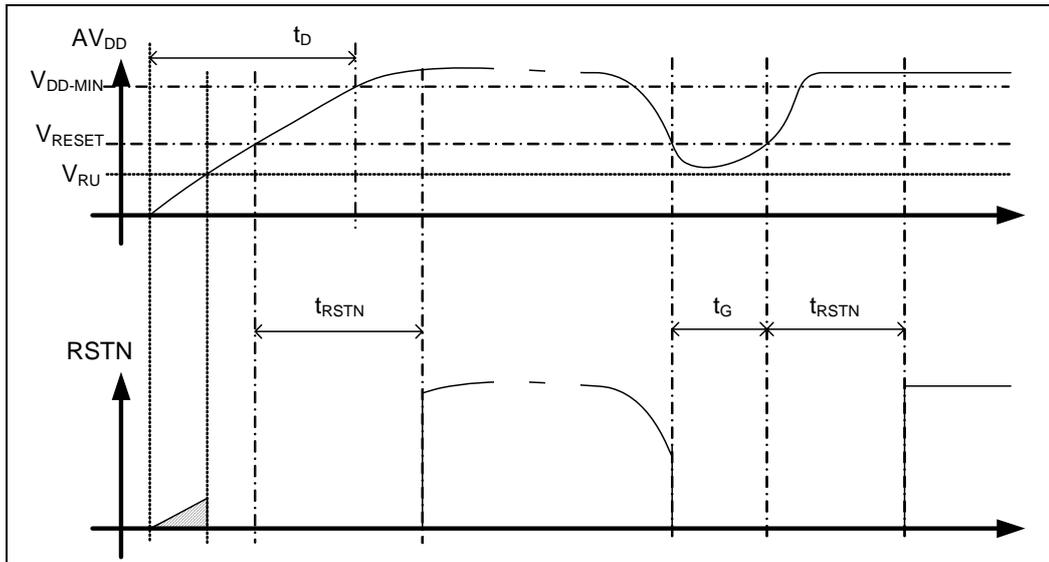
Figure 7.2 Power-Up and Power Glitch Reset Timing

8 Status Register and Internal Diagnostic Monitoring

Internally in the SAR10(H), 6 error monitoring functions are employed to make sure an irregular output angular rate is detected. If any of the monitoring functions detects an irregular condition the corresponding flag becomes a '0', otherwise a '1'. The Status Register flags are available to the application via the RSR SPI command. It is assumed that a flag can signal an "error" for any length of time. To make sure short error ('0') pulses are visible to the application, the '0' pulses are "stretched" in time to between 1.5 and 2.0 ms.

Bit Position	Flag Name	Monitoring function	Recoverable
7	ADC_OK	ADC_OK is '0' if an ADC overflow occurs, otherwise '1'.	Yes
6	SIG_OK	SIG_OK is '0' if an arithmetic overflow or underflow occurs in the digital signal processing, EXCEPT if the signal amplitude exceeds the output range in the final scaling (by the S0INV parameter), otherwise '1'.	No
5	OTPPAR_OK	OTPPAR_OK is '0' if OTP parity check fails, otherwise'1'.	No
4	ATEST_ INACTIVE	ATEST_INACTIVE is '0' if an analog test mode is active, otherwise '1'. This monitoring function will not result in any Error Code signaling.	-
3	PRNG_OK	PRNG_OK is '0' if the AVDD voltage is out of range, otherwise '1'.	No
2	DET_OK	DET_OK is '0' if a sensor die detection electrode connection is open or if a leakage current is present on one or both electrodes, otherwise '1'.	No
1	EXC_OK	EXC_OK is '0' if the excitation control loop fails to lock on resonance frequency such that the excitation amplitude falls below a critical level, otherwise '1'.	Yes
0	(no name)	Not used. Always '1'.	-

After power-up and until the device start-up is complete the output from the RARH and RARLX commands is substituted by the Error Code, see 5.3. After start-up, if any of the flags go to '0' (the internal monitoring functions indicate that the output is irregular), the Error Code is the output from the RARH and RARLX commands, and also internal digital signal processing is held. This signaling continues indefinitely until the device is powered down, or, in case of some of the conditions (see 'Recoverable' in the table above), until the PRCEN command is issued.

The PRCEN command execution must obey the following algorithm:
1. Wait until no recoverable error conditions are flagged (polling the Status Register).
2. Wait minimum 30 ms (recommended 100 ms).
3. Execute the SGDIS1, -2 and -3 commands.
4. Execute the PRCEN command.
5. Execute the SGEN command

Note that for the PRCEN command to take effect, the Safe Guard must first be disabled by means of the SGDIS1,-2 and -3 commands. To resume normal operation after recovery, the SafeGuard must be re-enabled by using the SGEN command. If, before the Safe Guard was disabled, a non-recoverable error condition existed, the SAR10(H) will return to responding with the Error Code to RARH, -LX commands as well as holding internal digital signal processing even after the SGEN command was issued (the error is non-recoverable). Also note that while the SafeGuard is disabled, no error condition will be latched.
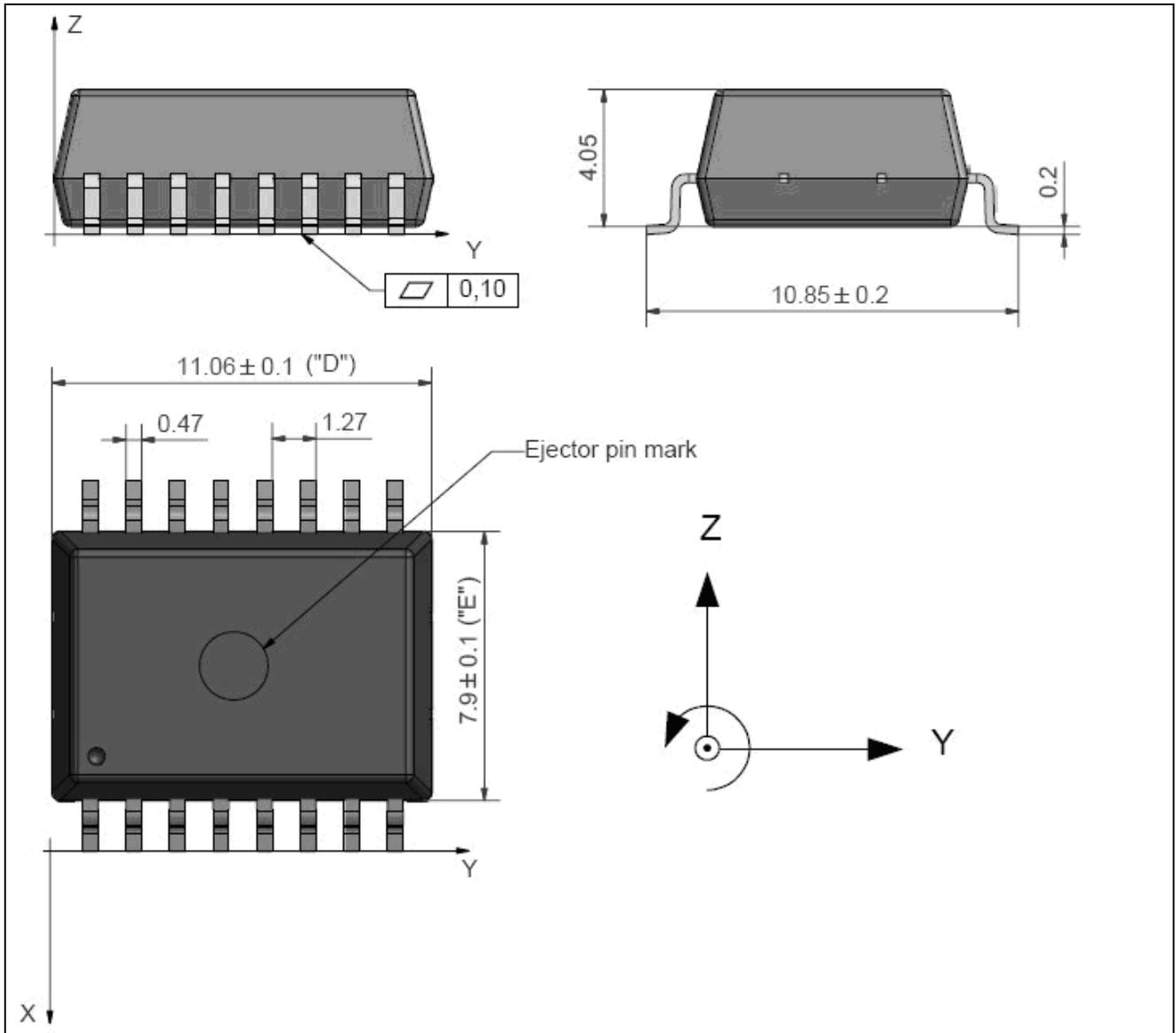
9 Mechanical Specifications

9.1 Physical dimensions

Figure 9.1 Package dimensions and sensitive direction of rotation. Top, side and bottom view.

Characteristics	Specifications
Package type	Plastic moulded SOIC
Number of pins	16
Weight	1.5 grams

9.2 Pin Configuration

Pin Number	Name	Type	Direction	Note	Function
1	SCLK	Digital	Input		SPI clock
2	LOAD	Digital	Input		SPI load
3	VSS	Power	-	1	Digital ground
4	AVSS	Power	-	1	Analog ground
5	-	-	-	2	Test pin. Connect to ground
6	REFV	-	-	3	Internal voltage reference
7	-	-	-	2	No internal connection. Connect to ground
8	-	-	-	2	Lead frame. Connect to ground
9	-	-	-	2	Lead frame. Connect to ground
10	-	-	-	2	No internal connection. Connect to ground
11	-	-	-	2	Test pin. Connect to ground
12	-	-	-	2	Test pin. Connect to ground
13	AVDD	Power	-	1, 4	Analog +5V supply voltage
14	VDD	Power	-	1, 4	Digital +5V supply voltage
15	MOSI	Digital	Input		SPI data input
16	MISO	Digital	Output	5	SPI data output

Note 1: To be connected externally.
Note 2: Connect to ground to minimize noise levels.
Note 3: Connect a 10nF low ESR decoupling capacitor between this pin and ground.
Note 4: Connect a 100nF low ESR decoupling capacitor between these pins and ground.
Note 5: This signal is tri-stated when LOAD is logical '1' (> $0.7V_{DD}$).