April 2002

FAIRCHILD SEMICONDUCTOR®

FDG901D

Slew Rate Control Driver IC for P-Channel MOSFETs

General Description

The FDG901D is specifically designed to control the turn on of a P-Channel MOSFET in order to limit the inrush current in battery switching applications with high capacitance loads. During turn-on the FDG901D drives the MOSFET's gate low with a regulated current source, thereby controlling the MOSFET's turn on. For turn-off, the IC pulls the MOSFET gate up quickly, for efficient turn off.

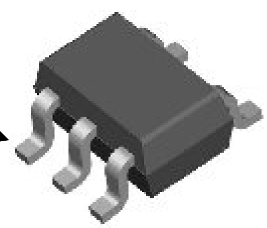
Applications

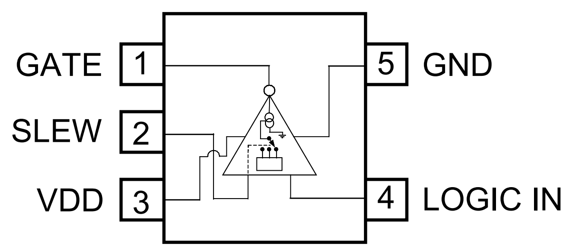
- Power management
- Battery Load switch

Features

- Three Programmable slew rates
- Reduces inrush current
- Minimizes EMI
- Normal turn-off speed
- Low-Power CMOS operates over wide voltage range
- Compact industry standard SC70-5 surface mount package

pin 1





Absolute Maximum Ratings $T_A=25^oC$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DD}	Supply Voltage	-0.5 to 10	V
V_{IN}	DC Input Voltage (Logic Inputs)	-0.7 to 6	V
P_D	Power Dissipation for Single Operation @ 85°C	150	mW
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-65 to +150	°C

Recommended Operating Range

V_{DD}	Supply Voltage	2.7 to 6.0	V
T_J	Operating Temperature	-40 to +125	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	425	°C/W

Package Marking and Ordering Information

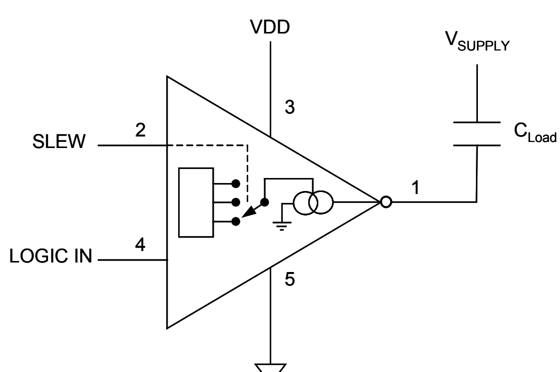
Device Marking	Device	Reel Size	Tape width	Quantity
91	FDG901D	7''	8mm	3000 units

Electrical Characteristics

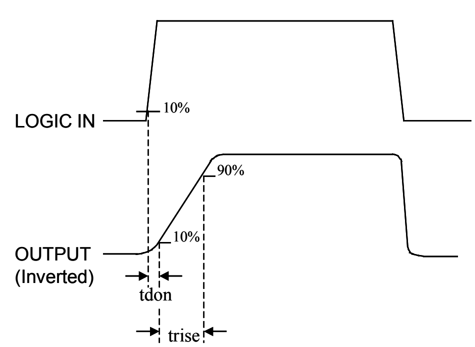
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Logic Levels						
V_{IH}	Logic HIGH Input Voltage	V_{DD} = 2.70V to 6.0 V	75% of V_{DD}			V
V_{IL}	Logic LOW Input Voltage	V_{DD} = 2.70V to 6.0 V			25% of V_{DD}	V
OFF Characteristics						
BV_{IN}	Logic Input Breakdown Voltage	I_{IN} = 10µA, V_{SLEW} = 0 V	9			V
BV_{SLEW}	Slew Input Breakdown Voltage	I_{SLEW} = 10µA, V_{IN} = 0 V	9			V
BV_{DG}	Supply Input Breakdown Voltage	I_{DG} = 10µA, V_{IN} = 0 V, V_{SLEW} = 0 V	9			V
I_{RIN}	LOGIC Input Leakage Current	V_{IN} = 8 V, V_{SLEW} = 0 V			100	nA
I_{RSLEW}	SLEW Input Leakage Current	V_{SLEW} = 8 V, V_{IN} = 0 V			100	nA
I_{RDG}	Supply Input Leakage Current	V_{DG} = 8 V, V_{IN} = 0 V, V_{SLEW} = 0 V			100	nA
ON Characteristics						
I_G	Gate Current	V_{IN} = 6V, V_{GATE} = 2V, SLEW = OPEN		90	120	µA
		SLEW = GND		1	10	µA
		SLEW = V_{DD}		10	50	nA
Switching Characteristics						
t_{don}	Output Turn-On Delay Time Slew Pin = OPEN	V_{Supply} = 5.5 V, V_{DD} = 5.5 V, Logic IN = 5.5 V, C_{LOAD} = 510 pF, Test Circuit		8.3		µs
t_{don}	Output Turn-On Delay Time Slew Pin = GROUND			0.6		ms
t_{don}	Output Turn-On Delay Time Slew Pin = VDD			2.2		ms
t_{rise}	Output Rise Time Slew Pin = OPEN	V_{Supply} = 5.5 V, V_{DD} = 5.5 V, Logic IN = 5.5 V, C_{LOAD} = 510 pF, Test Circuit		28		µs
t_{rise}	Output Rise Time Slew Pin = GROUND			1.8		ms
t_{rise}	Output Rise Time Slew Pin = VDD			11		ms
dv/dt	Output Slew Rate Slew Pin = OPEN	V_{Supply} = 5.5 V, V_{DD} = 5.5 V, Logic IN = 5.5 V, C_{LOAD} = 510 pF, Test Circuit		162		V/ms
dv/dt	Output Slew Rate Slew Pin = GROUND			2.6		V/ms
dv/dt	Output Slew Rate Slew Pin = VDD			0.3		V/ms

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



Test Circuit



Switching Waveforms

Typical Characteristics

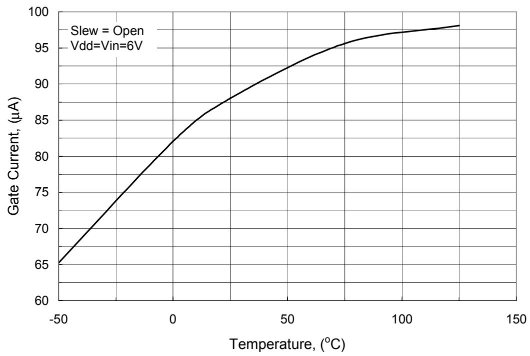


Figure 1. GATE Output current vs. Temperature. SLEW = OPEN

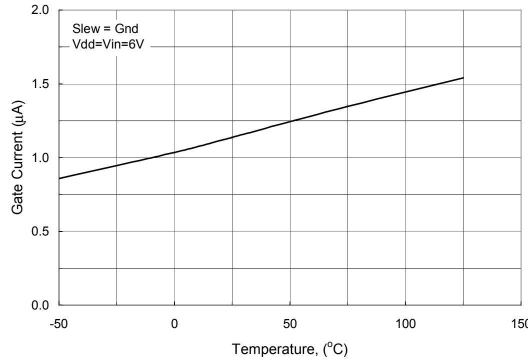


Figure 2. GATE Output current vs. Temperature. SLEW = Ground

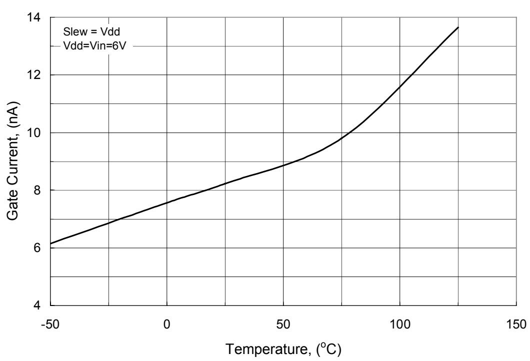


Figure 3. GATE Output current vs. Temperature. SLEW = V_{DD}

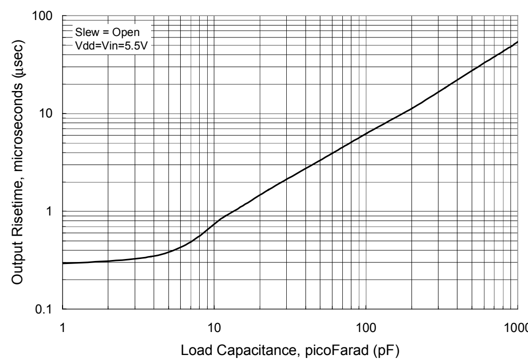


Figure 4. t_{rise} vs. Load Capacitance. SLEW = OPEN

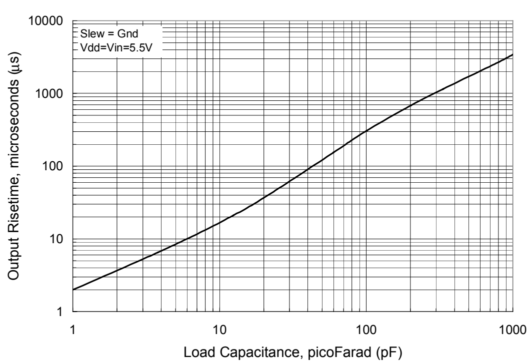


Figure 5. t_{rise} vs. Load Capacitance. SLEW = GROUND

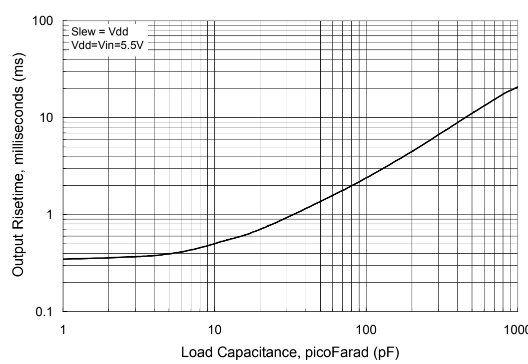
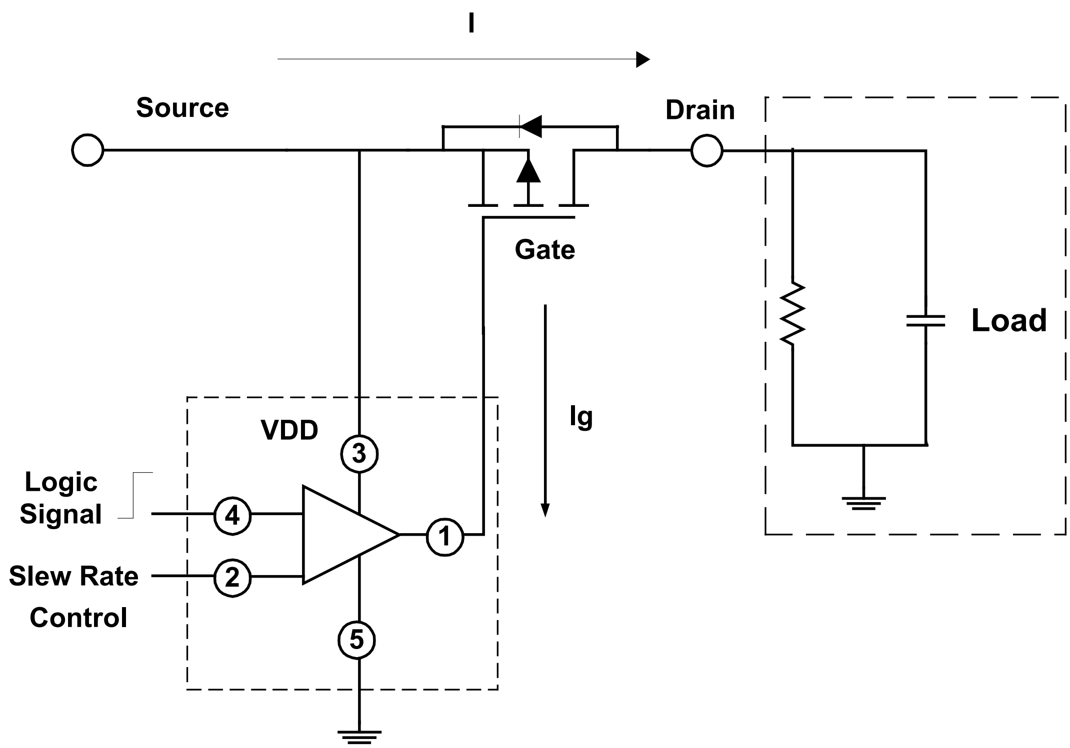


Figure 6. t_{rise} vs. Load Capacitance. SLEW = V_{DD}



Application Circuit

Typical Application

Battery powered systems make extensive usage of load switching, turning the power to subsystems off, in order to extend battery life. Power MOSFETs are used to accomplish this task. In PDA's and Cell phones, these MOSFETs are usually low threshold P-Channels. Since the loads typically include bypass capacitor components (high capacitive component), a high inrush current can occur when the load is switched on. This inrush current can cause transients on the main power supply disturbing circuitry supplied by it.

The simplest method of limiting the inrush current is to control the slew rate of the MOSFET switch. This can be done with external R/C circuits, but this approach can occupy significant PCB area, and involves other compromises in performance. The slew rate control driver IC FDG901D is specifically designed to interface low voltage digital circuitry with power MOSFETs and reduce the rapid inrush current in load switch applications. The IC limits inrush current by controlling the current, which drives the gate of the P-Channel MOSFET switch.

The control input is a CMOS compatible input with a minimum high input voltage of 2.55V with a power rail voltage of 6V. Therefore, it is compatible with any CMOS logic voltages between 2.55V and 5V and under these conditions there is no additional configuration required.

The Slew Rate Control Driver (FDG901D) is designed to give a programmed choice of one of three steady dv/dt states on the output during turn-on. To change the dv/dt value, the user needs to use the Slew Rate Control Pin (Pin 2). To utilize the smallest current setting (≈10 nA) from the IC, a voltage equal to Vdd must be applied to the Slew Rate Control Pin 2. To use the next higher current setting (≈1 μA) a voltage equal to Ground must be applied to Pin 2. To achieve the highest current setting (≈ 80 μA) or obtain a faster switching speed, the Slew Rate Pin2 must be open (floating). A higher value of capacitance will result in a slower switching rate. To determine the switching times of each setting use the simple equation:

$$t = \frac{Q_g}{I_G}$$

where Q_g is the Gate charge in nC for a given MOSFET and I_G is the gate current controlled by the slew rate pin.

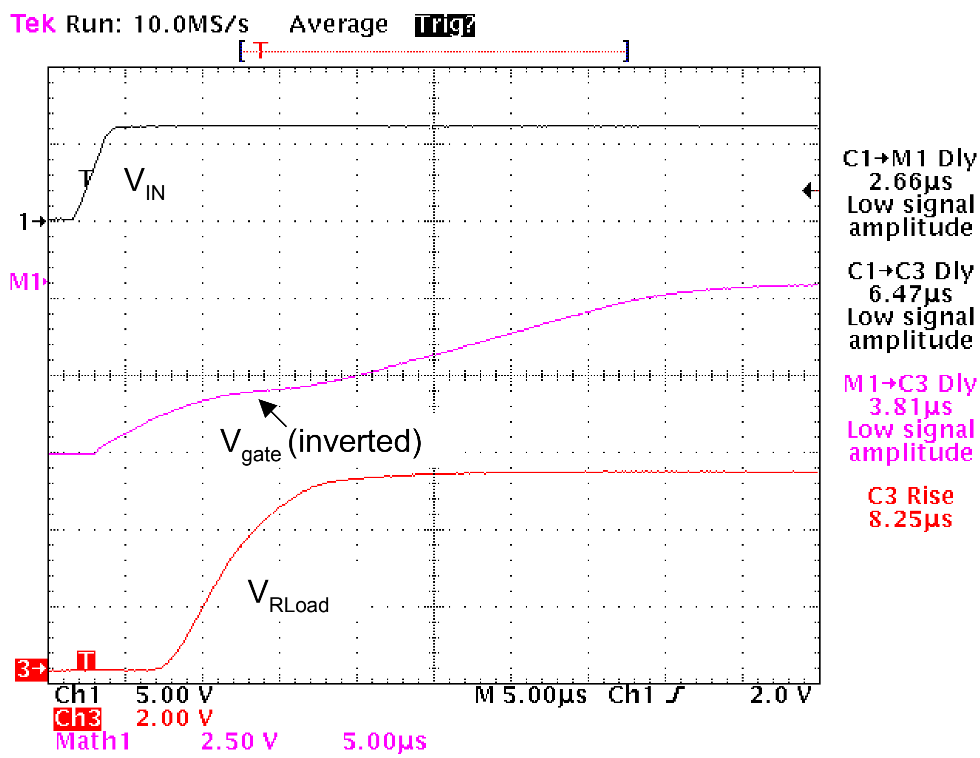
Below is a captured image from an oscilloscope depicting the device response. The FDG901D was connected to control an FDG258P P-Channel DMOS. The Slew Rate control pin was set to open (floating state).

Test Conditions:

V_{DD} = 5.5V

V_{IN} = 5.5V

R_{LOAD} = 1.5Ω



Circuit waveforms for an FDG901D controlling a P-Channel FDG258P MOSFET.

TRADEMARKS

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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