Intronics Power ®

14-Bit & 15-Bit Sampling Analog To Digital Converter

DAS1152/DAS1153

FEATURES

- Complete with High Accuracy Sample/Hold and A/D Converter
- Differential Nonlinearity: ±0.002% FSR max (DAS1153)
- Nonlinearity: DAS1152: ±0.005% FSR max
  DAS1153: ±0.003% FSR max
- Low Differential Nonlinearity T.C.: ±2ppm/°C max
- High Throughput Rate: 25kHz min (DAS1152)
- High Feedthrough Rejection: −96dB
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules
- Low Cost

APPLICATIONS

- Process Control Data Acquisition
- Automated Test Equipment
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Robotics

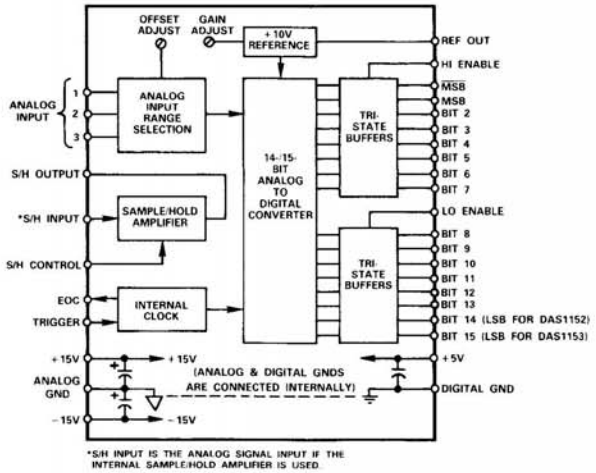

Figure 1. DAS1152/DAS1153 Block Diagram

GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

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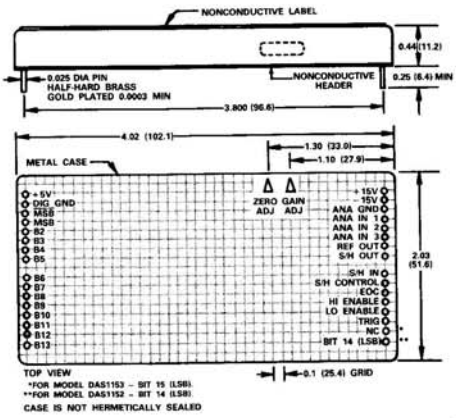
SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE		
Throughput Rate	25kHz min	20kHz min
Conversion Time	35µs max	44µs max
S/H Acquisition Time	4µs max	5µs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	−96dB	*
Droop Rate	0.05µV/µs (0.1µV/µs max)	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max
Differential Nonlinearity	±0.003% FSR[3] max	±0.002% FSR[3] max
No Missing Codes	Guaranteed	*
±3σ Noise (S/H plus A/D)	75µV rms	*
±3σ Noise (A/D)	50µV rms	*
STABILITY		
Differential Nonlinearity T.C.	±2ppm/°C max	*
Gain T.C.	±8ppm/°C max	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	±5V, ±10V	*
Unipolar	0 to +5V, 0 to +10V	*
ADC Input Impedance 0 to +5V	2.5kΩ	*
0 to +10V, ±5V	5kΩ	*
±10V	10.0kΩ	*
S/H Input Impedance	100MΩ‖5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	±5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	±15V (±3%), +5V (±5%)	*
Operating Voltages[5]	±12V to +17V, +4.75V to +5.25V	*
Supply Current Drain ±15V	±37mA	*
+5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES

*Specifications same as DAS1152

[1]Measured in hold mode, input 20V pk-pk @ 10kHz.

[2]Worst-case summation of S/H and A/D nonlinearity errors.

[3]FSR means Full Scale Range.

[4]When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (max, DAS1152)/5µs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2).

[5]If only the ADC portion is used, the operating power supply voltage can be maintained at ±12V to ±17V. But if the S/H section is required, the operating voltage must be maintained at ±15V (±3%) or the S/H input voltage must be limited to −7V to +10V for a ±12V supply voltage.

[6]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OPERATION

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table 1. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table 1. Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

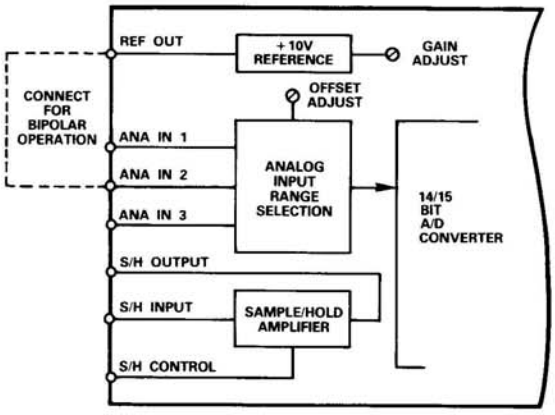


Figure 2. Analog Input Block Diagram

TIMING DIAGRAM

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs (DAS1152)/5μs (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

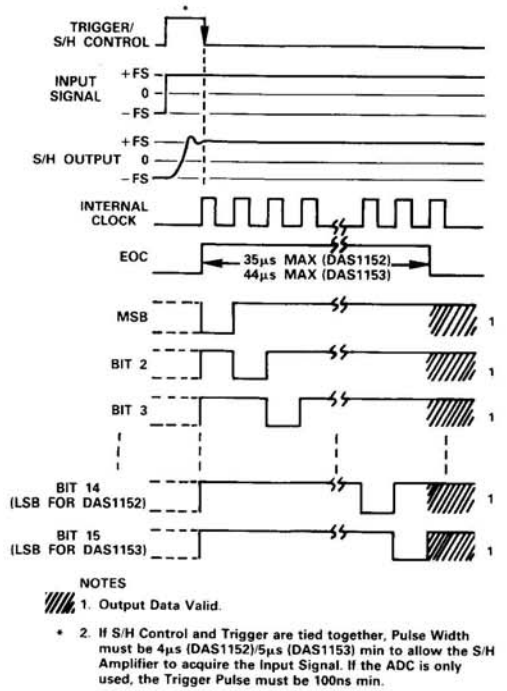


Figure 3. DAS1152/DAS1153 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a 0 to +5V unipolar range set the input to +153μV for the DAS1152 and +76μV for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a ±10V bipolar range set the input voltage precisely to +610μV for the DAS1152 and +305μV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for ±10V units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. Table 2 shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables 3 and 4 show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

ANALOG INPUT			
0 to +5V Range		0 to +10V Range	
DAS1152	DAS1153	DAS1152	DAS1153
+4.99969V	+4.99984V	+9.99939V	+9.99969V
+2.50000V	+2.50000V	+5.0000V	+5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+0.0000V	+0.0000V	+0.0000V	+0.0000V

DIGITAL OUTPUT	
Binary Code	
DAS1152	DAS1153
11 111 111 111 111	111 111 111 111 111
10 000 000 000 000	100 000 000 000 000
00 100 000 000 000	001 000 000 000 000
00 000 000 000 001	000 000 000 000 001
00 000 000 000 000	000 000 000 000 000

Table 2. Unipolar Input-Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99939V	+9.99878V	11 111 111 111 111	01 111 111 111 111
+2.50000V	+5.0000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001
+0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	−10.00000V	00 000 000 000 000	10 000 000 000 000

Table 3. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111
+2.50000V	+5.0000V	110 000 000 000 000	010 000 000 000 000
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	−10.00000V	000 000 000 000 000	100 000 000 000 000

Table 4. DAS1153 Bipolar Input/Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.