

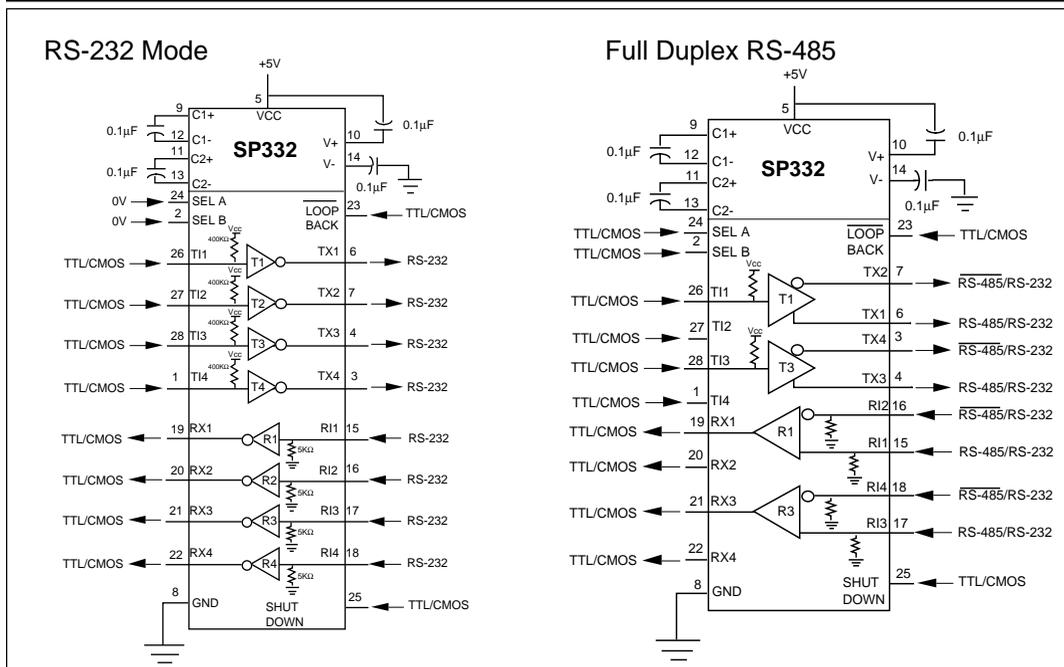
## RS-232/RS-485 Multi-Mode Serial Transceiver

- +5V-Only Single Supply Operation
- 4 Drivers, 4 Receivers RS-232
- 2 Drivers, 2 Receivers RS-485
- Loop Back Function for Self Test
- 28 Pin SOIC Packaging



### DESCRIPTION...

The **SP332** is a monolithic device that contains both RS-232 and RS-485 line drivers and receivers. The configuration of the **SP332** can be changed at any time by changing the logic state of two control input pins. The device also includes a loop back function which internally connects driver outputs to receiver inputs for a chip self test. A **Sipex**-patented charge pump (5,306,954) allows +5V-only operation.



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V <sub>CC</sub> .....	+12V
Input Voltages	
Logic.....	-0.5V to (V <sub>CC</sub> +0.5V)
Drivers.....	-0.5V to (V <sub>CC</sub> +0.5V)
Receivers.....	±30V@≤100mA
Driver Outputs.....	±15V
Storage Temperature.....	-65°C to +150°C
Power Dissipation.....	1000mW

## SPECIFICATIONS

T<sub>MIN</sub> to T<sub>MAX</sub> and V<sub>CC</sub> = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RS-485 DRIVER</b>					
<b>DC Characteristics</b>					
Differential Output Voltage	GND		V <sub>CC</sub>	Volts	Unloaded; R=∞; <i>see figure 1</i>
Differential Output Voltage	2.0		5.0	Volts	With Load; R=50Ω (RS-422); <i>see figure 1</i>
Differential Output Voltage	1.5		5.0	Volts	With Load; R=27Ω (RS-485); <i>see figure 1</i>
Change in Magnitude of Driver Differential Output Voltage for Complementary States			0.2	Volts	R=27Ω or R=50Ω; <i>see figure 1</i>
Driver Common-Mode Output Voltage			3	Volts	R=27Ω or R=50Ω; <i>see figure 1</i>
Input High Voltage	2.0			Volts	Applies to transmitter inputs, SEL A, SEL B, SD, $\overline{\text{LB}}$
Input Low Voltage			0.8	Volts	Applies to SEL A, SEL B, SD, $\overline{\text{LB}}$
Input Current			±10	μA	Applies to:
Pull-Up Current		1.5		μA	transmitter inputs, $\overline{\text{LB}}$
Pull-Down Current		3.0		μA	SEL A, SEL B, SD,
Driver Short-Circuit Current					
V <sub>OUT</sub> = HIGH	35		250	mA	-7V≤V <sub>O</sub> ≤10V
V <sub>OUT</sub> = LOW	35		250	mA	-7V≤V <sub>O</sub> ≤10V
<b>AC Characteristics</b>					
Driver Data Rate	10			Mbps	
Driver Input to Output		70	180	ns	R <sub>DIFF</sub> =54Ω, C <sub>L1</sub> =C <sub>L2</sub> =100pF; <i>see figures 3 and 6</i>
t <sub>PLH</sub> Driver Input to Output		70	180	ns	R <sub>DIFF</sub> =54Ω, C <sub>L1</sub> =C <sub>L2</sub> =100pF; <i>see figures 3 and 6</i>
t <sub>PHL</sub> Driver Skew		5	10	ns	From output to output; <i>see figures 3 and 6</i>
Driver Rise or Fall Time	3	15	40	ns	From 10% to 90%; R <sub>DIFF</sub> =54Ω, C <sub>L1</sub> =C <sub>L2</sub> =100pF; <i>see figures 3 and 6</i>
<b>RS-485 RECEIVER</b>					
<b>DC Characteristics</b>					
Differential Input Threshold	-0.2		+0.2	Volts	-7V≤V <sub>CM</sub> ≤12V
Input Hysteresis		70		mV	V <sub>CM</sub> =0V
Output Voltage High	3.5			Volts	I <sub>O</sub> =-4mA, V <sub>ID</sub> =+200mV
Output Voltage Low			0.4	Volts	I <sub>O</sub> =+4mA, V <sub>ID</sub> =-200mV
Input Resistance	12	15		kΩ	-7V≤V <sub>CM</sub> ≤12V
Input Current (A, B); V <sub>IN</sub> = 12V			+1.5	mA	V <sub>IN</sub> = 12V, A is the non-inverting receiver input. B is the inverting receiver input
Input Current (A, B); V <sub>IN</sub> = -7V			-0.8	mA	V <sub>IN</sub> = -7V
Short Circuit Current			85	mA	0V≤V <sub>CM</sub> ≤V <sub>CC</sub>

## SPECIFICATIONS (CONTINUED)

$T_{MIN}$  to  $T_{MAX}$  and  $V_{CC} = 5V \pm 5\%$  unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>AC Characteristics</b> Receiver Data Rate Receiver Input to Output $t_{PLH}$ Receiver Input to Output $t_{PHL}$ Diff. Receiver Skew $ t_{PLH} - t_{PHL} $	10	130	250	Mbps ns ns ns	$R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100pF$ ; <i>Figures 3 and 8</i> $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100pF$ ; <i>Figures 3 and 7</i> $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100pF$ ; <i>Figures 3 and 7</i>
<b>RS-232 DRIVER</b> <b>DC Characteristics</b> TTL Input Levels $V_{IL}$ $V_{IH}$ Voltage Outputs High Level Output Low Level Output Open Circuit Output Short Circuit Current Power Off Impedance			0.8	Volts Volts Volts Volts Volts mA Ohms	Applies to transmitter inputs, SEL A, SEL B, SD, LB Applies to transmitter inputs, SEL A, SEL B, SD, LB $R_T = 3k\Omega$ to Gnd $R_T = 3k\Omega$ to Gnd $R_L = \infty$ $V_{OUT} = 0V$ $V_{CC} = 0V$ ; $V_{OUT} = \pm 2V$
<b>AC Characteristics</b> Transmission Rate Transition Time Propagation Delay $t_{PHL}$ $t_{PLH}$ Slew Rate	120		1.56	kbps $\mu s$ $\mu s$ $\mu s$ $V/\mu s$	Rise/fall time, +3V to -3V; -3V to +3V $R_L = 3k\Omega$ , $C_L = 2500pF$ $R_T = 3k\Omega$ , $C_i = 2500pF$ ; From 1.5V of $T_{IN}$ to 50% of $V_{OUT}$ $R_T = 3k\Omega$ , $C_i = 2500pF$ ; From 1.5V of $T_{IN}$ to 50% of $V_{OUT}$ $R_T = 3k\Omega$ , $C_i = 50pF$ ; From +3V to -3V or -3V to +3V
<b>RS-232 RECEIVER</b> TTL Output Levels $V_{OL}$ $V_{OH}$ Receiver Input High Threshold Low Threshold Input Voltage Range Input Impedance Hysteresis	3.5	2.1	0.4	Volts Volts Volts Volts kOhms Volts	$I_{SINK} = 4mA$ $I_{SOURCE} = -4mA$ $V_{IN} = \pm 15V$ $V_{CC} = +5V$
<b>AC Characteristics</b> Transmission Rate Transition Time Propagation Delay $t_{PHL}$ $t_{PLH}$	120	50		kbps ns ns ns ns	Rise/fall time 10% to 90% From 50% of $V_{IN}$ to 1.5V of $R_{OUT}$ From 50% of $V_{IN}$ to 1.5V of $R_{OUT}$
<b>POWER REQUIREMENTS</b> No Load Supply Current Full Load Supply Current Shutdown Supply Current		19	25	mA mA $\mu A$	No load; $V_{CC} = 5.0V$ ; $T_A = 25^\circ C$ RS-232 drivers $R_L = 3k\Omega$ to Gnd; DC Input RS-485 drivers $R_L = 54\Omega$ from A to B; DC Input $T_A = 25^\circ C$ , $V_{CC} = 5.0V$

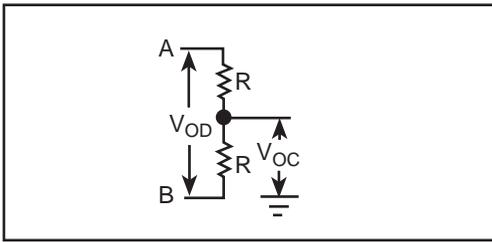


Figure 1. RS-485 Driver DC Test Load Circuit

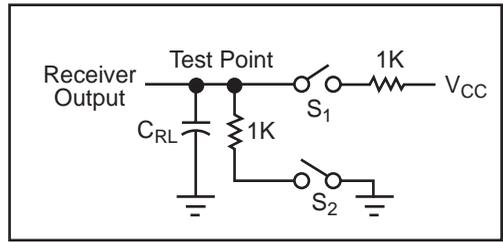


Figure 2. Receiver Timing Test Load Circuit

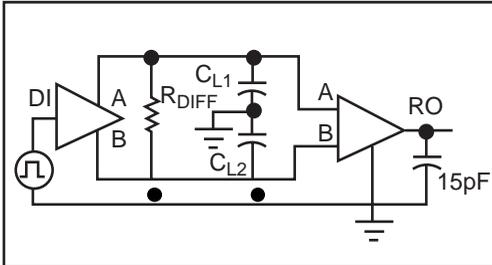


Figure 3. RS-485 Driver/Receiver Timing Test Circuit

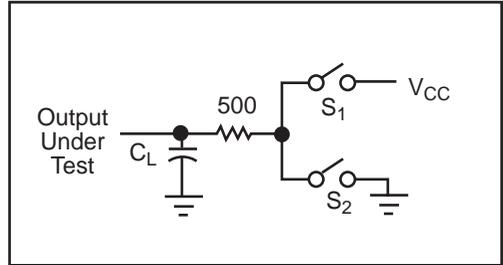


Figure 4. RS-485 Driver Timing Test Load #2 Circuit

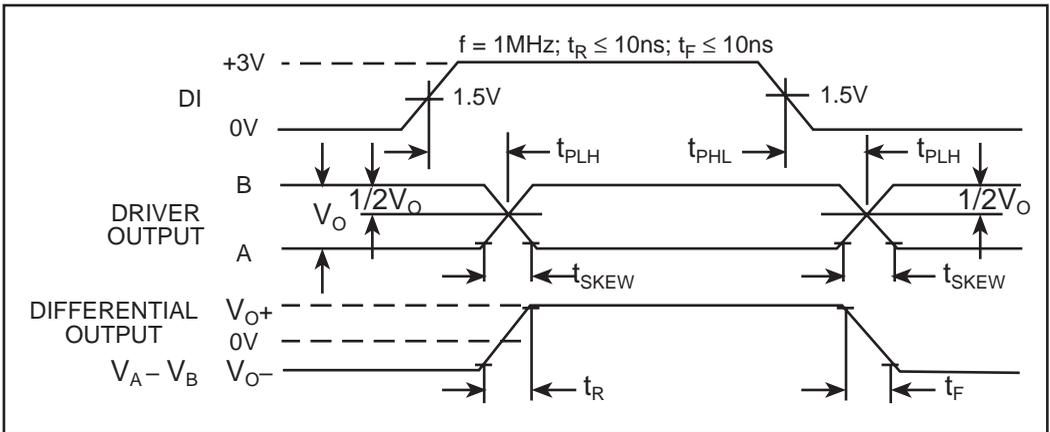


Figure 6. RS-485 Driver Propagation Delays

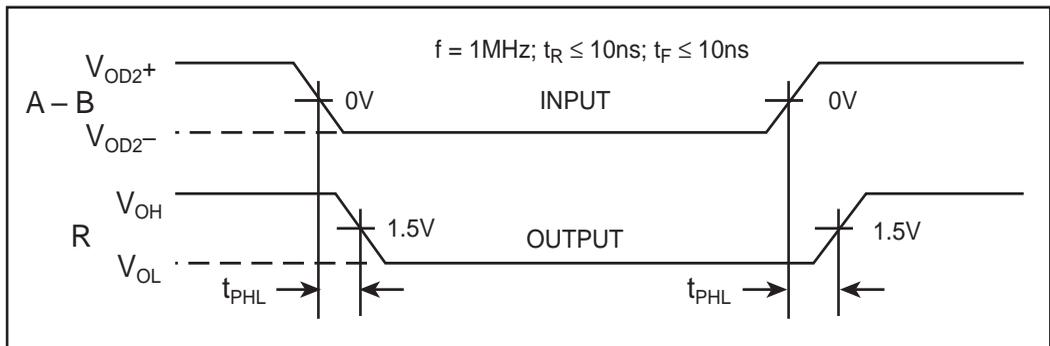


Figure 7. RS-485 Receiver Propagation Delays

## THEORY OF OPERATION...

The **SP332** is a single chip device that can be configured via software for either RS-232, RS-485 or both interface modes at any time. The **SP332** is made up of three basic circuit elements, single-ended drivers and receivers, differential drivers and receivers and charge pump.

## DIFFERENTIAL DRIVER/RECEIVER...

### RS-485, RS-422 Drivers...

The differential drivers and receivers comply with the RS-485 and RS-422 standards. The driver circuits are able to drive a minimum of 1.5V when terminated with a 54 $\Omega$  resistor across the two outputs. The typical propagation delay from the driver input to output is 60ns. The driver outputs are current limited to less than 250mA, and can tolerate short circuits to ground, or to any voltage within a +10V to -7V range with no damage.

### RS-485, RS-422 Receivers...

The differential receivers of the **SP332** comply with the RS-485, RS-422 and V.11 standards. The input to the receiver is equipped with a common mode range of +12V to -7V. The input threshold over this range is a minimum of  $\pm 200$ mV. The differential receivers can receive data up to 10Mbps. The typical propagation delay from the receiver input to output is 90ns.

## SINGLE ENDED DRIVER/RECEIVER...

### RS-232 (V.28) Drivers...

The single-ended drivers and receivers comply with the RS-232E and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is  $\pm 9$ V with no load and is guaranteed to be greater than  $\pm 5$ V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3k $\Omega$  and 2500pF, the four RS-232 drivers can still maintain  $\pm 5$ V output levels. The drivers can operate up to 120kbps; the propagation delay from input to output is typically 2 $\mu$ s.

## RS-232 (V.28) Receivers...

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy transmission lines. The inputs also have a 5k $\Omega$  resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3k $\Omega$ -7k $\Omega$  over a  $\pm 15$ V range. The maximum operating voltage range for the receiver is  $\pm 30$ V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to  $\pm 15$ V levels. The RS-232 receivers can operate up to 120kbps.

## CHARGE PUMP...

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 8a* shows the waveform found on the positive side of capacitor C2, and *Figure 8b* shows the negative side of capacitor C2. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

-V<sub>ss</sub> charge storage- During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to +5V. C1+ is then switched to ground and charge in C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 is now 10V.

### Phase 2

-V<sub>ss</sub> transfer- Phase two of the clock connects the negative terminal of C2 to the V<sub>ss</sub> storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

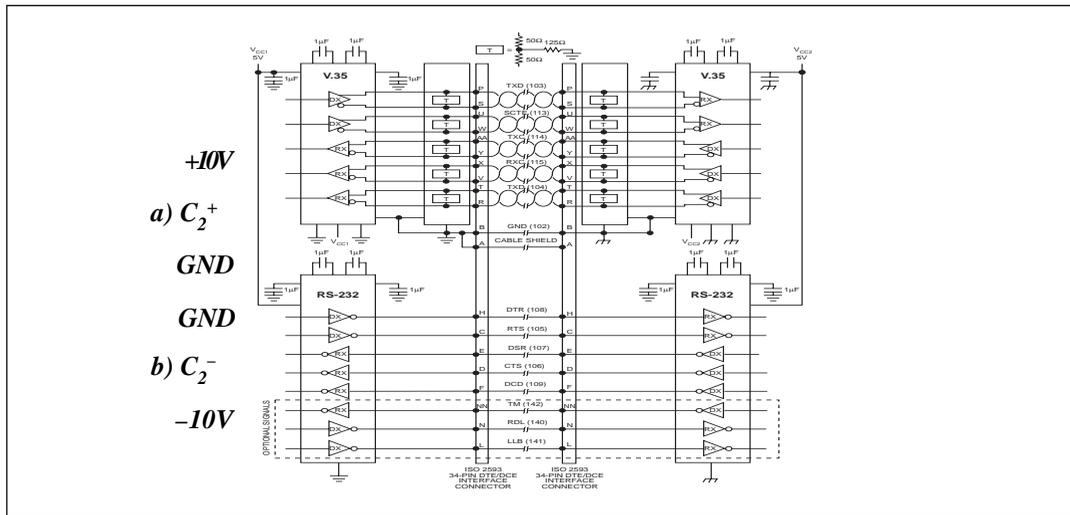


Figure 8. Charge Pump Waveforms

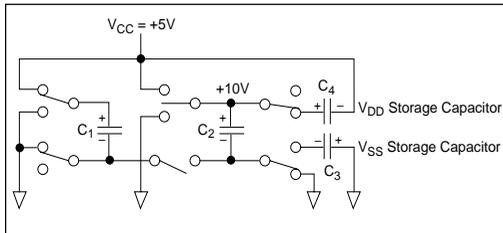


Figure 9. Charge Pump Phase 1

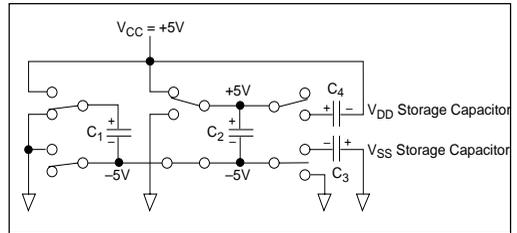


Figure 10. Charge Pump Phase 2

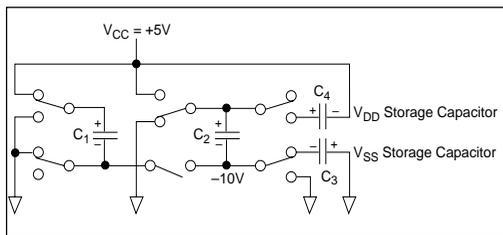


Figure 11. Charge Pump Phase 3

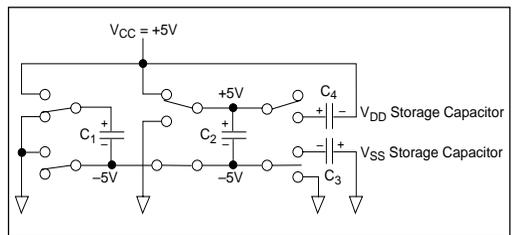


Figure 12. Charge Pump Phase 4

### Phase 3

-Vdd charge storage- The third phase of the clock is identical to the first phase- the transferred charge in C1 produces -5V in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is 10V.

### Phase 4

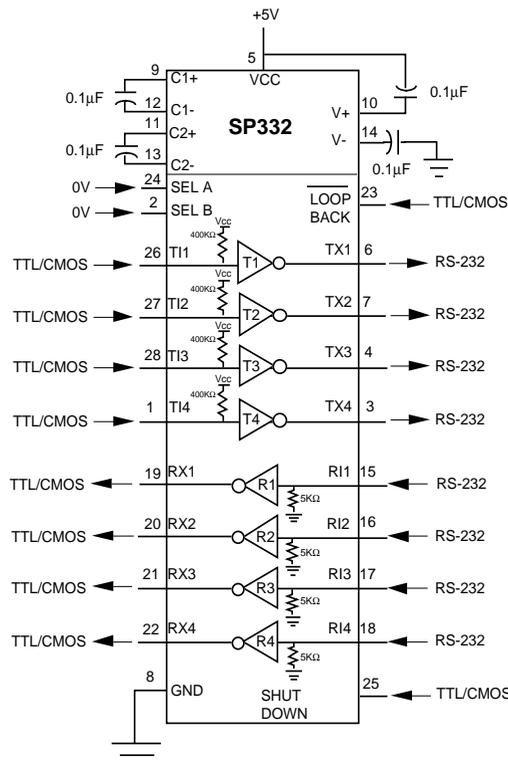
-Vdd transfer- The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated 10V across C2 to C4, the Vdd storage capacitor. Simultaneously with this, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+ and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in the design.

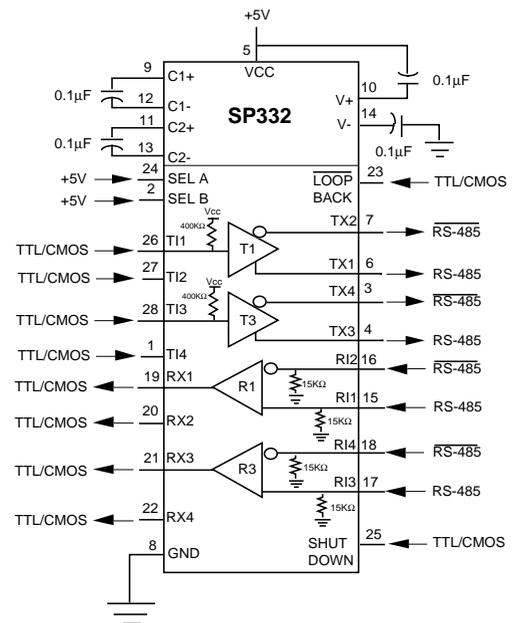
The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 0.1μF with a 16V breakdown rating.

## SP332 TYPICAL OPERATING CIRCUIT

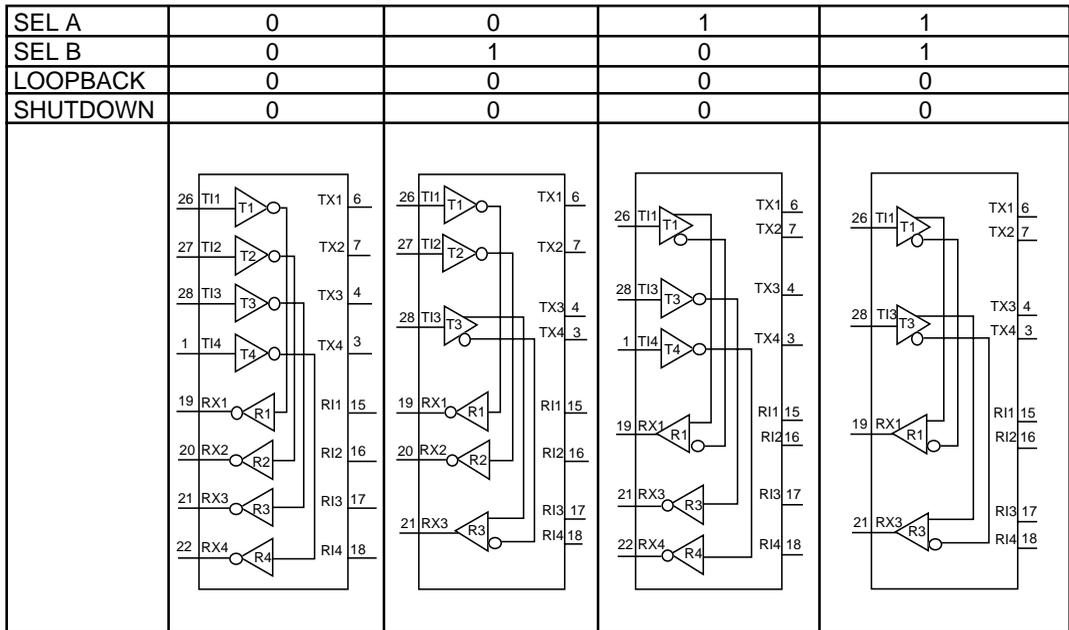
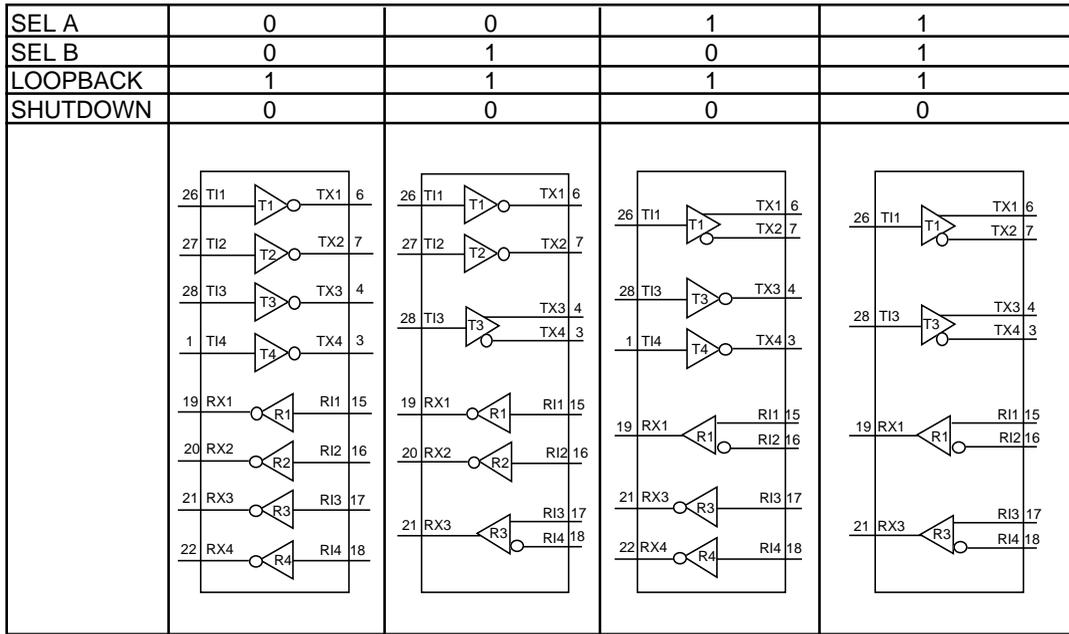
### RS-232 Mode



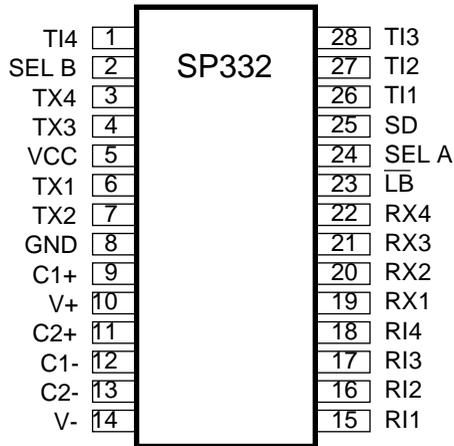
### RS-485 Mode



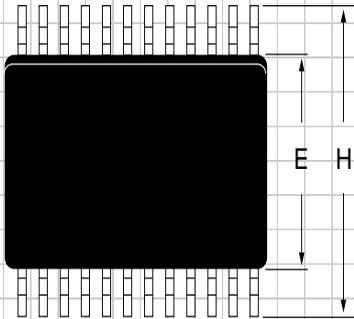
# SP332 CONTROL LOGIC CONFIGURATION



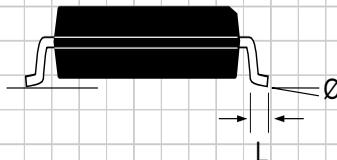
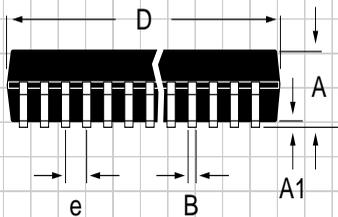
Receiver Inputs are inactive in Loopback Mode ( $\overline{\text{LOOPBACK}} = 0$ )  
 Driver Outputs are Tri-States in Loopback Mode ( $\overline{\text{LOOPBACK}} = 0$ )  
 Unused Outputs are Tri-States



**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	28-PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0 <sup>°</sup> /8 <sup>°</sup> (0 <sup>°</sup> /8 <sup>°</sup> )



## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP332CT .....	0°C to +70°C .....	28-Pin SOIC
SP332ET .....	-40°C to +85°C .....	28-Pin SOIC



SIGNAL PROCESSING EXCELLENCE

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