

# DATA SHEET

## **SA624**

High performance low power FM IF  
system with high-speed RSSI

Product specification  
Replaces data of November 3, 1992  
RF Data Handbook

1997 Nov 07

**Philips Semiconductors**



**PHILIPS**

# High performance low power FM IF system with high-speed RSSI

## SA624

### DESCRIPTION

The SA624 is pin-to-pin compatible with the SA604A, but has faster RSSI rise and fall time. The SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the SA604. The SA624 is available in 16-lead SO (surface-mounted miniature) package.

### FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5 $\mu$ V across input pins (0.22 $\mu$ V into 50 $\Omega$  matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

### PIN CONFIGURATION

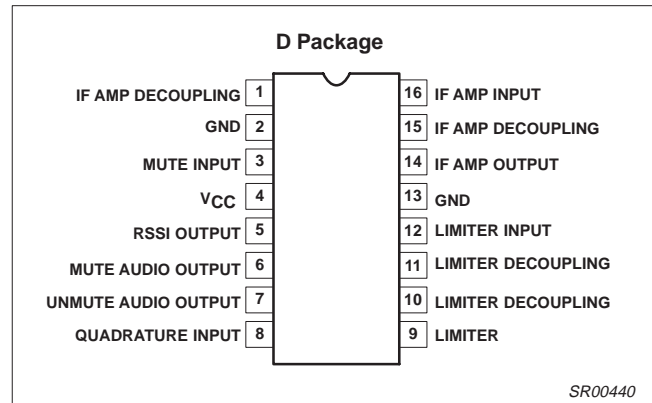


Figure 1. Pin Configuration

### APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

### ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA624D	SOT109-1

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}$	Single supply voltage	9	V
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_A$	Operating ambient temperature range SA624	-40 to +85	°C
$\theta_{JA}$	Thermal impedance D package	90	°C/W

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## BLOCK DIAGRAM

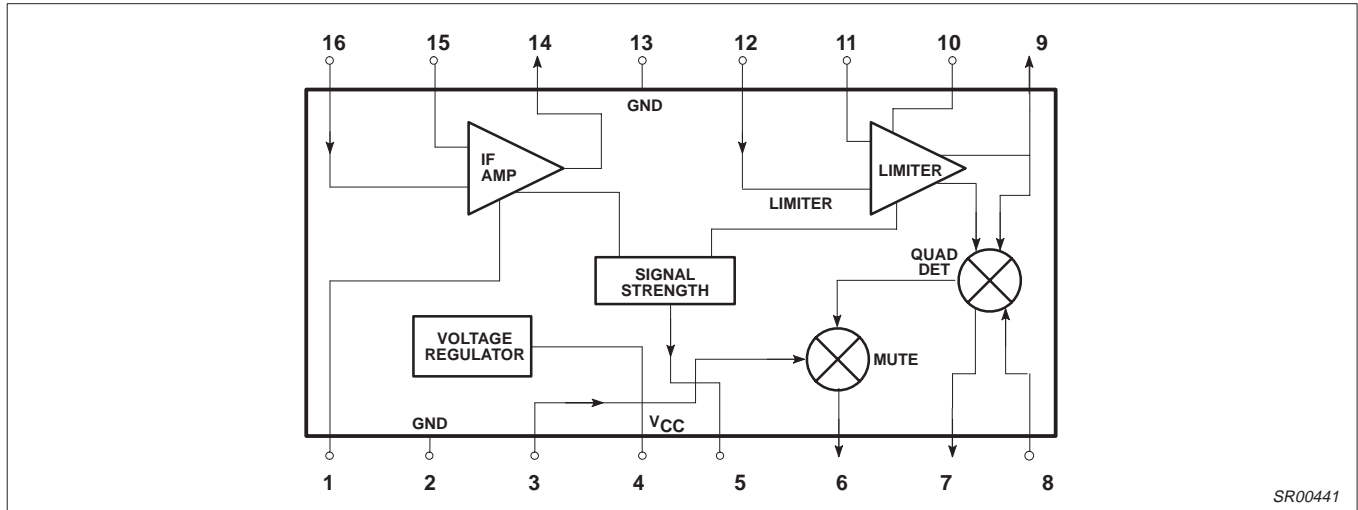


Figure 2. Block Diagram

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +6V$ ,  $T_A = 25^{\circ}C$ ; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA624			
			MIN	TYP	MAX	
$V_{CC}$	Power supply voltage range		4.5		8.0	V
$I_{CC}$	DC current drain		2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		1.0	V V

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## AC ELECTRICAL CHARACTERISTICS

Typical reading at  $T_A = 25^\circ\text{C}$ ;  $V_{CC} = +6\text{V}$ , unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with  $\pm 8\text{kHz}$  peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA624			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50 $\Omega$
	AM rejection	80% AM 1kHz	30	34		dB
	Recovered audio level	15nF de-emphasis	80	175	260	mV <sub>RMS</sub>
	Recovered audio level	150pF de-emphasis		530		mV <sub>RMS</sub>
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	RSSI output <sup>1</sup>	RF level = -118dBm	0	160	650	mV
		RF level = -68dBm	1.9	2.65	3.1	V
		RF level = -18dBm	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz IF level = -44dBm		1.1		$\mu\text{s}$
		IF level = -16dBm		1.2		$\mu\text{s}$
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 10.7MHz IF level = -44dBm		1.2		$\mu\text{s}$
		IF level = -16dBm		1.1		$\mu\text{s}$
		IF freq. = 455kHz IF level = -44dBm		1.3		$\mu\text{s}$
	RSSI output fall time (10kHz pulse, no IF filter)	IF level = -16dBm		4.7		$\mu\text{s}$
		IF freq. = 10.7MHz IF level = -44dBm		1.6		$\mu\text{s}$
		IF level = -16dBm		4.2		$\mu\text{s}$
	RSSI range	$R_4 = 100\text{k}$ (Pin 5)		90		dB
	RSSI accuracy	$R_4 = 100\text{k}$ (Pin 5)		$\pm 1.5$		dB
	IF input impedance		1.4	1.6		k $\Omega$
	IF output impedance		0.85	1.0		k $\Omega$
	Limiter input impedance		1.4	1.6		k $\Omega$
	Limiter output impedance			300		$\Omega$
	Limiter output level no load			280		mV <sub>RMS</sub>
	Unmuted audio output resistance			58		k $\Omega$
	Muted audio output resistance			58		k $\Omega$

### NOTE:

1. SA604 data sheets refer to power at 50 $\Omega$  input termination; about 21dB less power actually enters the internal 1.5k input.

SA604 (50)  
-97dBm  
-47dBm  
+3dBm

SA624 (1.5k)/SA605 (1.5k)  
-118dBm  
-68dBm  
-18dBm

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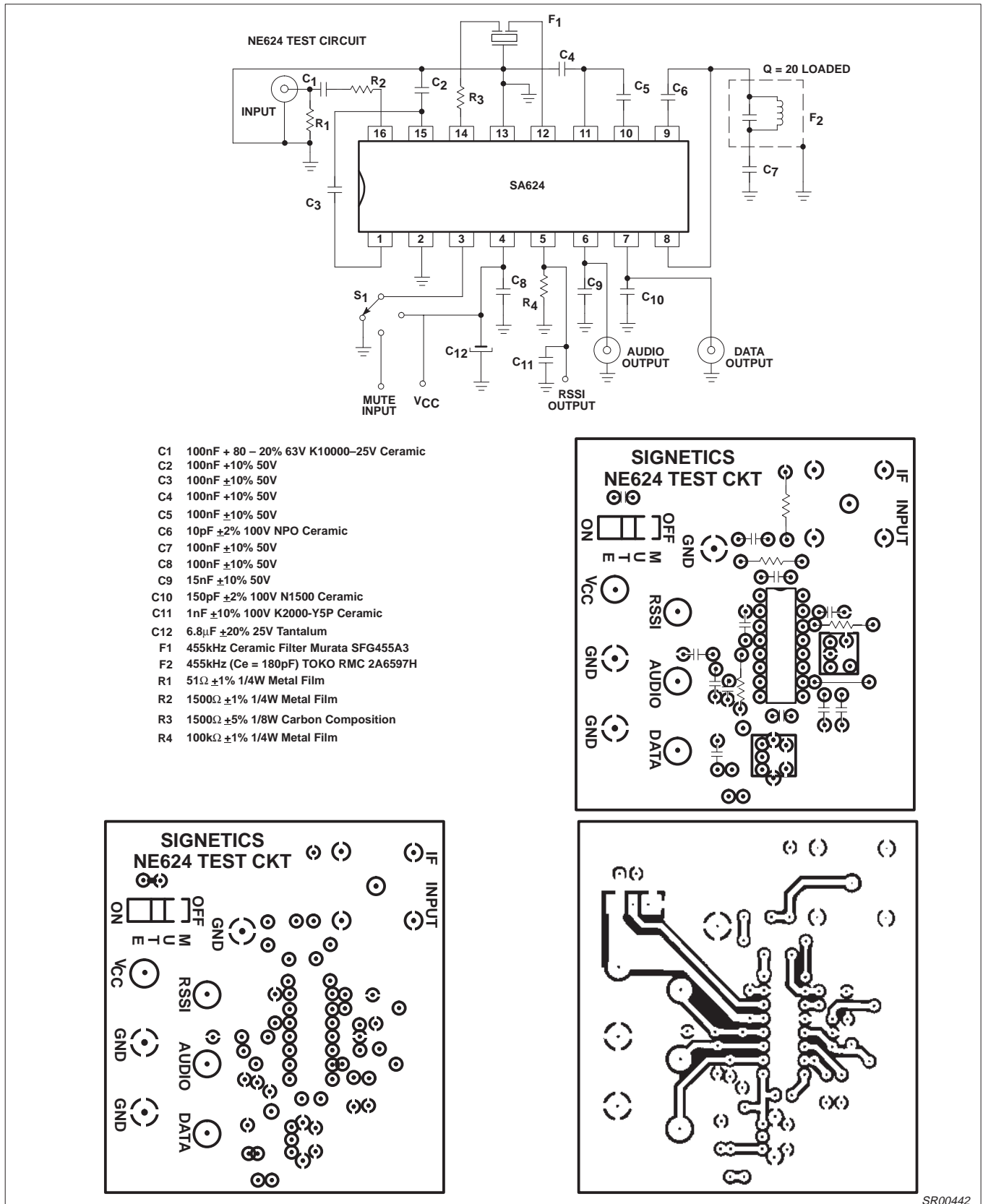


Figure 3. SA624 Test Circuit

SR00442

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## SA624

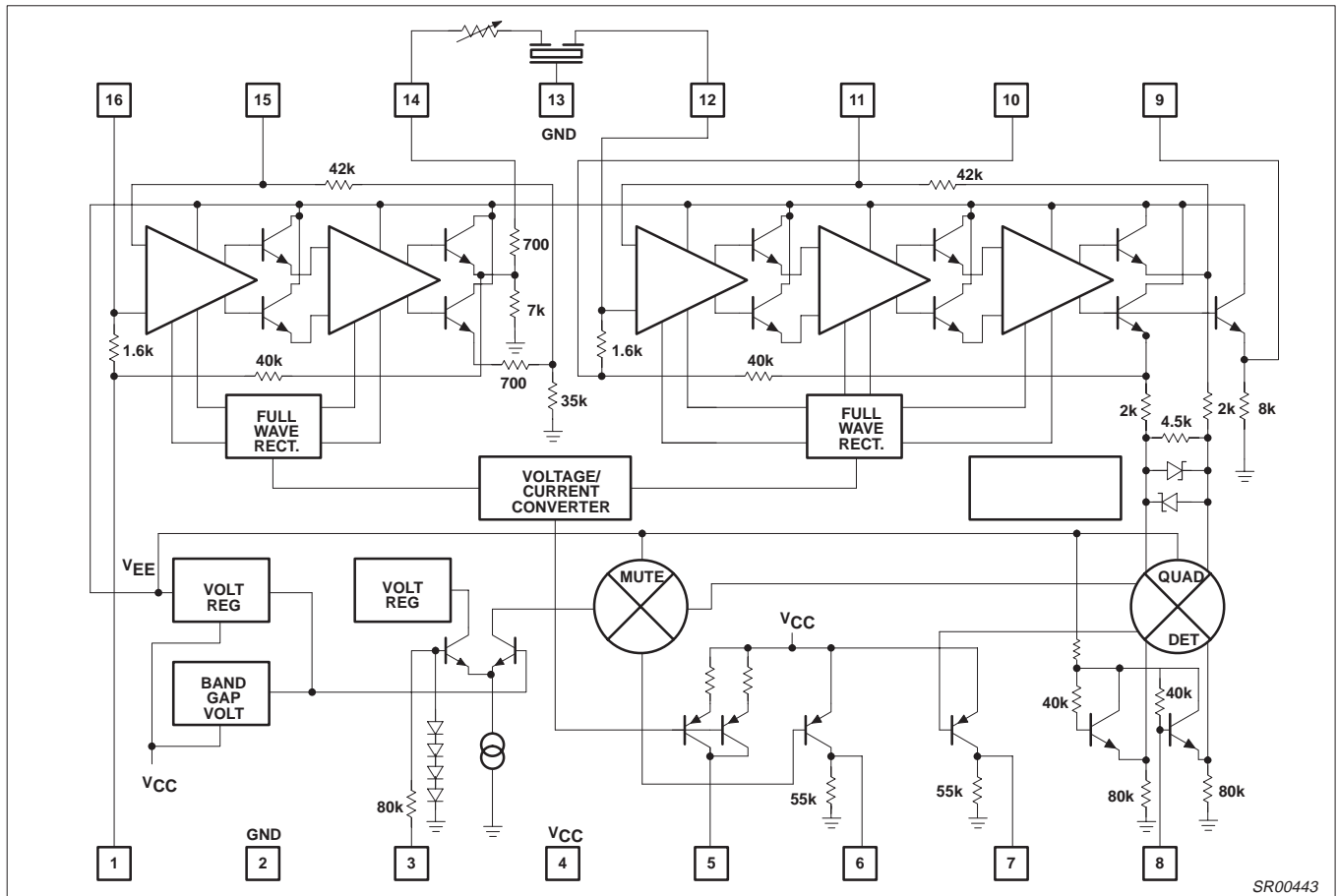


Figure 4. Equivalent Circuit

SR00443

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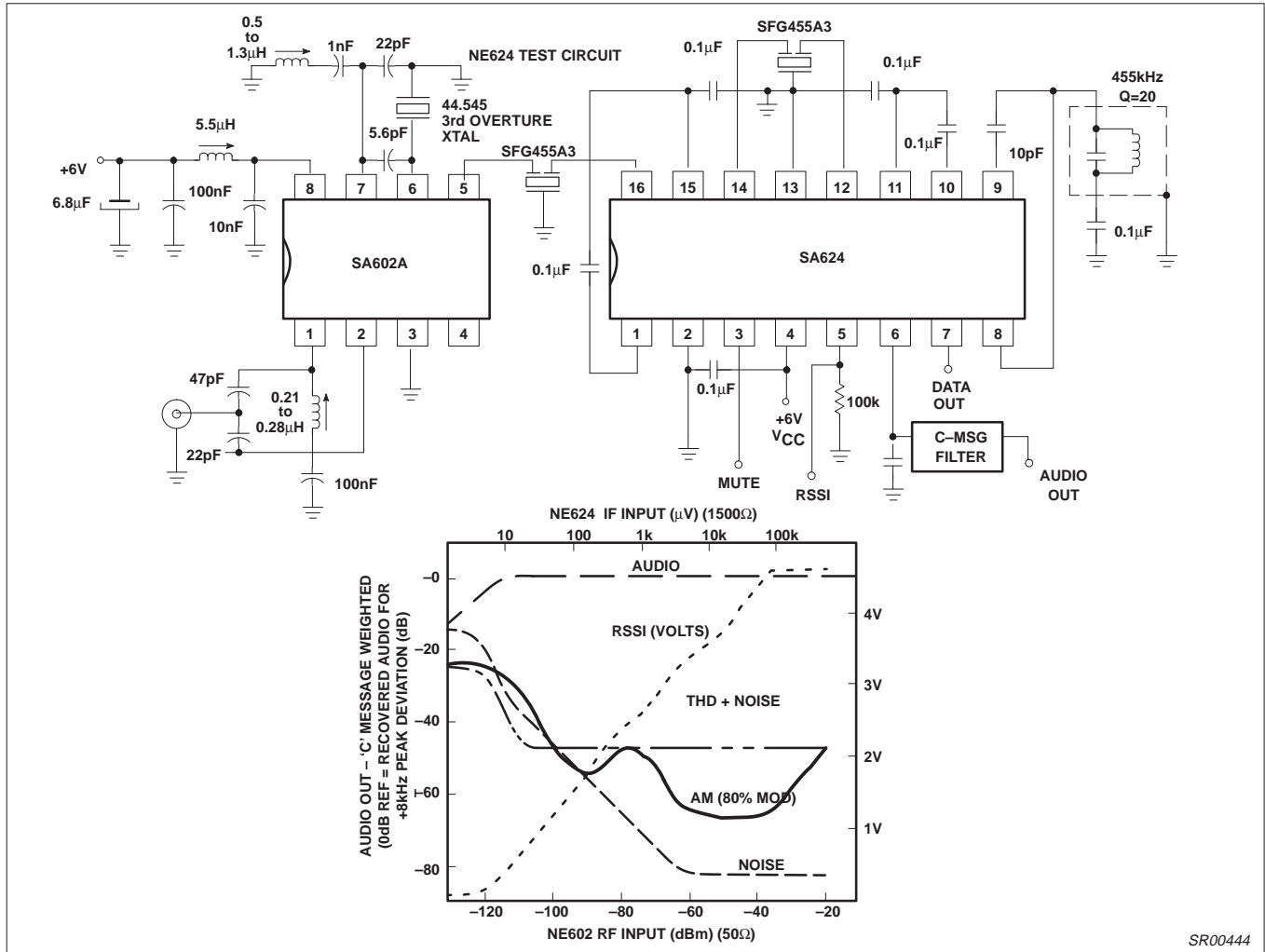


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

## CIRCUIT DESCRIPTION

The SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

## IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector.

One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

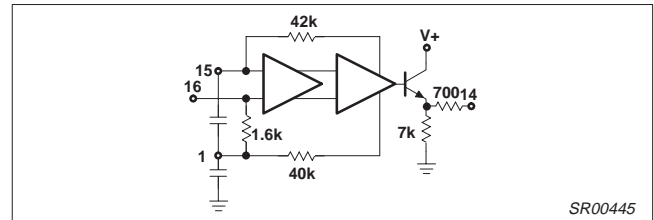


Figure 6. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

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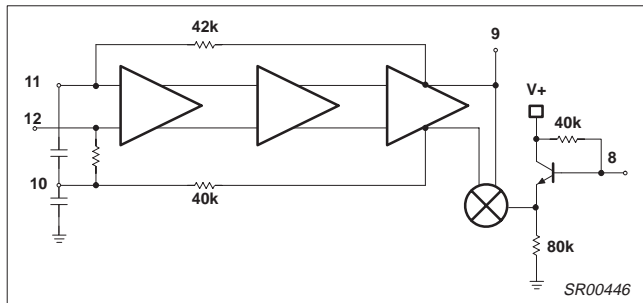


Figure 7. Second Limiter and Quadrature Detector

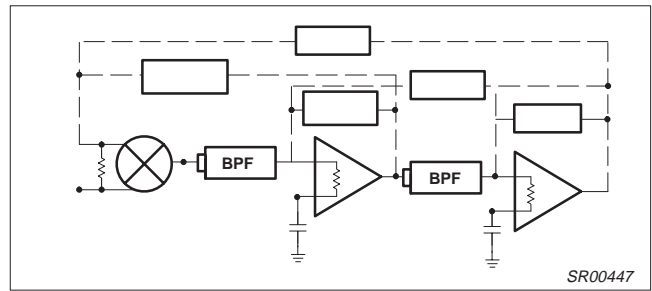


Figure 8. Feedback Paths

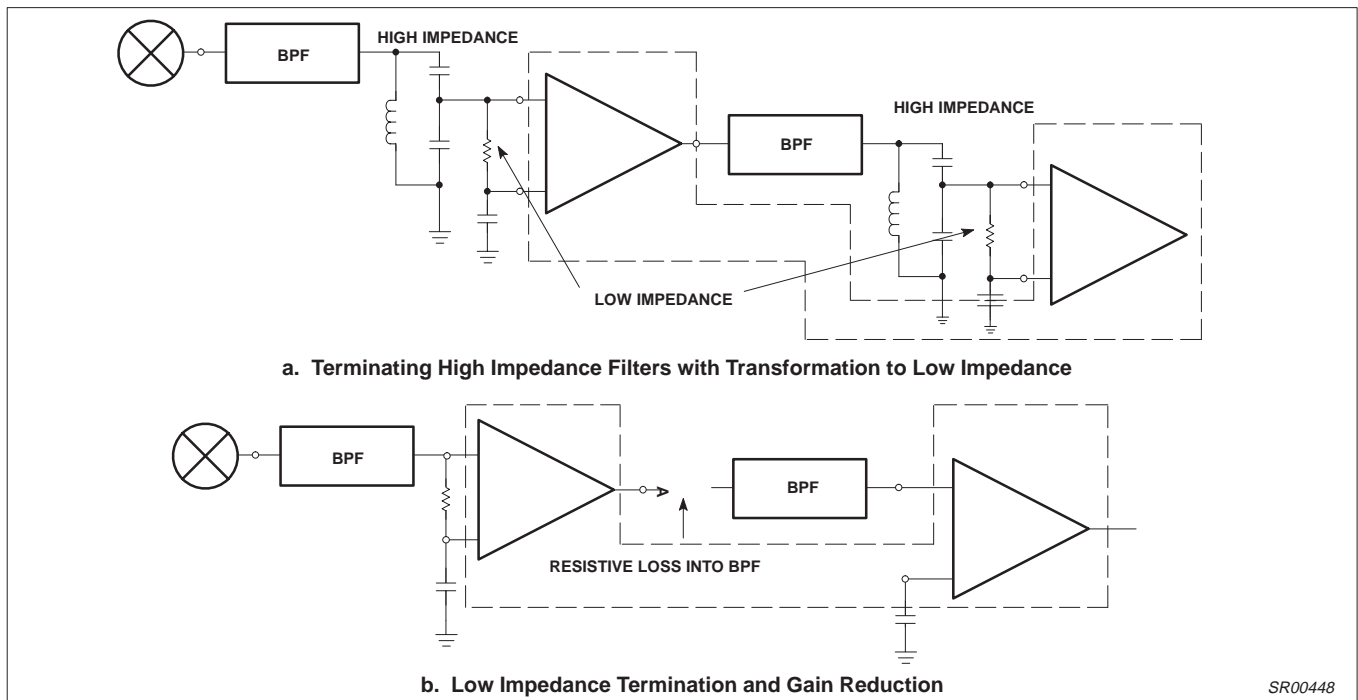


Figure 9. Practical Termination

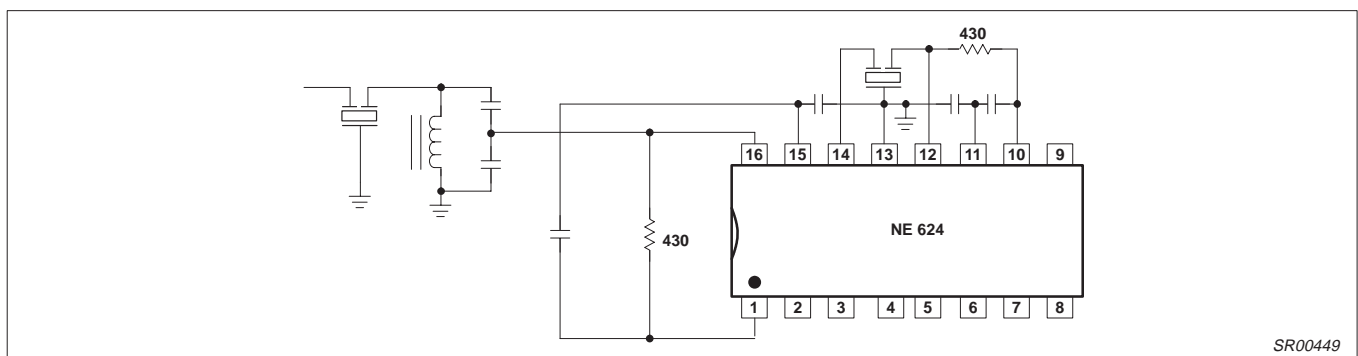


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain

input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be



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accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the SA624 IF amplifiers, which is not specified, is low phase shift. The SA624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

## Stability Considerations

The high gain and bandwidth of the SA624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V<sub>CC</sub> pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

## Quadrature Detector

Figure 7 shows an equivalent circuit of the SA624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

## Frequency Discriminator Design Equations for SA624

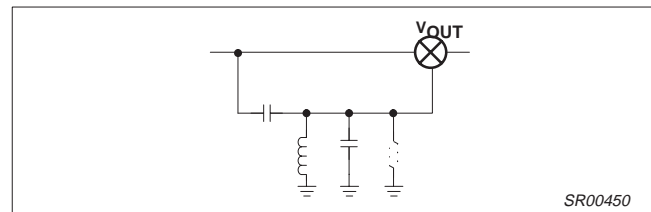


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R (C_P + C_S) \omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C<sub>S</sub> will be:

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$$\phi = \angle V_O - \angle V_{IN} = \tan^{-1} \left[ \frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2} \right] \quad (2)$$

Figure 12 is the plot of  $\phi$  vs.  $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at  $\omega = \omega_1$ , the phase shift is

$\frac{\pi}{2}$  and the response is close to a straight

line with a slope of  $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal  $V_O$  would have a phase shift of

$\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1} \omega\right]$  with respect to the  $V_{IN}$ .

If  $V_{IN} = A \sin \omega t \Rightarrow V_O = A$  (3)

$$\sin \left[ \omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1} \omega \right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$  (4)

$$\sin \left[ \omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1} \omega \right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos \left[ \frac{\pi}{2} - \frac{2Q_1}{\omega_1} \omega \right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin \left( \frac{2Q_1}{\omega_1} \omega \right)$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[ 2Q_1 \left( \frac{\omega_1 + \Delta\omega}{\omega_1} \right) \right] \quad (6)$$

$$\text{For } \frac{2Q_1 \omega}{\omega_1} \ll \frac{\pi}{2}$$

Which is discriminated FM output. (Note that  $\Delta\omega$  is the deviation frequency from the carrier  $\omega_1$ .)

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with  $\pm 5$ kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5 \text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at

$$\frac{\omega}{\omega_1} = 1.01.$$

The curves with  $Q = 100$ ,  $Q = 40$  are not linear, but  $Q = 20$  and less shows better linearity for this application. Too small  $Q$  decreases the amplitude of the discriminated FM signal. (Eq. 6)  $\Rightarrow$  Choose a  $Q = 20$

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$$C_P + C_S = 174 \text{pF and } L = 0.7 \text{mH.}$$

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series

resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a  $C_S = 10 \text{pF}$  and  $C_P = 164 \text{pF}$  (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of  $C_S = 1 \text{pF}$  is recommended.)

## Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with  $55 \text{k}\Omega$  nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal  $180^\circ$  phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a  $180^\circ$  phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

## RSSI

The "received signal strength indicator", or RSSI, of the SA624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a  $5.1 \text{k}\Omega$  resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of  $0.25 \mu\text{V}$  for 12dB SINAD was achieved. With the  $3.6 \text{k}\Omega$  resistor, sensitivity was optimized at  $0.22 \mu\text{V}$  for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry,

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will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about

100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

### Additional Circuitry

Internal to the SA624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

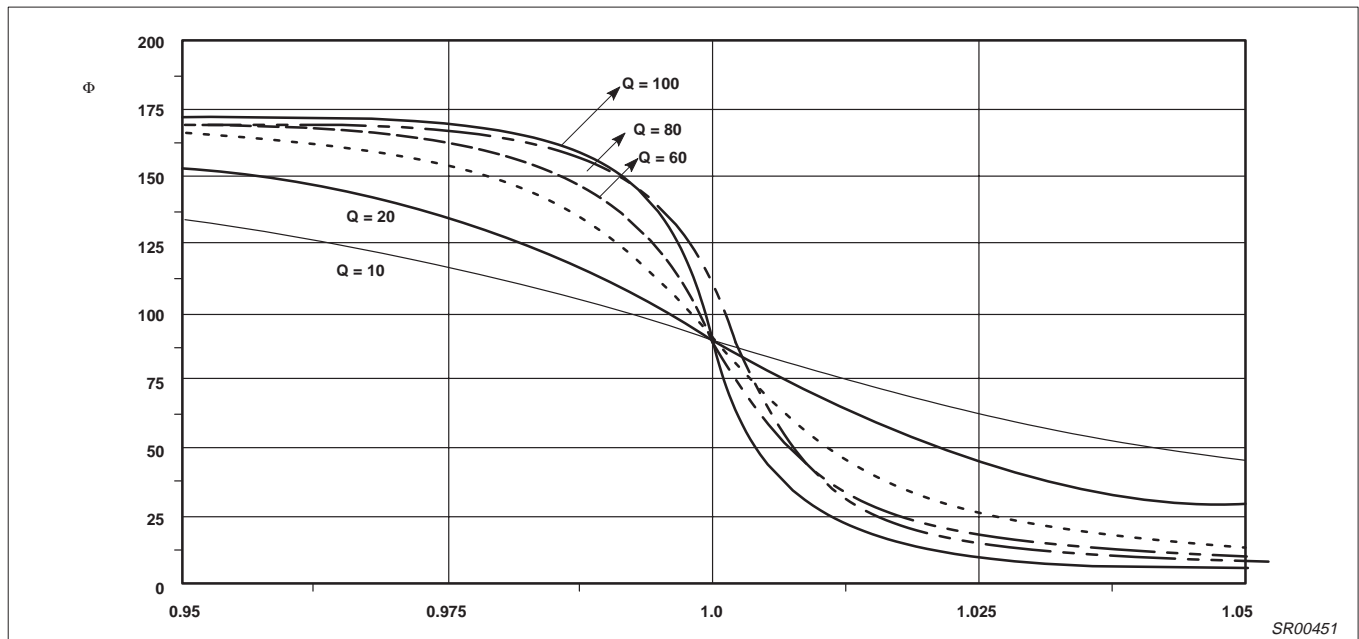


Figure 12. Phase vs Normalized IF Frequency  $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

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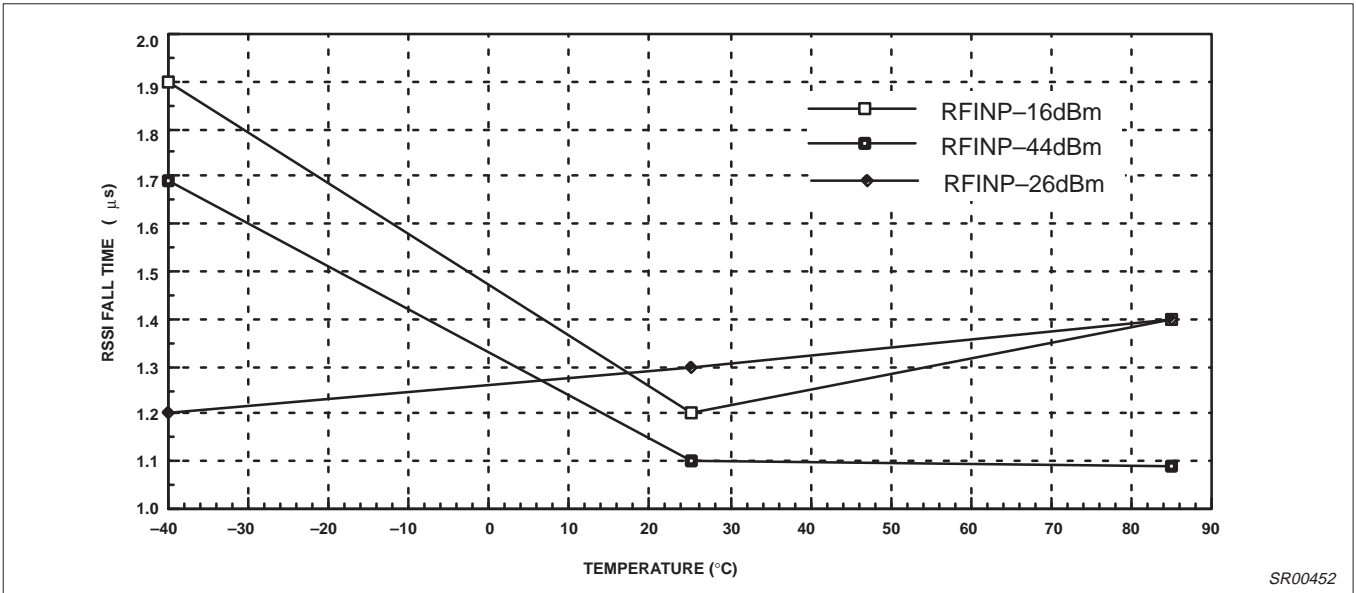


Figure 13. SA624 Rise Time 455kHz IF Frequency

SR00452

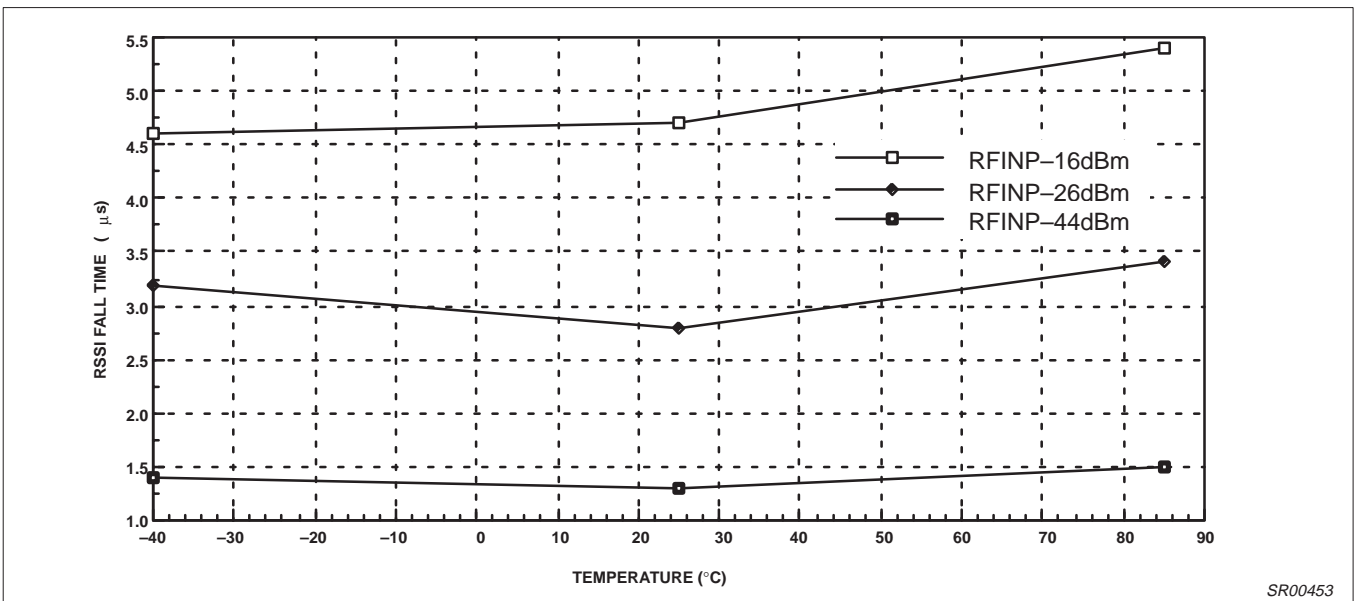


Figure 14. SA624 Fall Time 455kHz IF Frequency

SR00453

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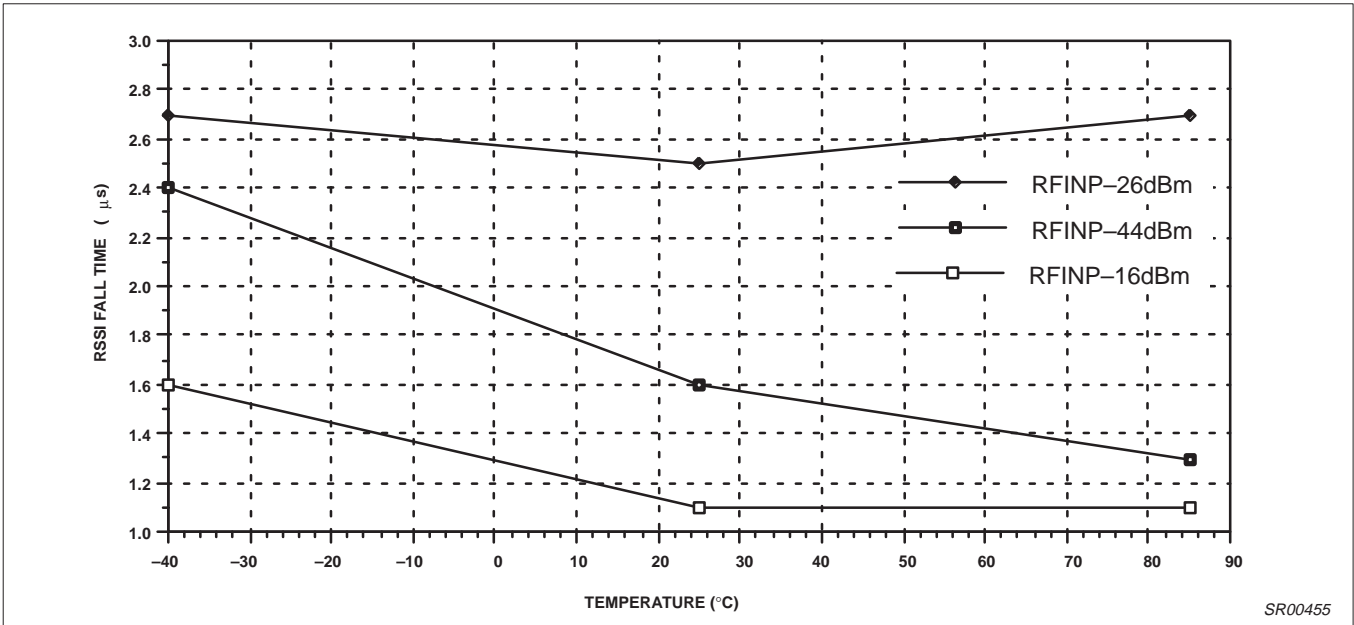


Figure 15. SA624 Rise Time 10.7MHz IF Frequency

SR00455

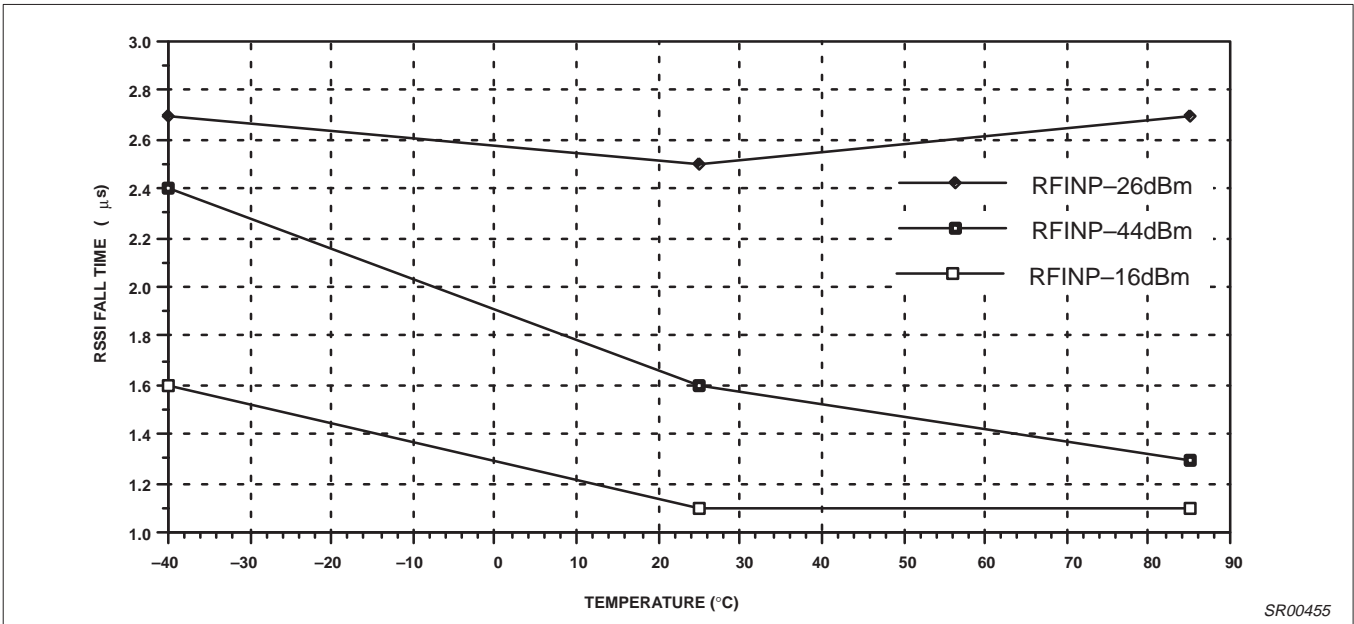


Figure 16. SA624 Fall Time 10.7MHz IF Frequency

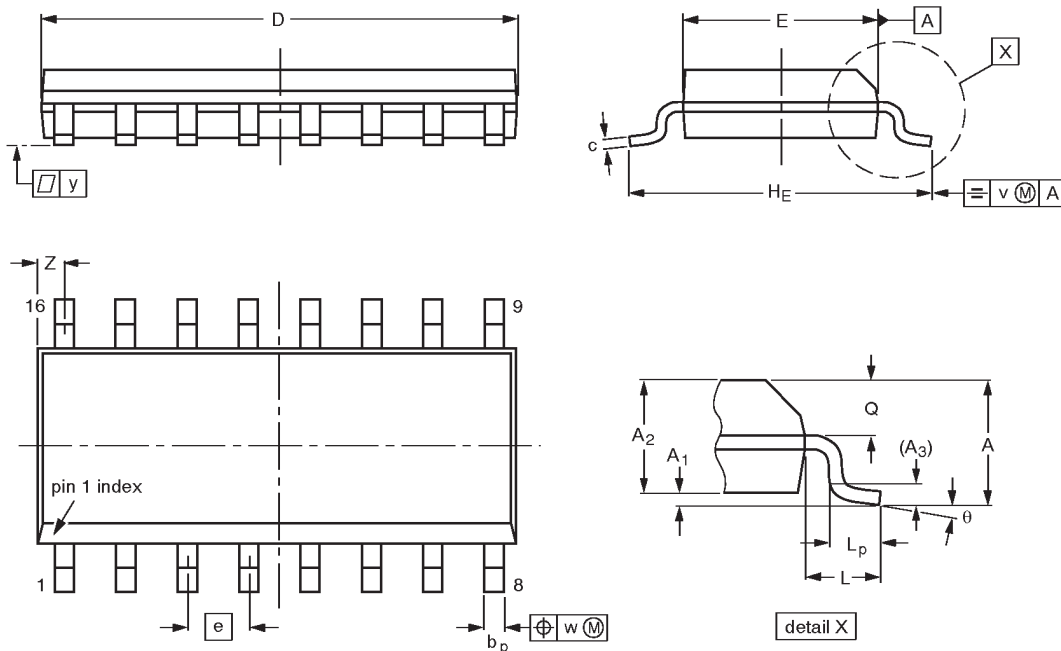
SR00455

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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