



CMOS Analog Switches

FEATURES

- Analog Signal Range: $\pm 15\text{ V}$
- Fast Switching— t_{ON} : 150 ns
- Low On-Resistance— $r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Latch-up Proof
- CMOS Compatible

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

DESCRIPTION

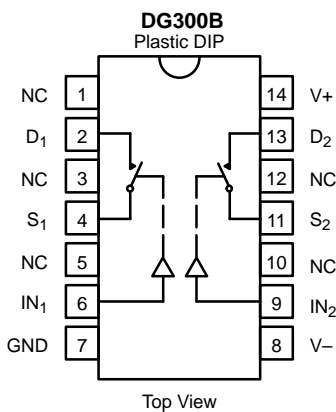
The DG300B-DG303B family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

Designed on the Vishay Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V- rail to 0 V.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



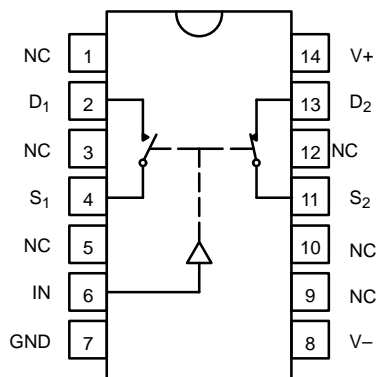
| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" $\leq 0.8\text{ V}$
 Logic "1" $\geq 4\text{ V}$

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG301B

Plastic DIP



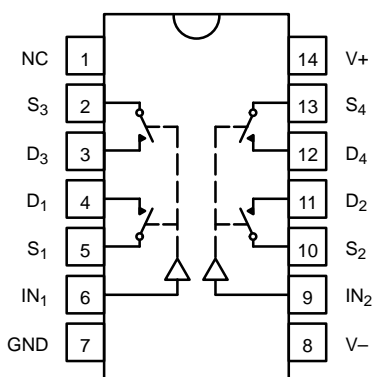
Top View

| TRUTH TABLE | | |
|-------------|-----------------|-----------------|
| Logic | SW ₁ | SW ₂ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

DG302B

Plastic DIP



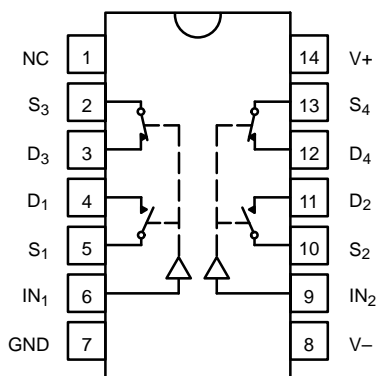
Top View

| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

DG303B

Plastic DIP and SOIC



Top View

| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| Logic | SW ₁ , SW ₂ | SW ₃ , SW ₄ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V



| ORDERING INFORMATION | | |
|----------------------|--------------------|-------------|
| Temp Range | Package | Part Number |
| DG300B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG300BDJ |
| DG301B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG301BDJ |
| DG302B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG302BDJ |
| DG303B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG303BDJ |
| | 14-SOIC | DG303BDY |

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
 V+ 44 V
 GND 25 V
 Digital Inputs^{NO TAG}, V_S, V_D (V-) -2 V to (V+) +2V or 30 mA, whichever occurs first
 Current, Any Terminal 30 mA
 Continuous Current, S or D
 (Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature -65 to 150°C
 Power Dissipation^{NO TAG}
 14-Pin Plastic DIP^{NO TAG} 470 mW
 SOIC-14^d 600 mW

Notes:

- a. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 25°C
- d. Derate 7.6 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

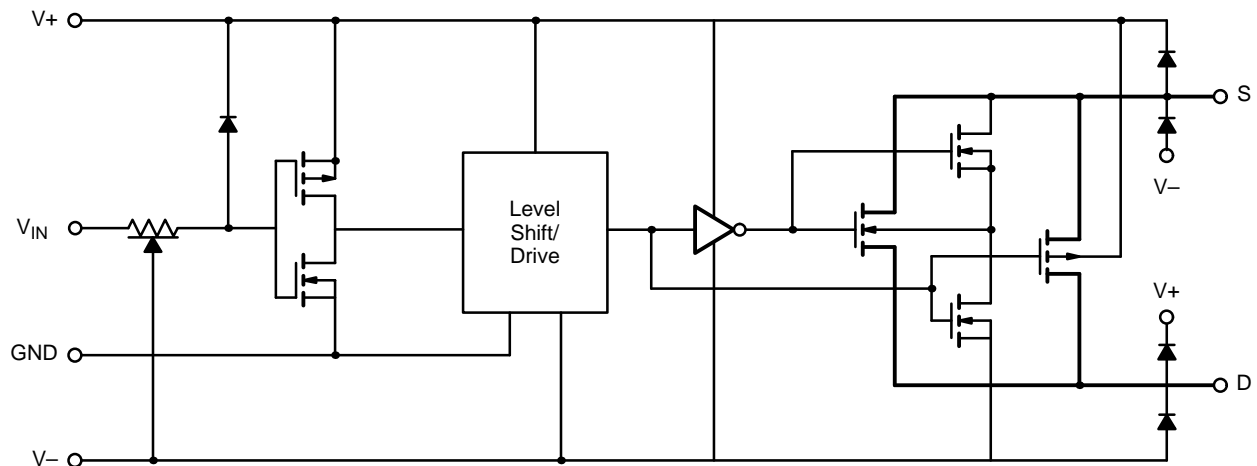


FIGURE 1.

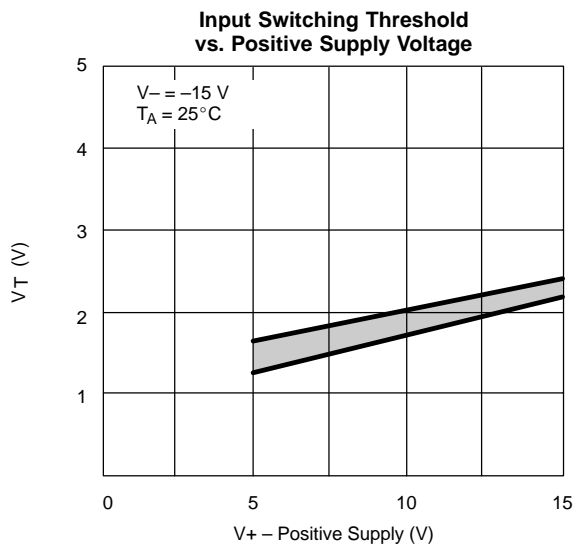
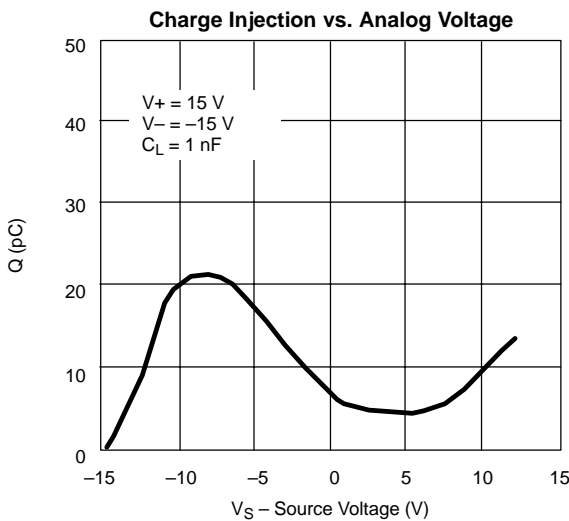
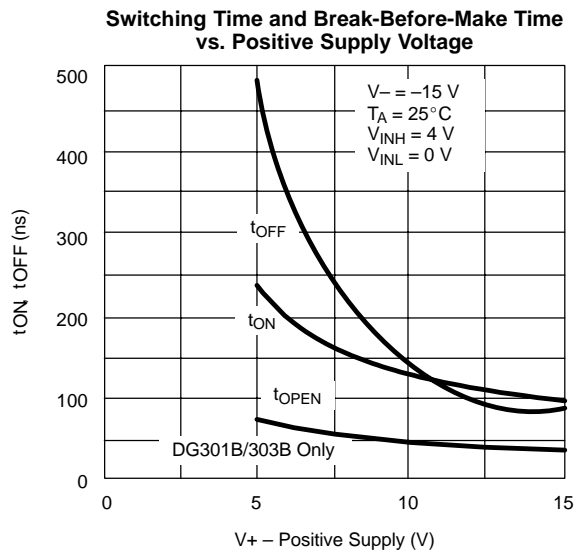
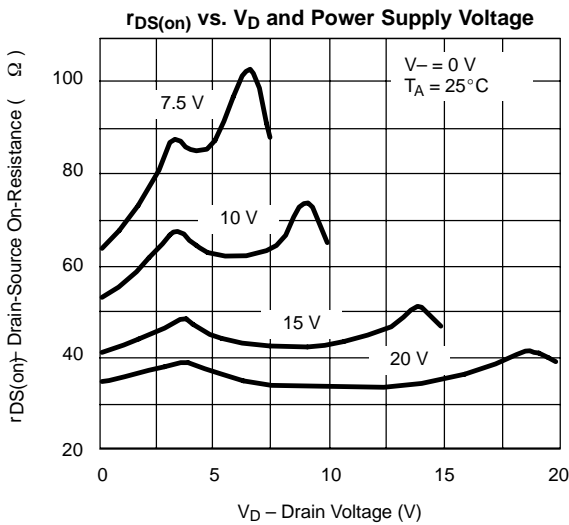
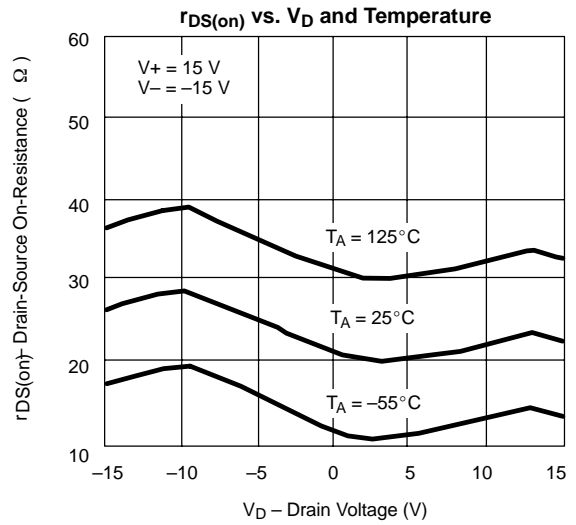
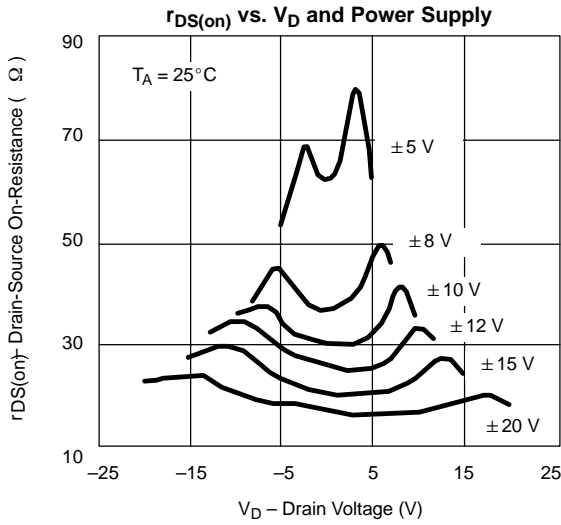
| SPECIFICATIONS ^a | | | | | | | |
|---------------------------------------|--------------|--|--------------------|-----------------------|------------------|------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 0.8\text{ V}$ or $V_{IN} = 4\text{ V}^f$ | Temp ^b | Limits -40 to 85°C | | | Unit |
| | | | | Min ^d | Typ ^c | Max ^d | |
| Analog Switch | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | -15 | | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ | Room Full | | 30 | 50 75 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S = \pm 14\text{ V}$, $V_D = \mp 14\text{ V}$ | Room Hot | -5 -100 | ± 0.1 | 5 100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | | Room Hot | -5 -100 | ± 0.1 | 5 100 | |
| Drain On Leakage Current | $I_{D(on)}$ | | Room Hot | -5 -100 | ± 0.1 | 5 100 | |
| Digital Control | | | | | | | |
| Input Current with Input Voltage High | I_{INH} | $V_{IN} = 5\text{ V}$ | Room Full | -1 | -0.001 | | μA |
| | | $V_{IN} = 15\text{ V}$ | Room Full | | 0.001 | 1 | |
| Input Current with Input Voltage Low | I_{INL} | $V_{IN} = 0\text{ V}$ | Room Full | -1 | -0.001 | | |
| Dynamic Characteristics | | | | | | | |
| Turn-On Time | t_{ON} | See Figure NO TAG | Room | | 150 | | ns |
| Turn-Off Time | t_{OFF} | | Room | | 130 | | |
| Break-Before-Make Time | t_{OPEN} | DG301B/303B Only Figure NO TAG | Room | | 50 | | |
| Charge Injection | Q | $C_L = 1\text{ nF}$, $R_{gen} = 0\ \Omega$ $V_{gen} = 0\text{ V}$, Figure NO TAG | Room | | 8 | | pC |
| Source-Off Capacitance | $C_{S(off)}$ | V_S , $V_D = 0\text{ V}$, $f = 1\text{ MHz}$ | Room | | 14 | | pF |
| Drain-Off Capacitance | $C_{D(off)}$ | | Room | | 14 | | |
| Channel-On Capacitance | $C_{D(on)}$ | | Room | | 40 | | |
| Input Capacitance | C_{in} | | $f = 1\text{ MHz}$ | Room | | 6 | |
| Off-Isolation | OIRR | $V_{IN} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$ $V_S = 1\text{ V}_{rms}$, $f = 500\text{ kHz}$ | Room | | 62 | | dB |
| Crosstalk (Channel-to-Channel) | X_TALK | | Room | | 74 | | |
| Power Supplies | | | | | | | |
| Positive Supply Current | I_+ | $V_{IN} = 4\text{ V}$ (One Input) All Others = 0 V | Room Full | | 0.23 | 1 | mA |
| Negative Supply Current | I_- | | Room Full | -100 | -0.001 | | |
| Positive Supply Current | I_+ | $V_{IN} = 0.8\text{ V}$ (All Inputs) | Room Full | | 0.001 | 100 | μA |
| Negative Supply Current | I_- | | Room Full | -100 | -0.001 | | |

Notes:

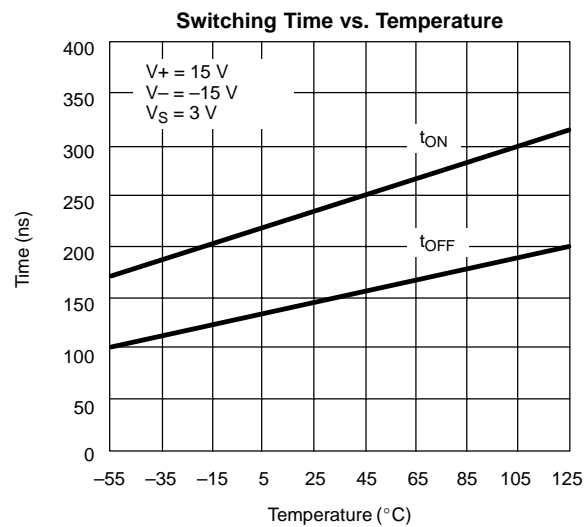
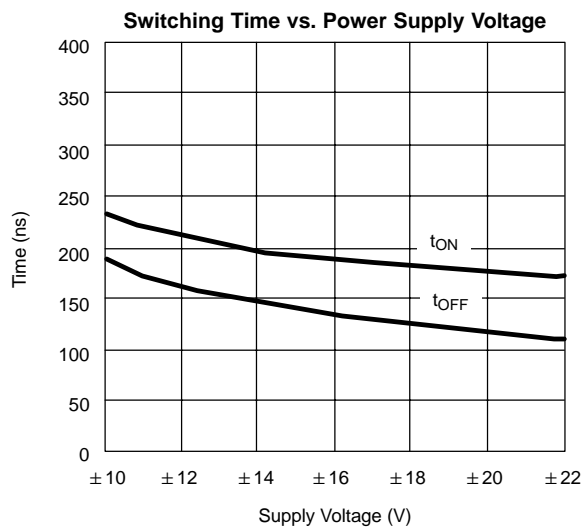
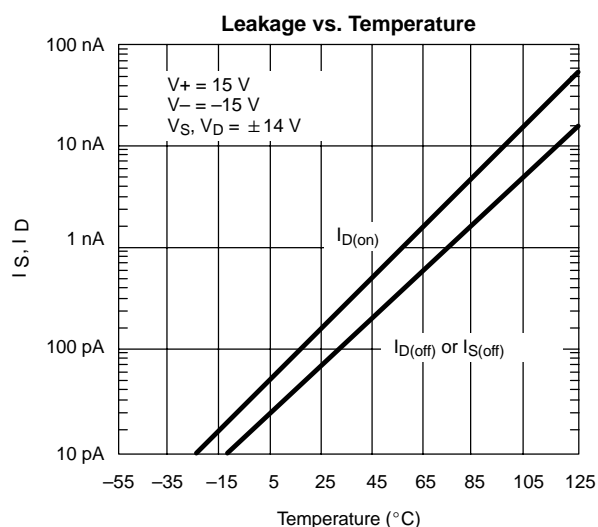
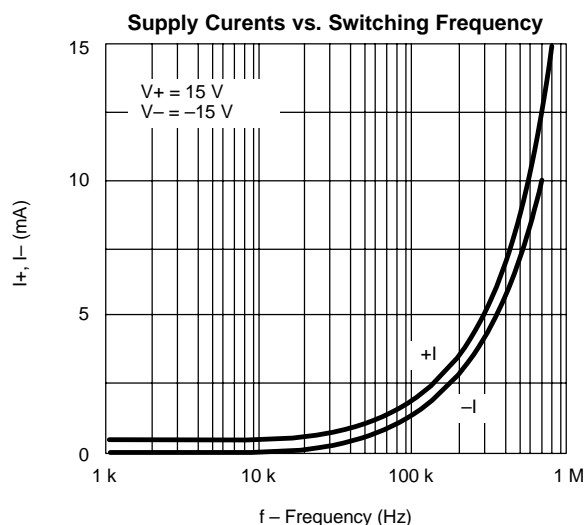
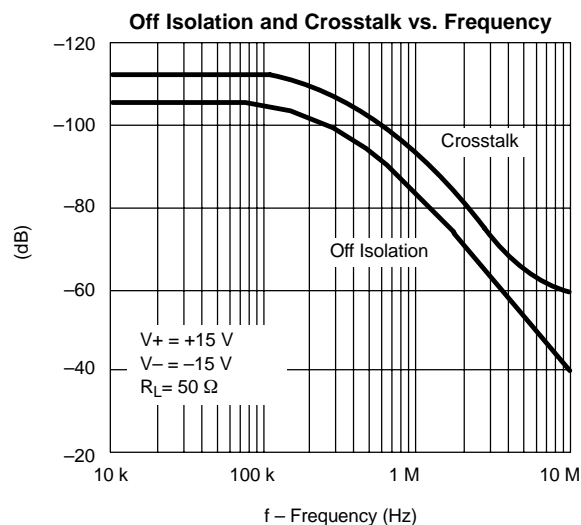
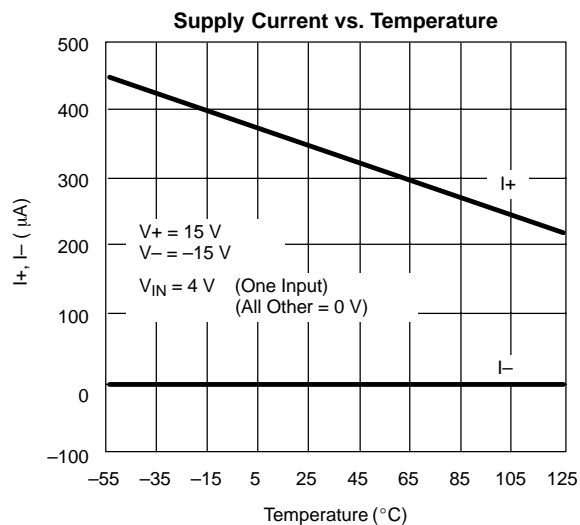
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS

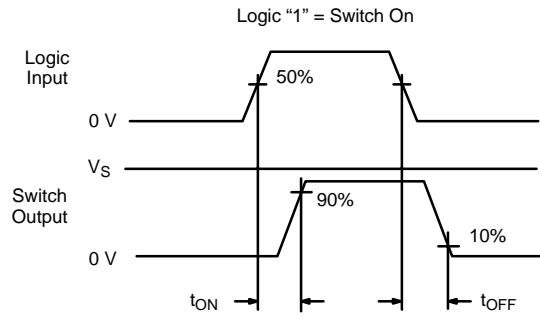
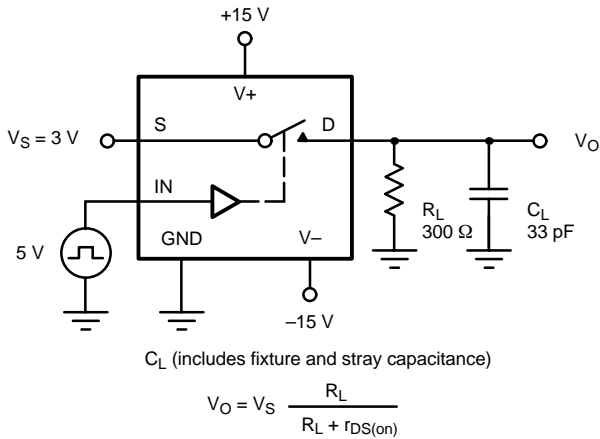


FIGURE 2. Switching Time

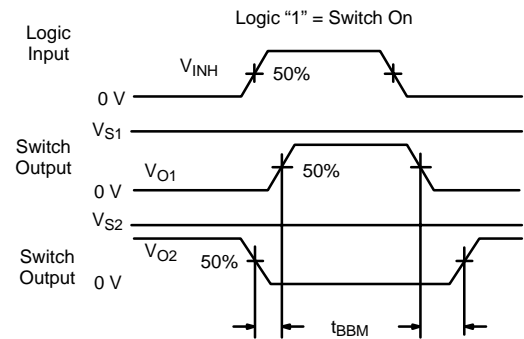
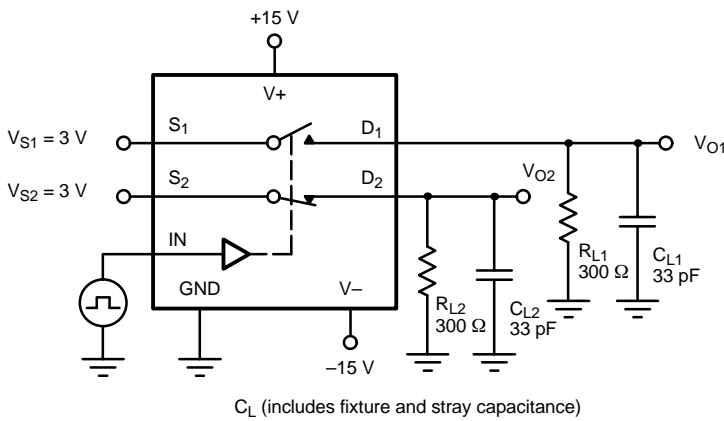


FIGURE 3. Break-Before-Make SPDT (DG301B, DG303B)

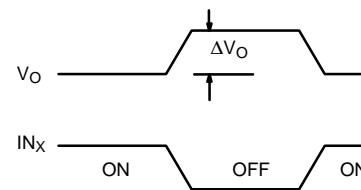
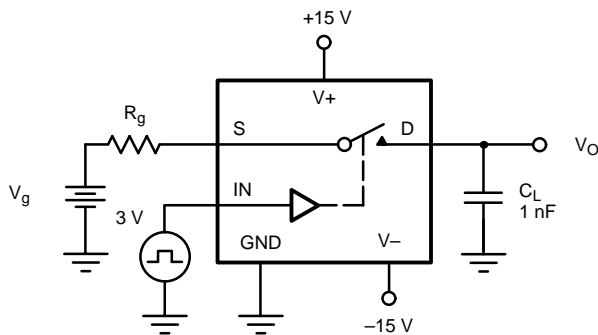


FIGURE 4. Charge Injection

| APPLICATION HINTS NO TAG | | | | |
|--------------------------------|--------------------------------|-----------------|--|---|
| V+ Positive Supply Voltage (V) | V- Negative Supply Voltage (V) | GND Voltage (V) | V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V) | V _S or V _D Analog Voltage Range (V) |
| 15 | -15 | 0 | 4/0.8 | -15 to 15 |
| 20 | -20 | 0 | 4/0.8 | -20 to 20 |
| 15 | 0 | 0 | 4/0.8 | 0 to 15 |

Note:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

The DG300B series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are:

1) Increased $r_{DS(on)}$; 2) slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V. (See Input Switching Threshold vs. Positive Supply Voltage Curve.)

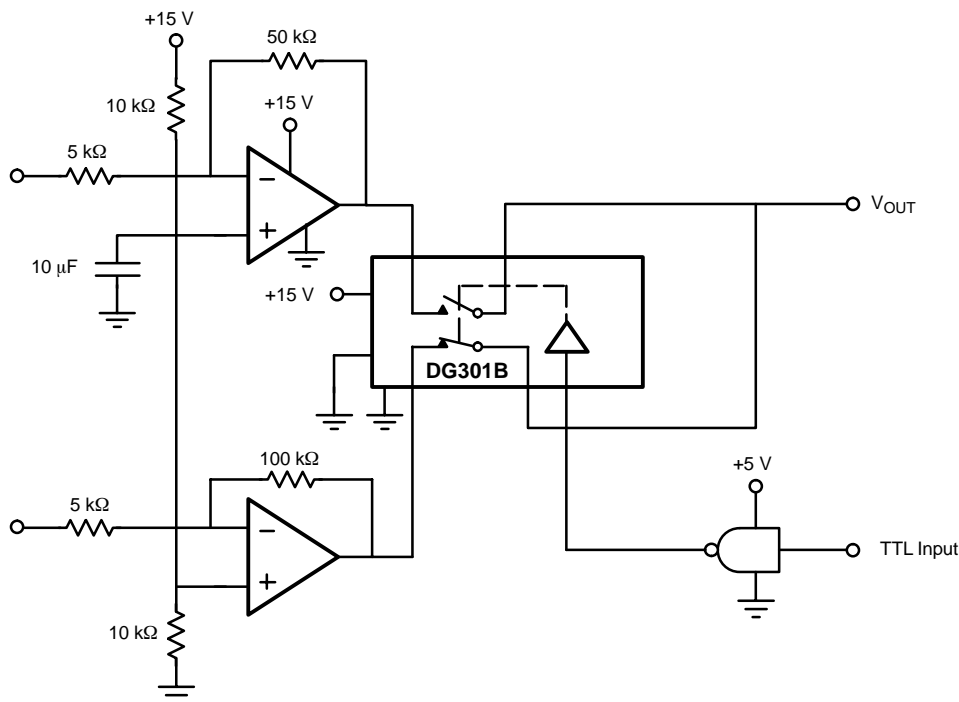


FIGURE 5. Single Supply Op Amp Switching

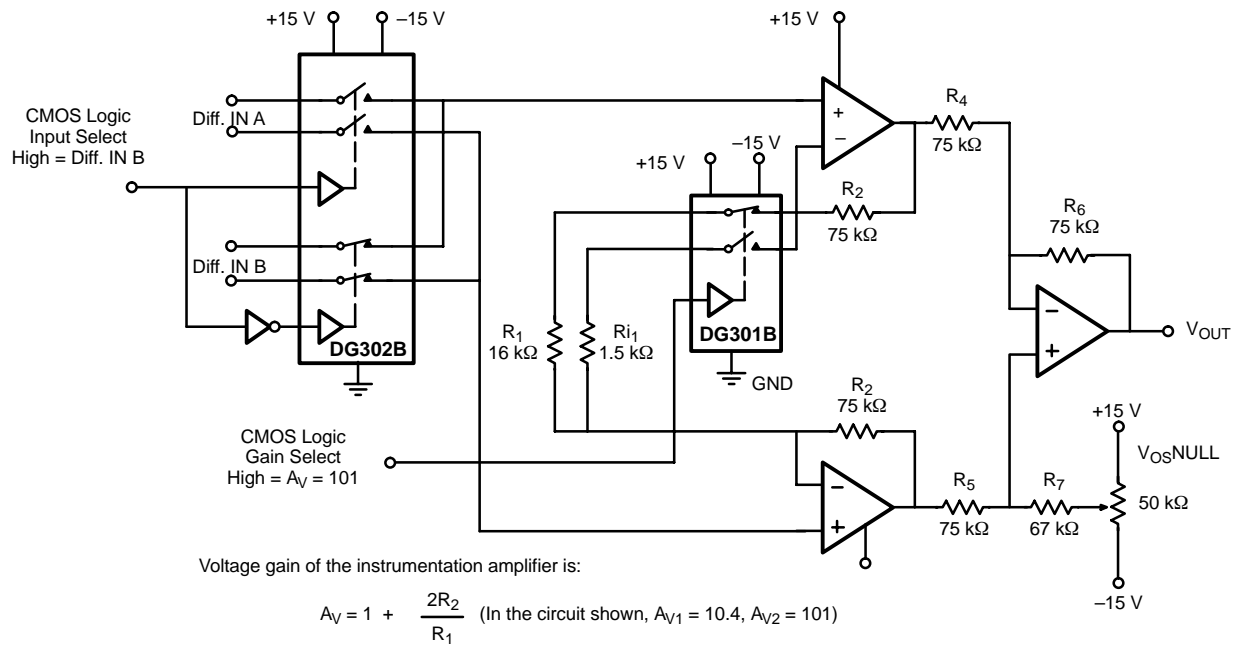


FIGURE 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain



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