DS87C520/DS83C520
EPROM/ROM High-Speed Microcontrollers

www.maxim-ic.com

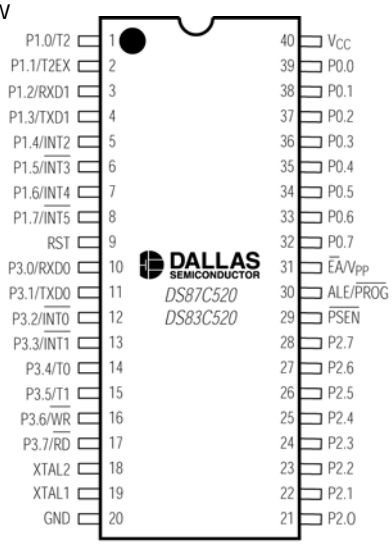
FEATURES

- **80C52 Compatible**
- **Large On-Chip Memory**
- **ROMSIZE Feature**
- **High-Speed Architecture**
- **Power Management Mode**
- **EMI Reduction Mode Disables ALE**
- **Two Full-Duplex Hardware Serial Ports**
- **High Integration Controller Includes**
- **13 Interrupt Sources with Six External**
- **Available in 40-pin PDIP, 44-Pin PLCC, 44-Pin TQFP, and 40-Pin Windowed CERDIP**
- **Factory Mask DS83C520 or EPROM (OTP) DS87C520**

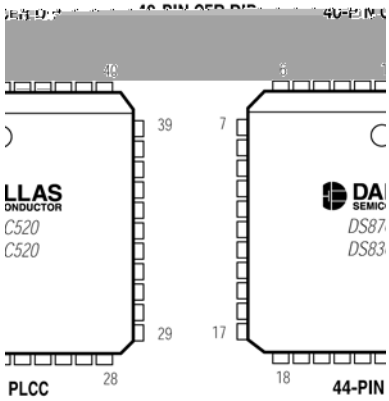
*The **High-Speed Microcontroller User's Guide** must be used in conjunction with this data sheet. Download it at: **www.maxim-ic.com/microcontrollers**.*

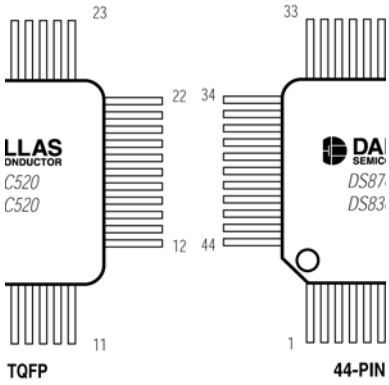
PIN CONFIGURATIONS

TOP VIEW



40-PIN PDIP





Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

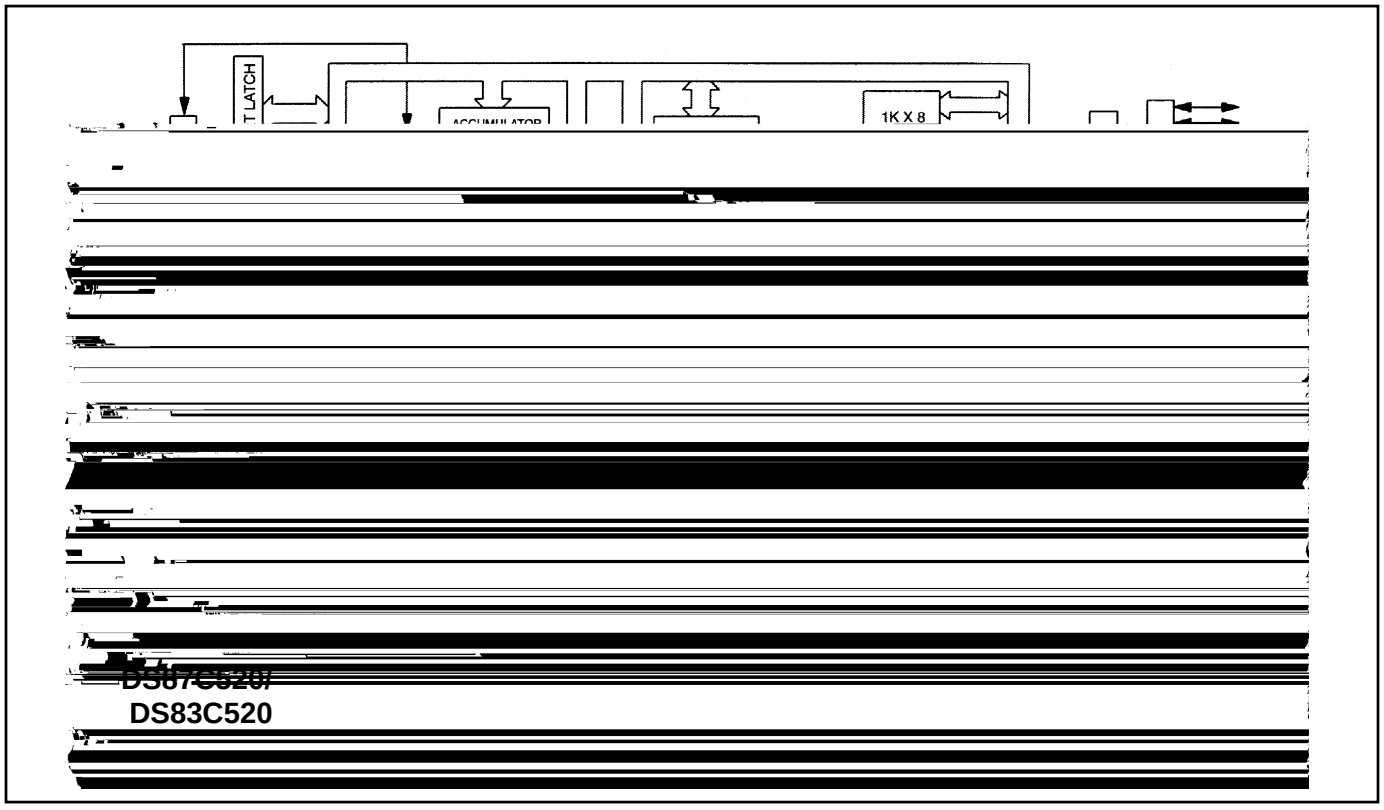
ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS87C520	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
DS83C520	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		
	° °		

Denotes a Pb-free/RoHS-compliant device.
The windowed ceramic DIP package is intrinsically Pb free.

DESCRIPTION

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
				Positive Supply Voltage.
				Digital Circuit Ground
				Reset Input.
				Crystal Oscillator Pins.
			$\overline{\text{PSEN}}$	**Program Store-Enable Output.** $\overline{\text{PSEN}}$

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
				Address Latch Enable Output
				Port 0 (AD0–7), I/O

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
				Port 2 (A8–15), I/O
				Port 3, I/O. $\overline{RD}$ $\overline{WR}$

COMPATIBILITY

PERFORMANCE OVERVIEW

INSTRUCTION SET SUMMARY

High-Speed Microcontroller User's Guide

High-Speed Microcontroller User's Guide

SPECIAL FUNCTION REGISTERS

High-Speed Microcontroller User's Guide

Table 1. Special Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
DPL1									
DPH1									
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	
		SMOD0							
		$\overline{T}$				$\overline{T}$			
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	
ROMSIZE						**RMS2**	**RMS1**	**RMS0**	
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	
TA									
							$\overline{T2}$	$\overline{RL2}$	
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	
EIE				**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	
EIP				**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	

Note: *New functions are in bold.*

MEMORY RESOURCES

OPERATIONAL CONSIDERATION

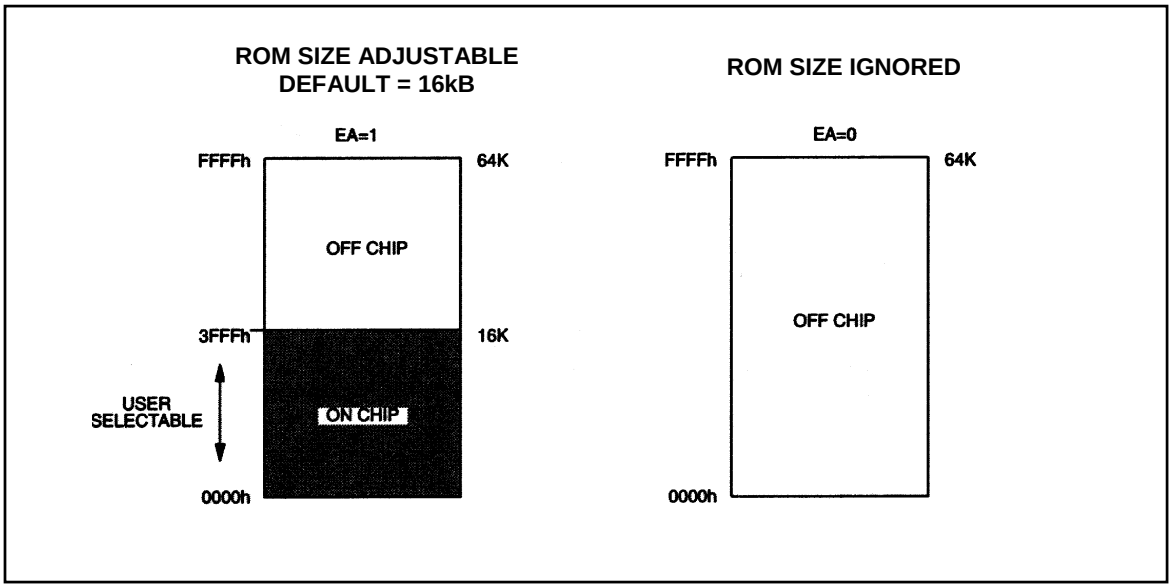
PROGRAM MEMORY ACCESS

RMS2	RMS1	RMS0	MAXIMUM ON-CHIP ROM ADDRESS

$\overline{EA}$ $\overline{EA}$

$\overline{PSEN}$

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Electrical Specifications

Table 3. Data Memory Cycle Stretch Values

CKCON.2-0			MEMORY CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME at 33MHz (ns)
M2	M1	M0			

DUAL DATA POINTER

POWER MANAGEMENT

POWER MANAGEMENT MODE (PMM)

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)

CRYSTAL-LESS PMM

PMM OPERATION

Clock Divider

CD1	CD0	CYCLE RATE

Switchback

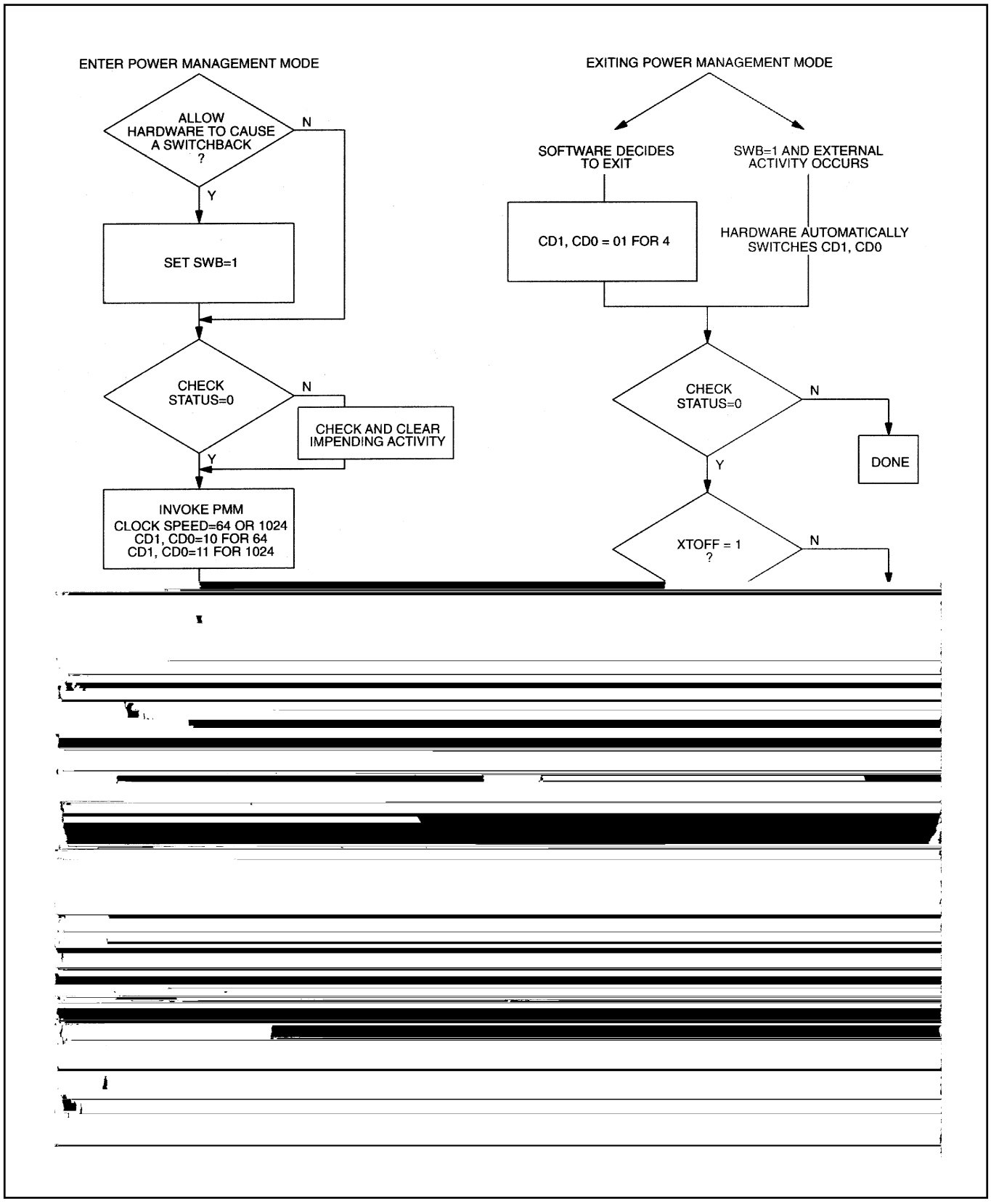
Status

Crystal/Ring Operation

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
$\overline{RG}$		$\overline{RG}$ $\overline{RG}$		
				$\overline{RG}$
		.		

Figure 3. Invoking and Clearing PMM



IDLE MODE

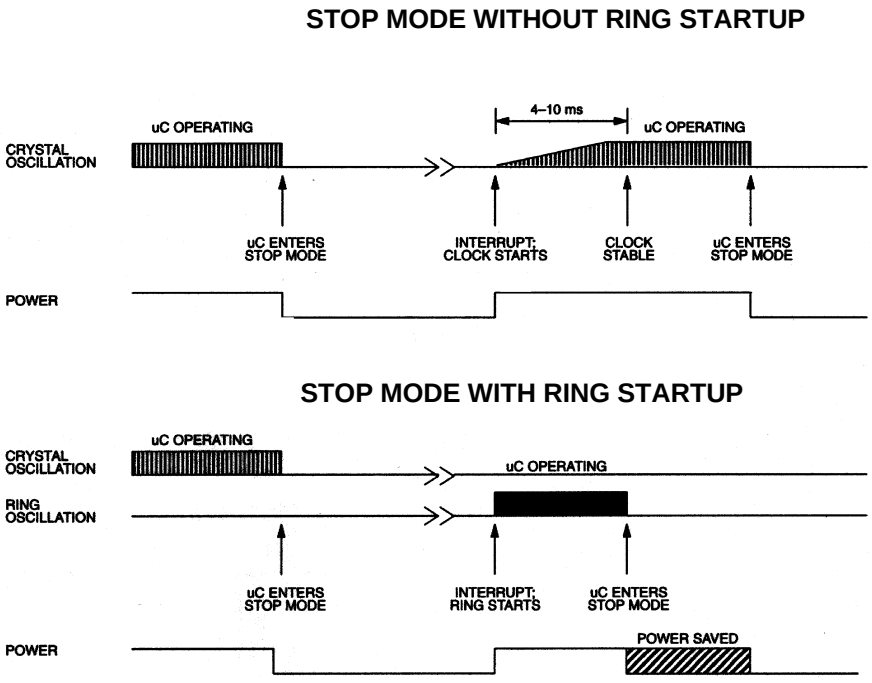
STOP MODE ENHANCEMENTS

μ

μ

μ

Figure 4. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

PERIPHERAL OVERVIEW

High-Speed Microcontroller User's Guide

SERIAL PORTS

TIMER RATE CONTROL

POWER-FAIL RESET

POWER-FAIL INTERRUPT

WATCHDOG TIMER

Table 7. Watchdog Timeout Values

WD1	WD2	INTERRUPT TIMEOUT	TIME (33 MHz)	RESET TIMEOUT	TIME (33 MHz)

INTERRUPTS

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
____				
____				
____				
____				

TIMED-ACCESS PROTECTION

EPROM PROGRAMMING

PROGRAMMING PROCEDURE

Electrical Specifications

Table 9. EPROM Programming Modes

MODE		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7

Table 10. DS87C520 EPROM Lock Bits

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
				$\overline{EA}$

SECURITY OPTIONS

Lock Bits

Memory

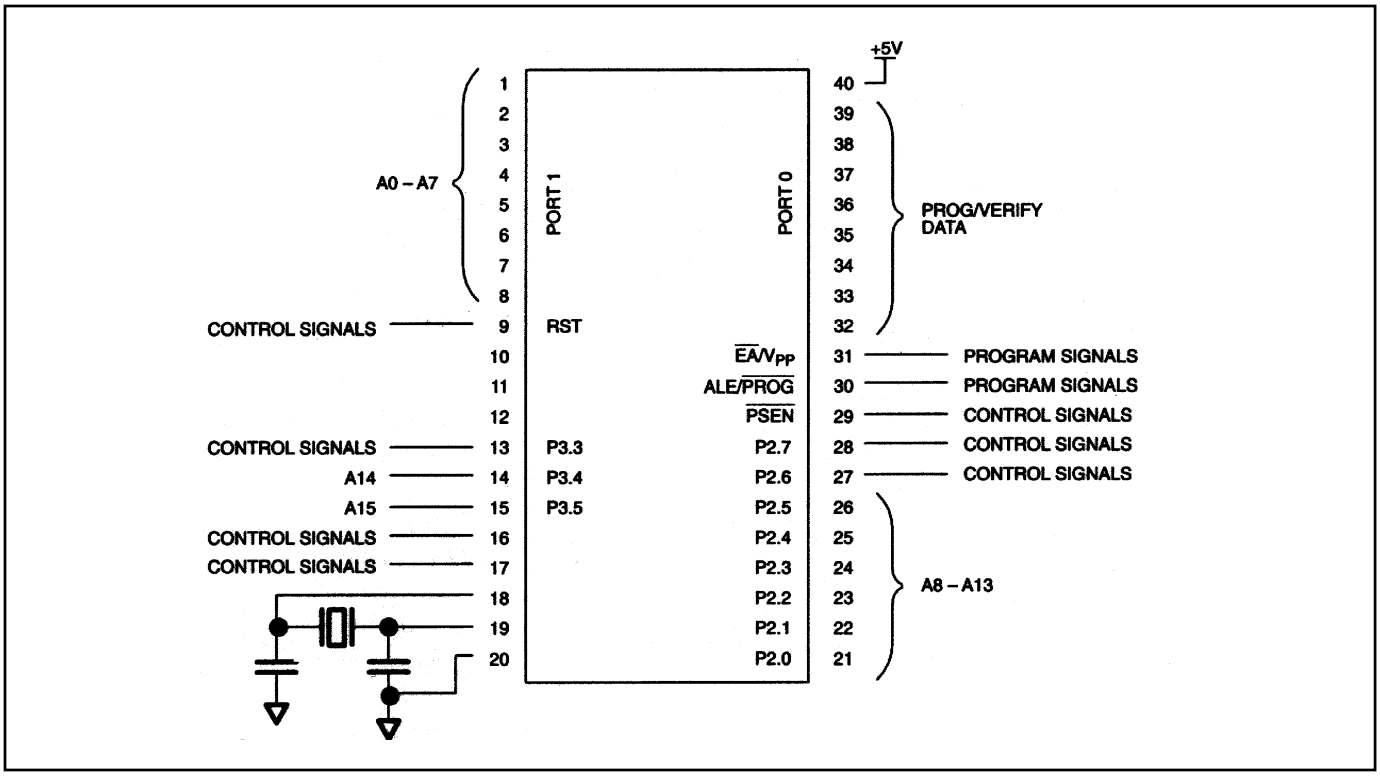
Encryption Array

OTHER EPROM OPTIONS

SIGNATURE

ADDRESS	VALUE	MEANING

Figure 5. EPROM Programming Configuration



ROM-SPECIFIC FEATURES

SECURITY OPTIONS

Lock Bits

—

Encryption Array

DS83C520 ROM VERIFICATION

DS83C520 SIGNATURE

ADDRESS	VALUE	MEANING

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
					µ	
					µ	
					µ	
					µ	
$\overline{PSEN}$						
$\overline{PSEN}$ µ						
$\overline{PSEN}$						
					µ	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
					µ	
$\overline{EA}$					µ	
					µ	
					Ω	

Note 1: All parameters apply to both commercial and industrial temperature operation, unless otherwise noted.

Note 2: All voltages are referenced to ground.

Note 3: Active current measured with 33MHz clock source on XTAL1, V_{CC} = RST = 5.5V, other pins disconnected.

Note 4: Idle mode current measured with 33MHz clock source on XTAL1, V_{CC} = 5.5V, RST at ground, other pins disconnected.

Note 5: Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.

Note 6: When addressing external memory. This specification only applies to the first clock cycle following the transition.

Note 7: RST = V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

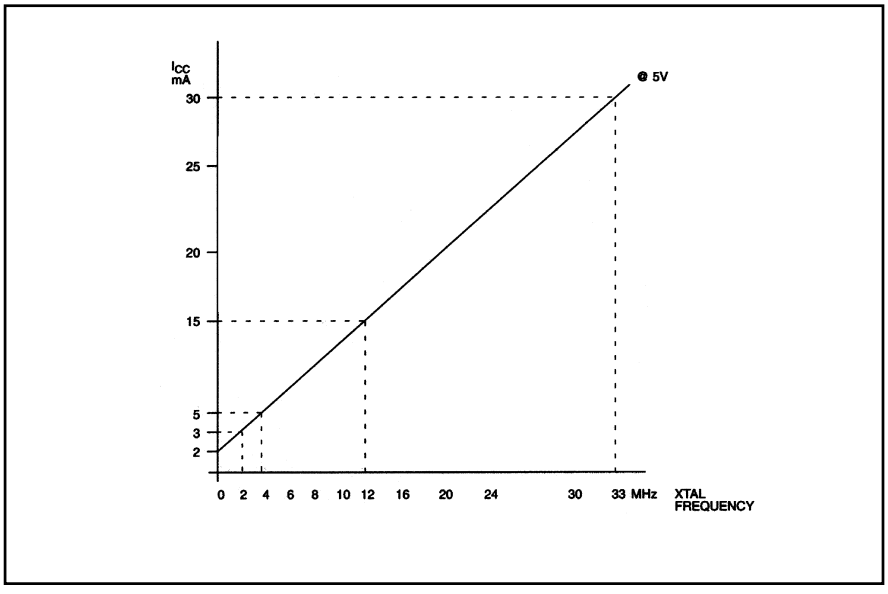
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

Note 10: 0.45 < V_{IN} < V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

Note 11: 0.45 < V_{IN} < V_{CC}. RST = V_{CC}. This condition mimics operation of pins in I/O mode.

Note 12: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

TYPICAL I_{CC} vs. FREQUENCY



AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
		MIN	MAX	MIN	MAX	

Note 1: All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics are not 100% tested, but are characterized and guaranteed by design. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
$\overline{RD}$					
$\overline{WR}$					
$\overline{RD}$					
$\overline{RD}$ $\overline{WR}$					

MOVX CHARACTERISTICS (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS

EXPLANATION OF AC SYMBOLS

$\overline{WR}$

$\overline{PSEN}$

$\overline{RD}$

POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES

Note 1: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox.

Note 2: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

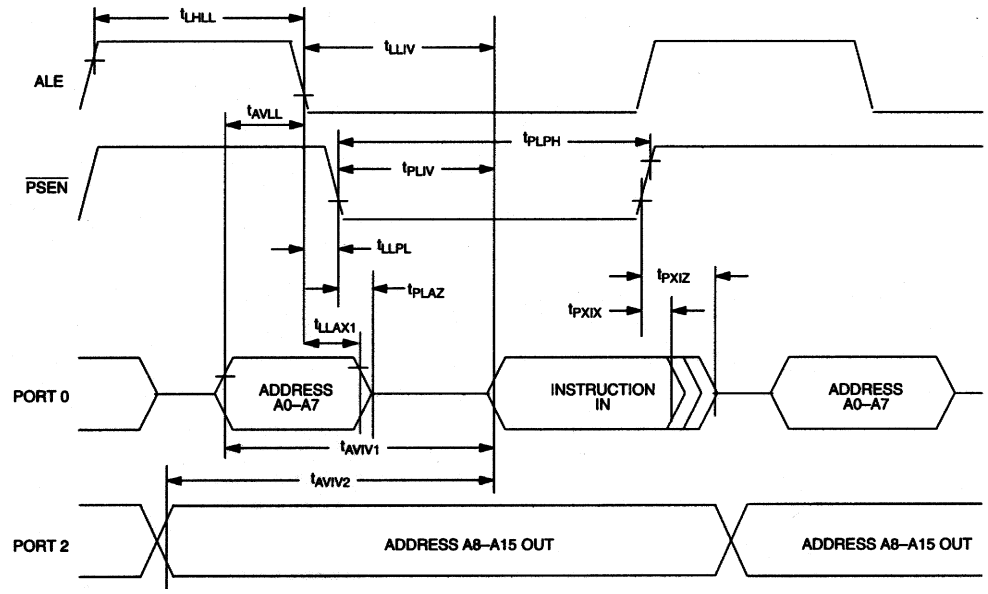
EPROM PROGRAMMING AND VERIFICATION

(V_{CC} = 4.5V to 5.5V, T_A = +21°C to +27°C.)

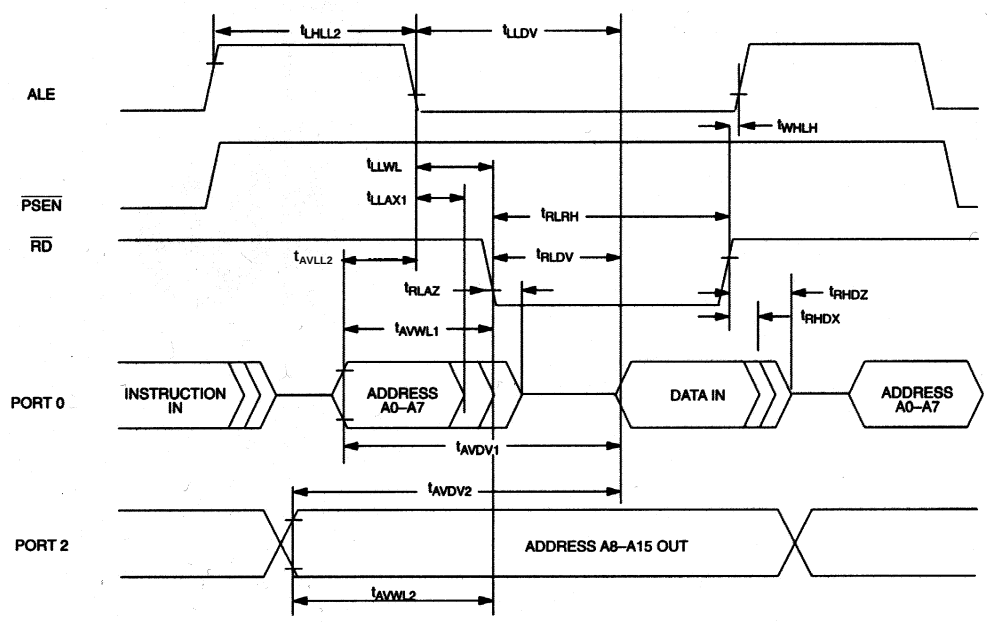
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
					µ	
					µ	
					µ	
					µ	

Note 1: All voltages are referenced to ground.

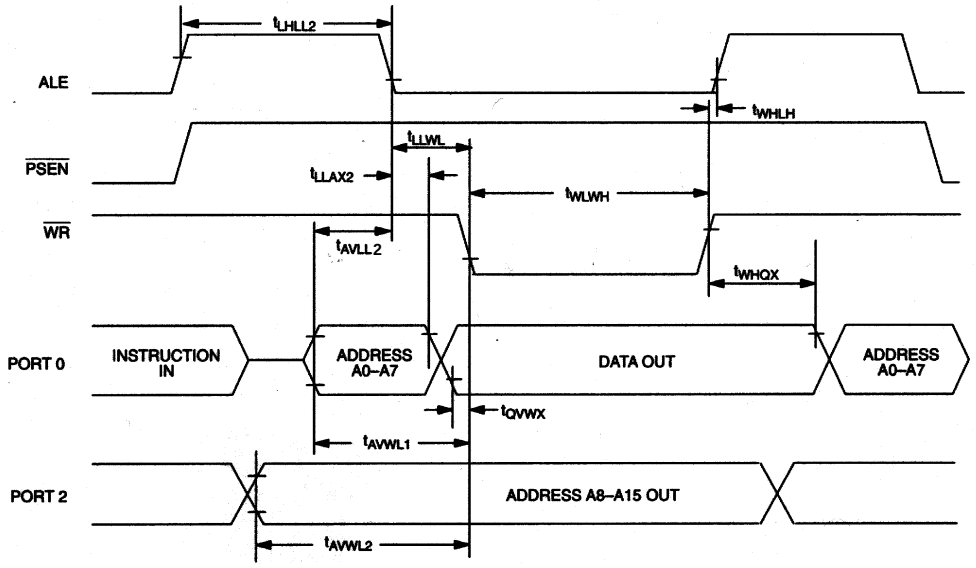
EXTERNAL PROGRAM MEMORY READ CYCLE



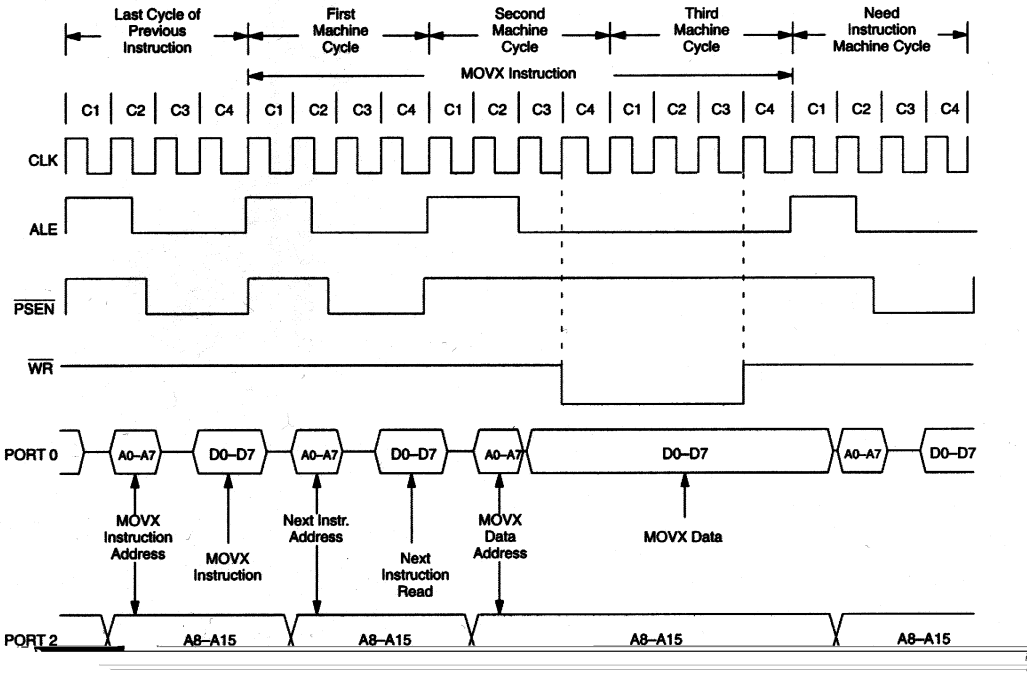
EXTERNAL DATA MEMORY READ CYCLE



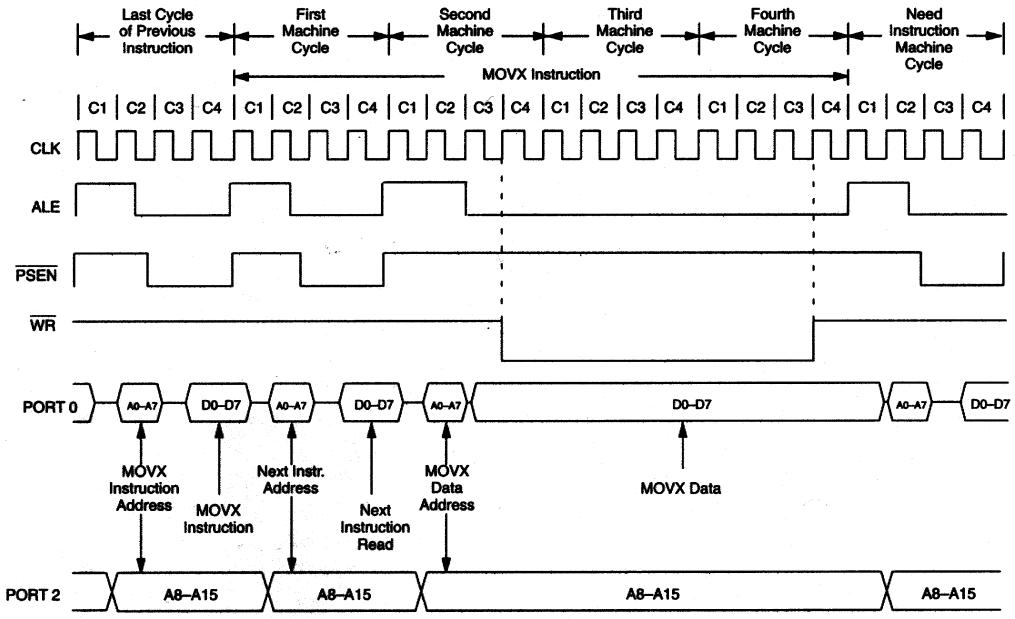
EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

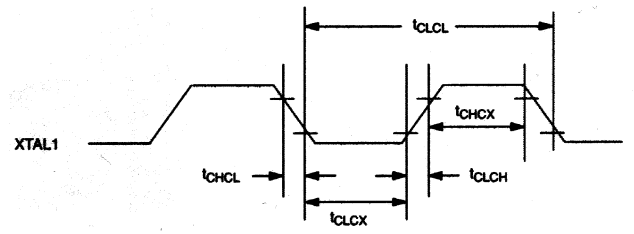


DATA MEMORY WRITE WITH STRETCH = 2

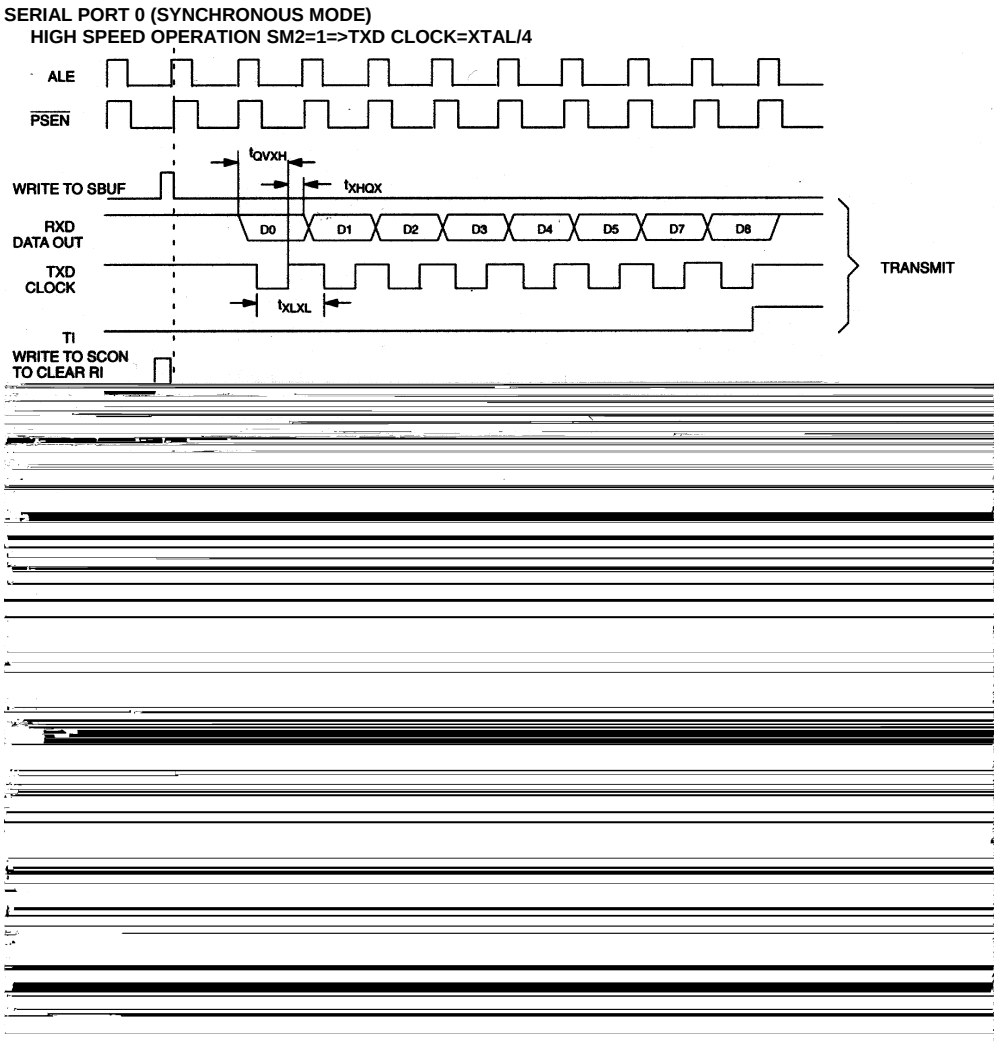


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

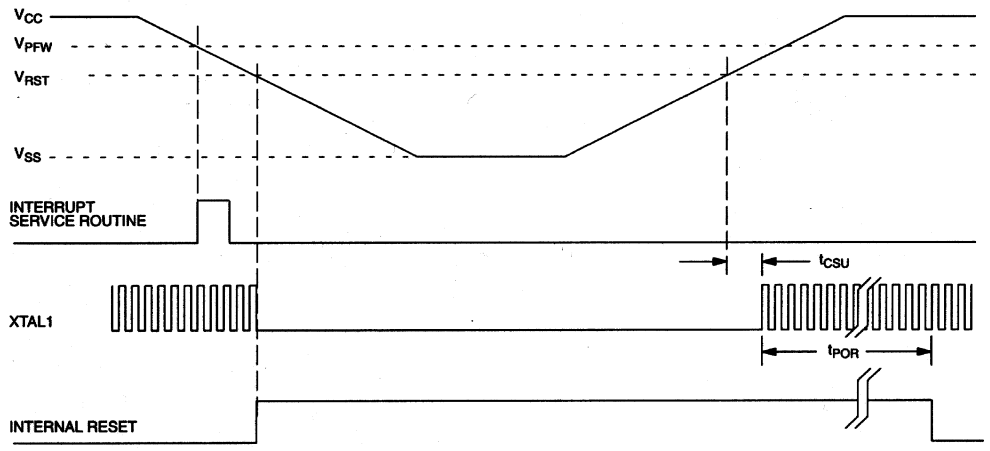
EXTERNAL CLOCK DRIVE



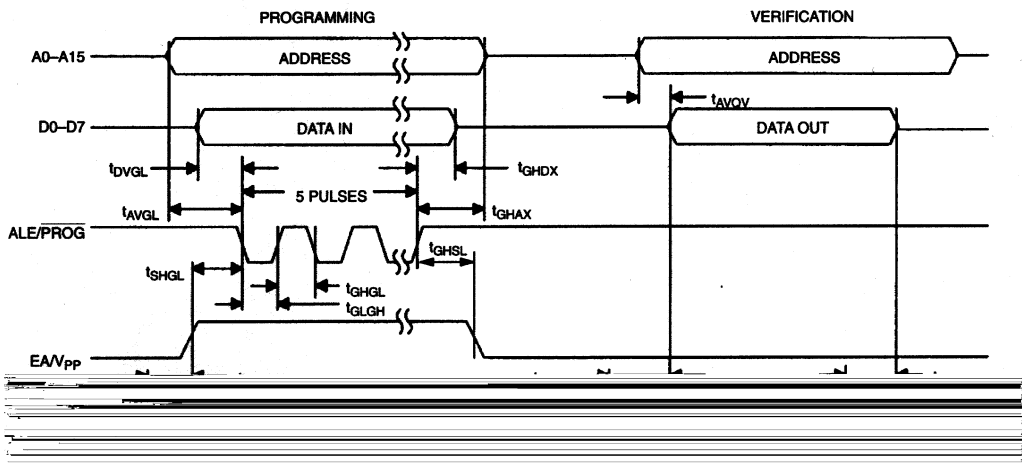
SERIAL PORT MODE 0 TIMING



POWER-CYCLE TIMING



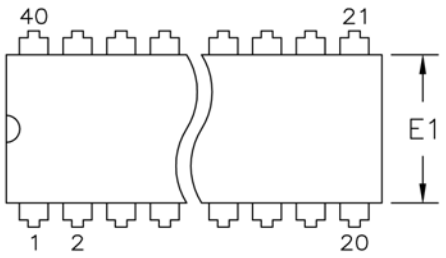
EPROM PROGRAMMING AND VERIFICATION WAVEFORMS

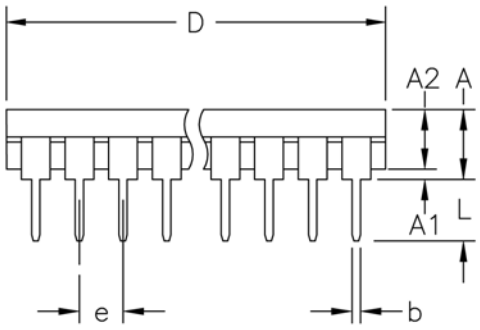


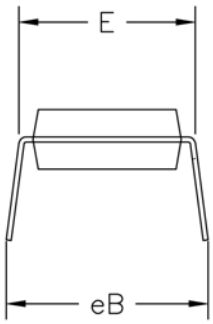
PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		







	40 PIN	
	MIN	MAX
A	–	0.200
A1	0.015	–
A2	0.140	0.160
b	0.014	0.022
c	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
e	0.090	0.110
L	0.115	0.145
eB	0.600	0.700

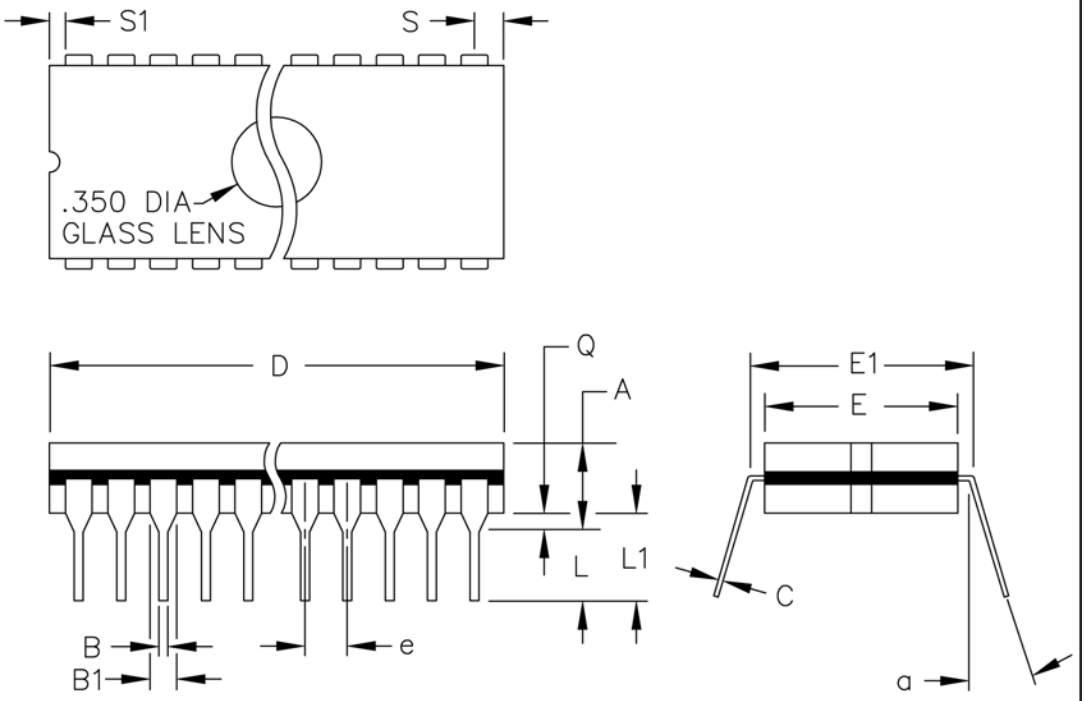
ALL DIMENSIONS ARE IN INCHES

SIGNATURE	DATE	DALLAS SEMICONDUCTOR MAXIM			
DOC. CONTROL:					
ENGR. MGR:		TITLE: MARKETING OUTLINE, 40 LEAD PLASTIC DUAL–IN–LINE PACKAGE (0.600")			
MFG. ENGR:					
CHECKED BY:					
DRAWN BY: R. RADKE	1/95	SIZE A	FSCM NO	PART NO. 56–G5000–000	REV A
DO NOT SCALE DWG.		SCALE N/A		SHEET 1 OF 1	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		



LTR	MIN	MAX
A	–	.225
B	.014	.023
B1	.038	.065
C	.006	.015
D	–	2.096
E	.510	.620
E1	.590	.630
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	–	.098
S1	.005	–
a	0°	15°

ALL DIMENSIONS SHOWN ARE IN INCHES.

SIGNATURE		DATE
DOC. CONTROL:		
ENGR. MGR:		
MFG. ENGR:		
CHECKED BY:		
DRAWN BY:	M.W.C.	5/94
DO NOT SCALE DWG.		

DALLAS SEMICONDUCTOR MAXIM

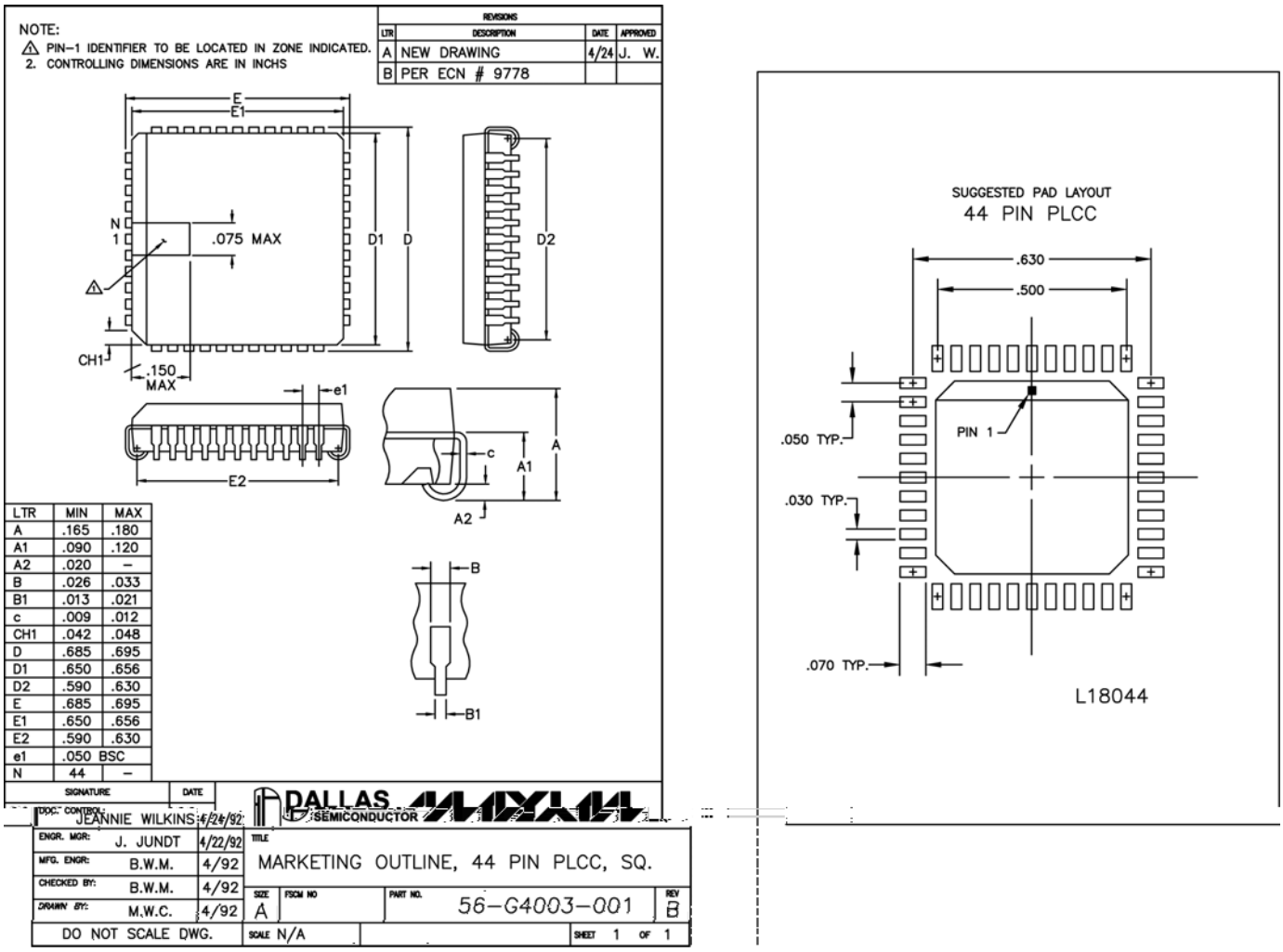
TITLE: MARKETING OUTLINE, 40-PIN CERAMIC DUAL-IN-LINE PACKAGE WITH GLASS LENS

SIZE	FSCM NO	PART NO.	REV
A		56-G4008-001	A

SCALE N/A | SHEET 1 OF 1

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



PACKAGE INFORMATION (continued)

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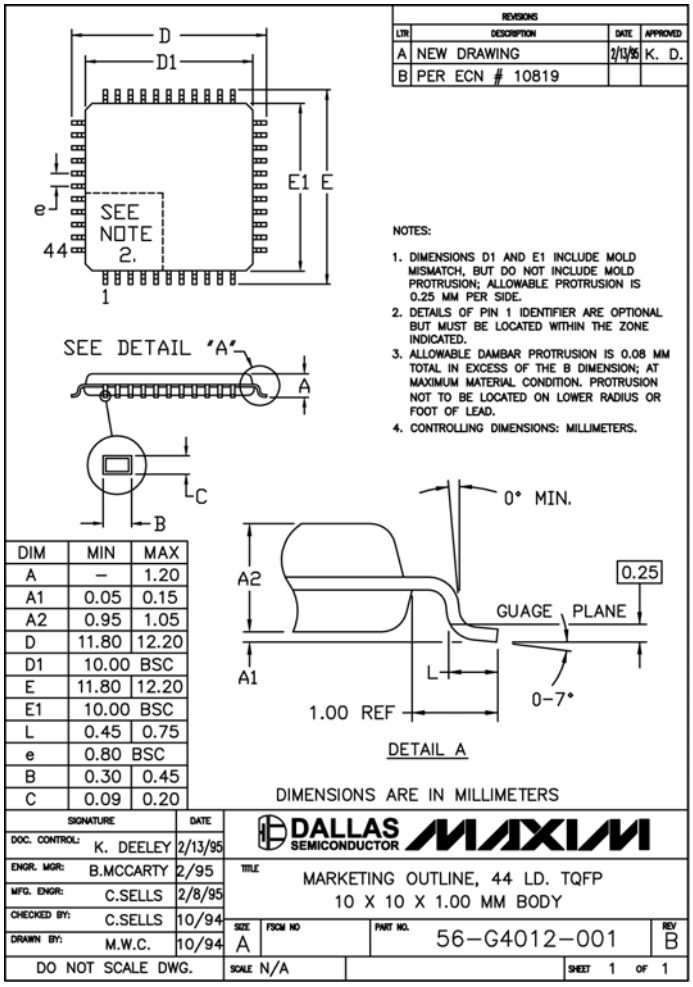

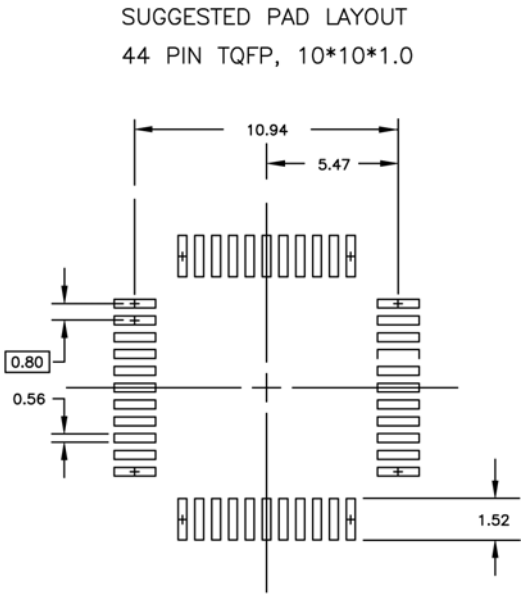

DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
	Ω Ω

° °

° °

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

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