

# HD146818

## RTC (Real Time Clock Plus RAM)

The HD146818 is a HMCS6800 peripheral CMOS device which combines three unique features: a complete time-of-day clock with alarm and one hundred calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of Low-power static RAM.

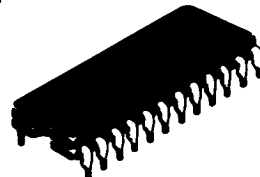
This device includes HD6801, HD6301 multiplexed bus interface circuit and 8085's multiplexed bus interface as well, so it can be directly connected to HD6801, HD6301 and 8085.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as battery powered CMOS part including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the HD146818 may be used with a CMOS microprocessor to relieve the software of timekeeping workload and to extend the available RAM of an MPU such as the HD6301.

### FEATURES

- Time-of-Day Clock and Calendar
  - Counts Seconds, Minutes, and Hours of the Day
  - Counts Days of Week, Date, Month, and Year
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24 Hour Clock with AM and PM in 12-Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced with Software as 64 RAM Locations
  - 14 Bytes of Clock and Control Register
  - 50 Bytes of General Purpose RAM
- Three Interrupt are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5 $\mu$ s to 500ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Three Time Base Input Options
  - 4.194304 MHz
  - 1.048576 MHz
  - 32.768 kHz
- Clock Output May be used as Microprocessor Clock Input
  - At Time Base Frequency  $\div 4$  or  $\div 1$
- Multiplexed Bus Interface Circuit of HD6801, HD6301 and 8085
- Low-Power, High-Speed, High-Density CMOS
- Battery Backed-up Operation
- Motorola MC146818 Compatible
- HD146818A in Development

HD146818P



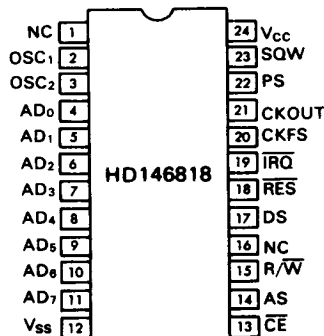
(DP-24)

HD146818FP



(FP-24)

### PIN ARRANGEMENT



(Top View)

### ABSOLUTE MAXIMUM RATINGS

| Item                  | Symbol            | Value       | Unit |
|-----------------------|-------------------|-------------|------|
| Supply Voltage        | V <sub>CC</sub> * | -0.3 ~ +7.0 | V    |
| Input Voltage         | V <sub>in</sub> * | -0.3 ~ +7.0 | V    |
| Operating Temperature | T <sub>opr</sub>  | 0 ~ +70     | °C   |
| Storage Temperature   | T <sub>stg</sub>  | -55 ~ +150  | °C   |

\* With respect to V<sub>SS</sub> (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum rating are exceeded. Normal operation should be under recommended operating condition. If these conditions are exceeded, it could affect reliability of LSI.



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# HD146818

## ■ RECOMENDED OPERATING CONDITIONS

| Item                  | Symbol     | min          | typ | max      | Unit |
|-----------------------|------------|--------------|-----|----------|------|
| Supply Voltage        | $V_{CC}^*$ | 4.5          | 5.0 | 5.25     | V    |
| Input Voltage         | $V_{IL}^*$ | -0.3         | —   | 0.7      | V    |
|                       | $V_{IH}^*$ | $V_{CC}-1.0$ | —   | $V_{CC}$ | V    |
| Operating Temperature | $T_{opr}$  | 0            | 25  | 70       | °C   |

\* With respect to  $V_{SS}$  (SYSTEM GND)

(NOTE) Refer to Battery Backed-up Electrical characteristics.

## ■ ELECTRICAL CHARACTERISTICS

- DC CHARACTERISTICS ( $V_{CC} = 4.5 \sim 5.25V$ ,  $V_{SS} = 0V$ ,  $T_a = 0 \sim +70^\circ C$ , unless otherwise noted.)

| Item                 | Symbol                                                            | Test Condition | min          | typ | max      | Unit |
|----------------------|-------------------------------------------------------------------|----------------|--------------|-----|----------|------|
| Input "High" Voltage | $AD_0 \sim AD_7, \overline{CE}, AS, R/\overline{W}, DS, CKFS, PS$ |                | $V_{CC}-2.0$ | —   | $V_{CC}$ | V    |
|                      | $\overline{RES}$                                                  |                | $V_{CC}-1.0$ | —   | $V_{CC}$ |      |
|                      | $OSC_1$                                                           |                | $V_{CC}-1.0$ | —   | $V_{CC}$ |      |
|                      | $AD_0 \sim AD_7, \overline{CE}, AS, R/\overline{W}, DS, CKFS, PS$ |                | 0.7          | —   | 0.7      |      |

• AC CHARACTERISTICS ( $V_{CC} = 4.5 \sim 5.25V$ ,  $V_{SS} = 0V$ ,  $T_a = 0 \sim +70^\circ C$ , unless otherwise noted.)

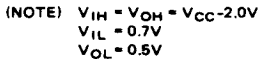
BUS TIMING

| Item                                                           | Symbol     | min | typ | max | Unit |
|----------------------------------------------------------------|------------|-----|-----|-----|------|
| Cycle Time                                                     | $t_{cyc}$  | 953 | —   | —   | ns   |
| Pulse Width, AS/ALE "High"                                     | $PW_{ASH}$ | 100 | —   | —   | ns   |
| AS Rise Time                                                   | $t_{ASr}$  | —   | —   | 30  | ns   |
| AS Fall Time                                                   | $t_{ASf}$  | —   | —   | 30  | ns   |
| Delay Time DS/E to AS/ALE Rise                                 | $t_{ASD}$  | 40  | —   | —   | ns   |
| DS Rise Time                                                   | $t_{DSr}$  | —   | —   | 30  | ns   |
| DS Fall Time                                                   | $t_{DSf}$  | —   | —   | 30  | ns   |
| Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ "High"  | $PW_{DSH}$ | 325 | —   | —   | ns   |
| Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ "Low"  | $PW_{DSL}$ | 300 | —   | —   | ns   |
| Delay Time, AS/ALE to DS/E Rise                                | $t_{ASDS}$ | 90  | —   | —   | ns   |
| Address Setup Time (R/ $\overline{W}$ )                        | $t_{AS1}$  | 15  | —   | —   | ns   |
| Address Setup Time ( $\overline{CE}$ )                         | $t_{AS2}$  | 55  | —   | —   | ns   |
| Address Hold Time (R/ $\overline{W}$ , $\overline{CE}$ )       | $t_{AH}$   | 10  | —   | —   | ns   |
| Muxed Address Valid Time to AS/ALE Fall                        | $t_{ASL}$  | 50  | —   | —   | ns   |
| Muxed Address Hold Time                                        | $t_{AHL}$  | 20  | —   | —   | ns   |
| Peripheral Data Setup Time                                     | $t_{DSW}$  | 195 | —   | —   | ns   |
| Write Data Hold Time                                           | $t_{DHW}$  | 0   | —   | —   | ns   |
| Peripheral Output Data Delay Time From DS/E or $\overline{RD}$ | $t_{DDR}$  | —   | —   | 220 | ns   |
| Read Data Hold Time                                            | $t_{DHR}$  | 10  | —   | —   | ns   |
| Input Rise and Fall Time                                       | $t_r, t_f$ | —   | —   | 30  | ns   |

CONTROL SIGNAL TIMING

| Item                              | Symbol     | min | typ | max  | Unit    |
|-----------------------------------|------------|-----|-----|------|---------|
| Oscillator Startup                | $t_{RC}$   | —   | —   | 100  | ms      |
|                                   |            | —   | —   | 1000 |         |
| Reset Pulse Width                 | $t_{RWL}$  | 5.0 | —   | —    | $\mu s$ |
| Reset Delay Time                  | $t_{RLH}$  | 5.0 | —   | —    | $\mu s$ |
| Power Sense Pulse Width           | $t_{PWL}$  | 5.0 | —   | —    | $\mu s$ |
| Power Sense Delay Time            | $t_{PLH}$  | 5.0 | —   | —    | $\mu s$ |
| $\overline{IRQ}$ Release from DS  | $t_{IRDS}$ | —   | —   | 2.0  | $\mu s$ |
| $\overline{IRQ}$ Release from RES | $t_{IRR}$  | —   | —   | 2.0  | $\mu s$ |
| VRT Bit Delay                     | $t_{VRTD}$ | —   | —   | 2.0  | $\mu s$ |

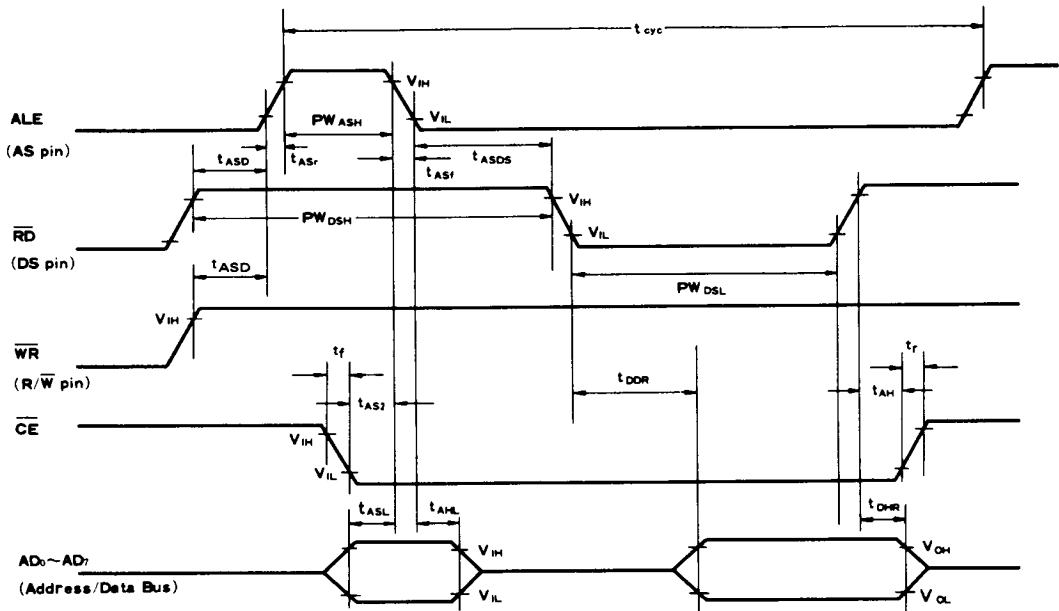




### Figure 1 Bus Read, Write Timing (6801 Family)

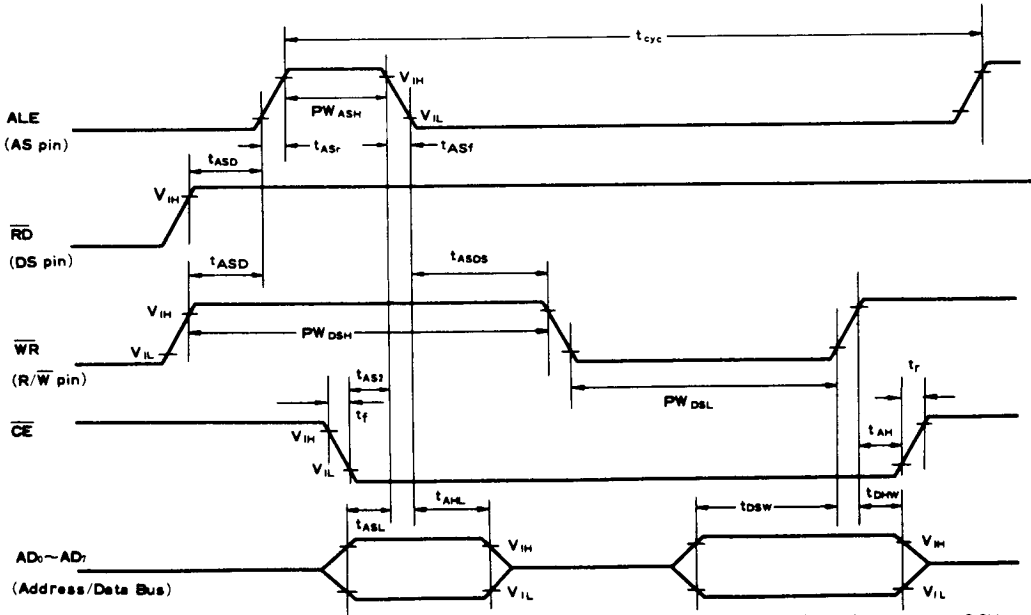


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**Figure 2 Read Timing (8085 Family)**

(NOTE)  $V_{IH} = V_{OH} = V_{CC} - 2.0V$   
 $V_{IL} = 0.7V, V_{OL} = 0.5V$



### Figure 3 Write Timing (8085 Family)

(NOTE)  $V_{IH} = V_{CC} - 2.0V$   
 $V_{IL} = 0.7V$



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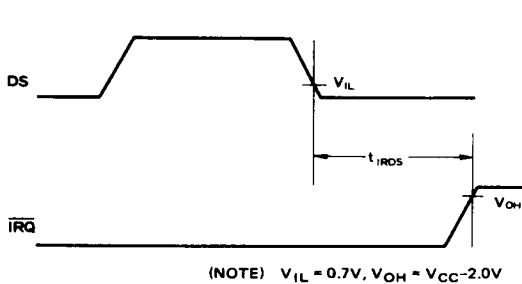


Figure 4  $\overline{IRQ}$  Release Delay (from DS)

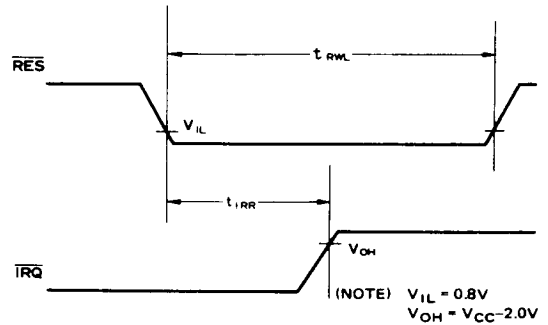
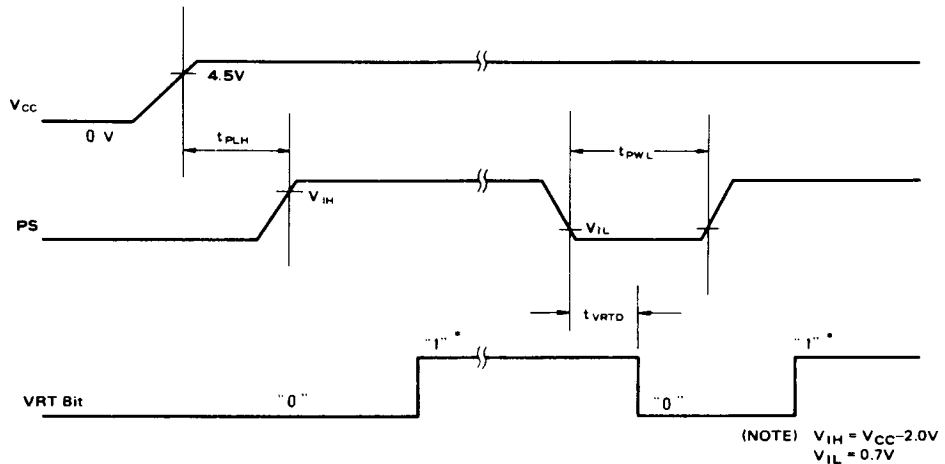


Figure 5  $\overline{IRQ}$  Release Delay (from  $\overline{RES}$ )



\* The VRT bit is set to a "1" by reading control register #D. There is no additional way to clear the VRT bit.

Figure 6 VRT Bit Clear Timing

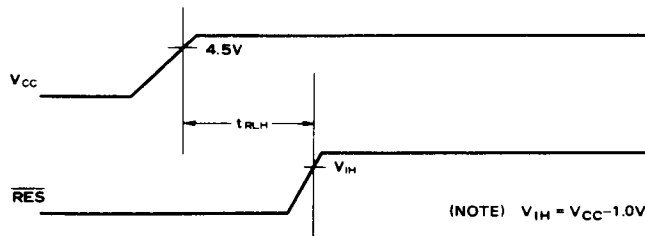


Figure 7  $\overline{RES}$  Release Delay



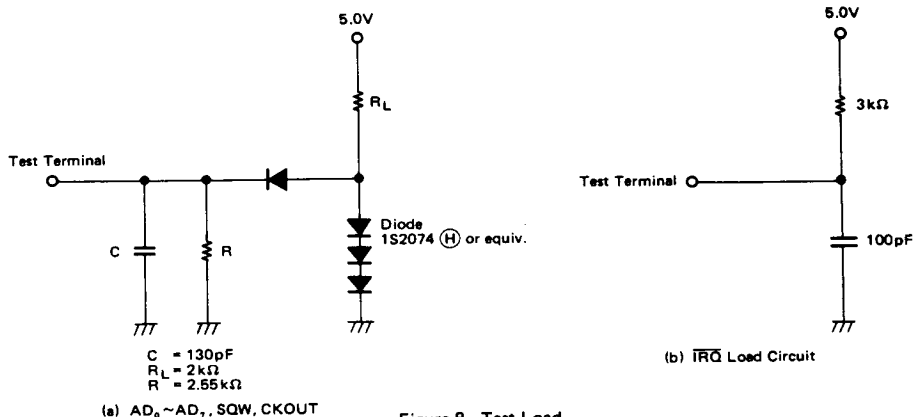


Figure 8 Test Load

### ■ BATTERY BACKED-UP OPERATION

### ● DEFINITION OF BATTERY BACKED-UP OPERATION

Active functions

(1) Clock function

(2) Retention of RAM data

(3) RES,  $\overline{IRQ}$ , CKFS, CKOUT, PS, SQW functions

Inactive functions

(1) Data bus read/write operation

### ● BATTERY BACKED-UP ELECTRICAL CHARACTERISTICS ( $V_{SS} = 0V$ , $T_A = 0 \sim +70^\circ C$ , unless otherwise noted.)

| Item                                 |                     | Symbol                         | Test Condition                                                     |                        | min                    | typ              | max | Unit |
|--------------------------------------|---------------------|--------------------------------|--------------------------------------------------------------------|------------------------|------------------------|------------------|-----|------|
| Supply Voltage                       |                     | V <sub>CCL</sub>               |                                                                    |                        | 2.7                    | —                | 4.5 | V    |
| Supply Current                       | Crystal Oscillation | I <sub>CCL</sub> *             | V <sub>CCL</sub> = 3.0V<br>SQW : disable<br>CKOUT : fosc (No load) | 4MHz                   | —                      | —                | 600 | μA   |
|                                      |                     |                                |                                                                    | 1MHz                   | —                      | —                | 350 | μA   |
|                                      |                     |                                |                                                                    | 32kHz                  | —                      | 50               | 100 | μA   |
|                                      | External Clock      |                                | V <sub>CCL</sub> = 3.0V<br>SQW : disable<br>CKOUT : fosc (No load) | 4MHz                   | —                      | —                | 500 | μA   |
|                                      |                     |                                |                                                                    | 1MHz                   | —                      | —                | 150 | μA   |
|                                      |                     |                                |                                                                    | 32kHz                  | —                      | 30               | 70  | μA   |
| Battery Backed-up Transit Setup Time |                     | t <sub>CE</sub>                | Fig. 9                                                             |                        | 0                      | —                | —   | ns   |
| Operation Recovery Time              |                     | t <sub>R</sub>                 |                                                                    |                        | t <sub>cyc</sub>       | —                | —   | ns   |
| Supply Voltage Fall Time             |                     | t <sub>pf</sub>                |                                                                    |                        | 300                    | —                | —   | μs   |
| Supply Voltage Rise Time             |                     | t <sub>pr</sub>                |                                                                    |                        | 300                    | —                | —   | μs   |
| Input "High" Voltage                 | V <sub>IHL</sub>    | V <sub>CCL</sub> = 2.7V ~ 3.5V | CE, PS                                                             | 0.7 x V <sub>CCL</sub> | —                      | V <sub>CCL</sub> | V   |      |
|                                      |                     |                                | CKFS                                                               | 2.5                    | —                      | V <sub>CCL</sub> | V   |      |
|                                      |                     | V <sub>CCL</sub> = 3.5V ~ 4.5V | RES                                                                | 0.8 x V <sub>CCL</sub> | —                      | V <sub>CCL</sub> | V   |      |
|                                      |                     |                                | OSC <sub>1</sub>                                                   | 0.8 x V <sub>CCL</sub> | —                      | V <sub>CCL</sub> | V   |      |
| Input "Low" Voltage                  | V <sub>ILL</sub>    |                                | CKFS, PS                                                           | -0.3                   | —                      | 0.5              | V   |      |
|                                      |                     |                                | RES                                                                | -0.3                   | —                      | 0.5              | V   |      |
|                                      |                     |                                | OSC <sub>1</sub>                                                   | -0.3                   | —                      | 0.5              | V   |      |
| Output "High" Voltage                |                     | V <sub>OHL</sub>               | I <sub>OH</sub> = -800μA                                           | SQW, CKOUT             | 0.8 x V <sub>CCL</sub> | —                | —   | V    |
| Output "Low" Voltage                 | V <sub>OLL</sub>    | I <sub>OL</sub> = 800μA        | SQW, CKOUT                                                         | —                      | —                      | 0.5              | V   |      |
|                                      |                     |                                | TRQ                                                                | —                      | —                      | 0.5              | V   |      |

\* The time-base frequency to be used needs to be chosen in Register A.



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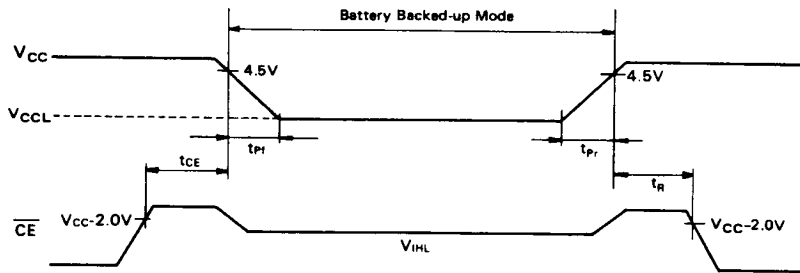


Figure 9 Battery Backed-up Timing

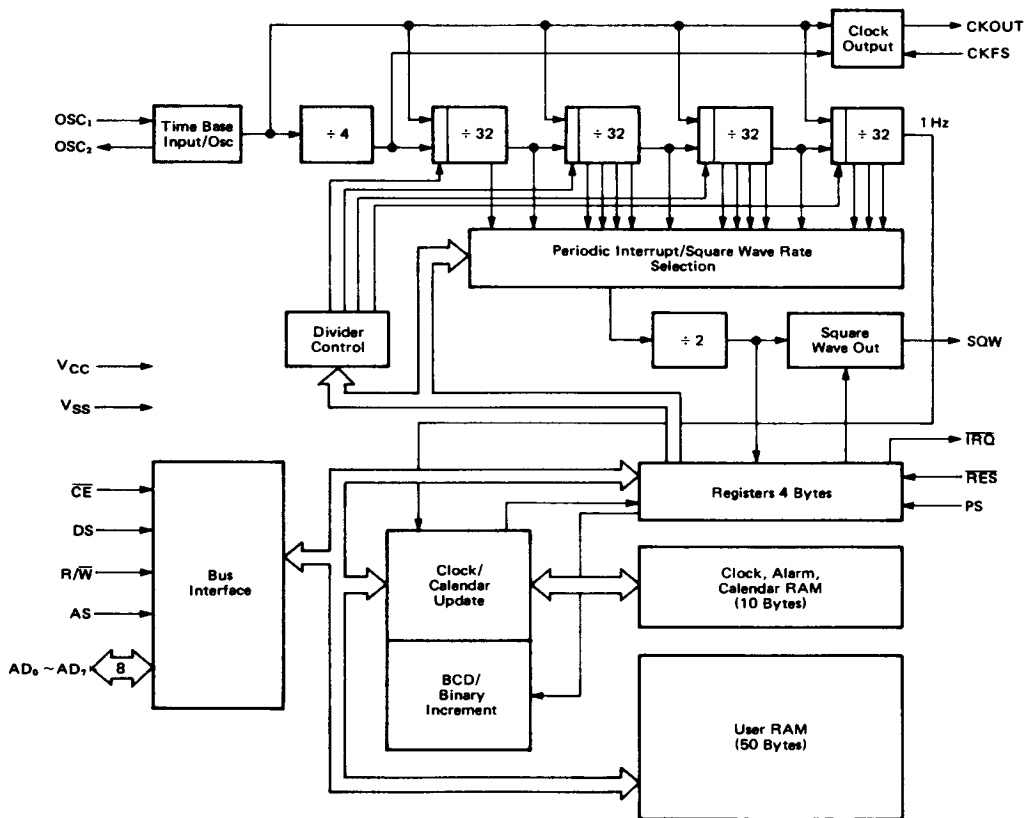


Figure 10 Block Diagram



# ■ CRYSTAL OSCILLATION CIRCUIT

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 11.

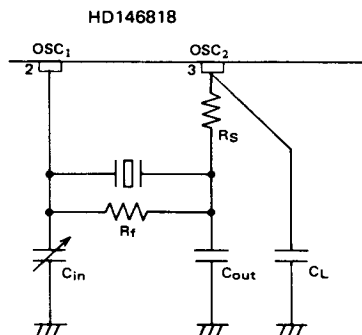


Figure 11 Crystal Oscillator Connection

# ■ NOTE FOR BOARD DESIGN OF THE OSCILLATION CIRCUIT

In designing the board, the following notes should be taken when the crystal oscillator is used.

- (1) Crystal oscillator, load capacity  $C_{in}$ ,  $C_{out}$ ,  $C_L$  and  $R_f$ ,  $R_s$  must be placed near the LSI as much as possible.  
[Normal oscillation may be disturbed when external noise is induced to pin 2 and 3.]

Table 1 Oscillator Circuit Parameters

| Parameter \ $f_{osc}$ | 4.194304 MHz      | 1.048576 MHz       | 32.768 kHz          |
|-----------------------|-------------------|--------------------|---------------------|
| $R_s$                 | —                 | —                  | 150 k $\Omega$      |
| $R_f$                 | 150 k $\Omega$    | 150 k $\Omega$     | 5.6 M $\Omega$      |
| $C_{in}$              | 22 pF             | 33 pF              | 15 pF               |
| $C_{out}$             | 22 pF             | 33 pF              | 33 pF               |
| $C_L$                 | —                 | —                  | 33 pF               |
| $C_I$                 | 80 $\Omega$ (max) | 700 $\Omega$ (max) | 40 k $\Omega$ (max) |

- (NOTE) 1.  $R_s$ ,  $C_L$  are used for 32.768 kHz only.  
 2. Capacitance ( $C_{in}$ ) should be adjusted to accurate frequency. Parameters listed above are applied to the supply current measurement (See table of DC CHARACTERISTICS).  
 3.  $C_I$ : Crystal impedance

- (2) Pin 3 signal line should be wired apart from pin 4 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when this signal is feedbacked to OSC<sub>1</sub>.
- (3) A signal line or a power source line must not cross or go near the oscillation circuit line as shown in the right figure to prevent the induction from these lines and perform the correct oscillation. The resistance among OSC<sub>1</sub>, OSC<sub>2</sub> and other pins should be over 10M $\Omega$ .

The following design must be avoided.

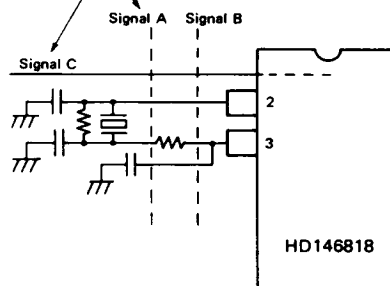
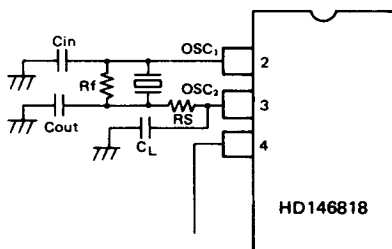


Figure 12 Note for Board Design of the Oscillation Circuit



# HD146818

## ■ INTERFACE CIRCUIT FOR HD6801, HD6301 AND 8085 PROCESSOR

HD146818 has a new interface circuit which permits the

Figure 13 shows the bus control circuit. This circuit automatically selects the processor type by using AS/ALE to latch the state of DS/RD pin. Since DS is always "Low" and RD is

HD146818 to be directly interfaced with many type of multiplexed bus microprocessor such as HD6801, HD6301 and 8085 etc.

always "High during AS/ALE, the latch automatically indicates which processor type is connected.

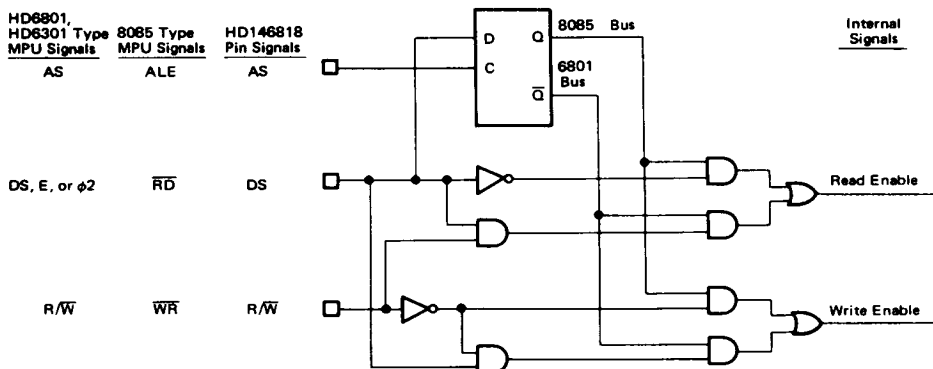


Figure 13 Functional Diagram of the Bus Control Circuit

## ■ ADDRESS MAP

Figure 14 shows the address map of the HD146818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except Registers C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section.

### ● Time, Calendar, and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program

may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

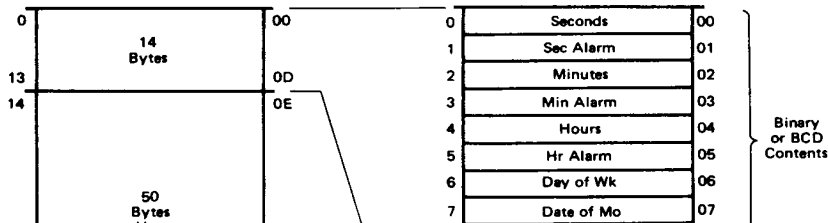


Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248  $\mu$ s at the 4.194304 MHz and 1.048567 MHz time bases and 1948  $\mu$ s for the 32.768 kHz time base. The Update Cycle section shows how to accommodate

the update cycle in the processor program.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is "1". The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 2 Time, Calendar, and Alarm Data Modes

| Address Location | Function                   | Decimal Range | Range                                 |                                       | Example*         |               |
|------------------|----------------------------|---------------|---------------------------------------|---------------------------------------|------------------|---------------|
|                  |                            |               | Binary Data Mode                      | BCD Data Mode                         | Binary Data Mode | BCD Data Mode |
| 0                | Seconds                    | 0 ~ 59        | \$00 ~ \$3B                           | \$00 ~ \$59                           | 15               | 21            |
| 1                | Seconds Alarm              | 0 ~ 59        | \$00 ~ \$3B                           | \$00 ~ \$59                           | 15               | 21            |
| 2                | Minutes                    | 0 ~ 59        | \$00 ~ \$3B                           | \$00 ~ \$59                           | 3A               | 58            |
| 3                | Minutes Alarm              | 0 ~ 59        | \$00 ~ \$3B                           | \$00 ~ \$59                           | 3A               | 58            |
| 4                | Hours (12 Hour Mode)       | 1 ~ 12        | \$01 ~ \$0C (AM) and \$81 ~ \$8C (PM) | \$01 ~ \$12 (AM) and \$81 ~ \$92 (PM) | 05               | 05            |
|                  | Hours (24 Hour Mode)       | 0 ~ 23        | \$00 ~ \$17                           | \$00 ~ \$23                           | 05               | 05            |
| 5                | Hours Alarm (12 Hour Mode) | 1 ~ 12        | \$01 ~ \$0C (AM) and \$81 ~ \$8C (PM) | \$01 ~ \$12 (AM) and \$81 ~ \$92 (PM) | 05               | 05            |
|                  | Hours Alarm (24 Hour Mode) | 0 ~ 23        | \$00 ~ \$17                           | \$00 ~ \$23                           | 05               | 05            |
| 6                | Day of the Week Sunday = 1 | 1 ~ 7         | \$01 ~ \$07                           | \$01 ~ \$07                           | 05               | 05            |
| 7                | Day of the Month           | 1 ~ 31        | \$01 ~ \$1F                           | \$01 ~ \$31                           | 0F               | 15            |
| 8                | Month                      | 1 ~ 12        | \$01 ~ \$0C                           | \$01 ~ \$12                           | 02               | 02            |
| 9                | Year                       | 0 ~ 99**      | \$00 ~ \$63                           | \$00 ~ \$99                           | 4F               | 79            |

\* Example: 5:58:21 Thursday 15th February 1979

\*\* Set the lower two digits of year in AD. If this number is multiple of 4, update applied to leap year is excused.

#### • Static CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the HD146818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional HD146818s may be included in the system. The time/calendar functions may be disabled by holding the dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

#### ■ INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517  $\mu$ s. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the  $\overline{\text{IRQ}}$  pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the  $\overline{\text{IRQ}}$  pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such



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earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the IRQ pin is asserted "Low".  $\overline{\text{IRQ}}$  is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The

IRQF bit in Register C is a "1" whenever the  $\overline{\text{IRQ}}$  pin is being driven "Low".

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one of more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

## ■ DIVIDER STAGES

The HD146818 has 22 binary-divider stages following the time base as shown in Figure 10. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bus (DV2, DV1, and DV0) in Register A.

## ● Divider Control

The divider-control bits have three uses, as shown in Table 3. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the HD146818.

Table 3 Divider Configuration

| Time-Base Frequency | Divider Bits Register A |     |     | Select Pin CKFS | Output Pin CKOUT | Operation Mode | Divider Reset | Bypass First N-Divider Bits |
|---------------------|-------------------------|-----|-----|-----------------|------------------|----------------|---------------|-----------------------------|
|                     | DV2                     | DV1 | DV0 |                 |                  |                |               |                             |
| 4.194304 MHz        | 0                       | 0   | 0   | High            | 4.194304 MHz     | Yes            | —             | N = 0                       |
|                     |                         |     |     | Low             | 1.048576 MHz     |                |               |                             |
| 1.048576 MHz        | 0                       | 0   | 1   | High            | 1.048576 MHz     | Yes            | —             | N = 2                       |
|                     |                         |     |     | Low             | 262.144 MHz      |                |               |                             |
| 32.768 kHz          | 0                       | 1   | 0   | High            | 32.768 kHz       | Yes            | —             | N = 7                       |
|                     |                         |     |     | Low             | 8.192 kHz        |                |               |                             |
| Any                 | 1                       | 1   | 1   |                 |                  | No             | Yes           | —                           |
| Any                 | 1                       | 1   | 1   |                 |                  | No             | Yes           | —                           |

## ● Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 10. The first purpose of selecting a divider tap is to generate a square-wave output signal in the SQW pin. Four bits in Register A establish the square-wave frequency as listed in Table 4. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

## ● Periodic Interrupt Selection

The periodic interrupt allows the  $\overline{\text{IRQ}}$  pin to be triggered from once every 500 ms to once every 30.517  $\mu\text{s}$ . The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 4 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of input from contact closures to serial receive bits or ties. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.



Table 4 Periodic Interrupt Rate and Square Wave Output Frequency

| Rate Select<br>Control Register 1 |     |     |     | 4.194304 or 1.048576 MHz<br>Time Base  |                         | 32.768 kHz<br>Time Base                |                         |
|-----------------------------------|-----|-----|-----|----------------------------------------|-------------------------|----------------------------------------|-------------------------|
|                                   |     |     |     | Periodic<br>Interrupt Rate<br>$t_{PI}$ | SQW Output<br>Frequency | Periodic<br>Interrupt Rate<br>$t_{PI}$ | SQW Output<br>Frequency |
| RS3                               | RS2 | RS1 | RS0 |                                        |                         |                                        |                         |
| 0                                 | 0   | 0   | 0   | None                                   | High Level              | None                                   | High Level              |
| 0                                 | 0   | 0   | 1   | 30.517 $\mu$ s                         | 32.768 kHz              | 3.90625 ms                             | 256 Hz                  |
| 0                                 | 0   | 1   | 0   | 61.035 $\mu$ s                         | 16.384 kHz              | 7.8125 ms                              | 128 Hz                  |
| 0                                 | 0   | 1   | 1   | 122.070 $\mu$ s                        | 8.192 kHz               | 122.070 $\mu$ s                        | 8.192 kHz               |
| 0                                 | 1   | 0   | 0   | 244.141 $\mu$ s                        | 4.096 kHz               | 244.141 $\mu$ s                        | 4.096 kHz               |
| 0                                 | 1   | 0   | 1   | 488.281 $\mu$ s                        | 2.048 kHz               | 488.281 $\mu$ s                        | 2.048 kHz               |
| 0                                 | 1   | 1   | 0   | 976.562 $\mu$ s                        | 1.024 kHz               | 976.562 $\mu$ s                        | 1.024 kHz               |
| 0                                 | 1   | 1   | 1   | 1.953125 ms                            | 512 Hz                  | 1.953125 ms                            | 512 Hz                  |
| 1                                 | 0   | 0   | 0   | 3.90625 ms                             | 256 Hz                  | 3.90625 ms                             | 256 Hz                  |
| 1                                 | 0   | 0   | 1   | 7.8125 ms                              | 128 Hz                  | 7.8125 ms                              | 128 Hz                  |
| 1                                 | 0   | 1   | 0   | 15.625 ms                              | 64 Hz                   | 15.625 ms                              | 64 Hz                   |
| 1                                 | 0   | 1   | 1   | 31.25 ms                               | 32 Hz                   | 31.25 ms                               | 32 Hz                   |
| 1                                 | 1   | 0   | 0   | 62.5 ms                                | 16 Hz                   | 62.5 ms                                | 16 Hz                   |
| 1                                 | 1   | 0   | 1   | 125 ms                                 | 8 Hz                    | 125 ms                                 | 8 Hz                    |
| 1                                 | 1   | 1   | 0   | 250 ms                                 | 4 Hz                    | 250 ms                                 | 4 Hz                    |
| 1                                 | 1   | 1   | 1   | 500 ms                                 | 2 Hz                    | 500 ms                                 | 2 Hz                    |

• **Initialization of the Time and the Start Sequence**

The first update of the time occurs about 500ms later after the SET bit of control register B is reset. So keep followings in mind when initializing and adjusting the time.

**Procedure of time initialization**

- (1) Set the SET bit of control register B. (SET = "1")
- (2) Set "1" into all the DV0, 1, 2 bits of control register A. (DV0 = DV1 = DV2 = "1")
- (3) Set the time and calendar to each RAM.
- (4) Set the frequency in use into DV0, 1 and DV2.

day shown below.

| Calendar, Time of day<br>& Status after Update                                                                                                          | Examples                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| If 29th 23:59:59 in all the months is initialized, update to 1st in the next month is executed. (Jan. — Dec. However except for Feb. 29th in leap year) | Mar. 29th<br>→ Apr. 1st |
| If 30th 23:59:59 in Apr., June, Sept., and                                                                                                              | Apr. 30th               |

date cycle takes 248  $\mu$ s while a 32.768 kHz time base update cycle takes 1984  $\mu$ s. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The HD146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes "1", the update cycle begins 244  $\mu$ s later. Therefore, if a "0" is read on the UIP bit, the user has at least 244  $\mu$ s before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the

time needed to read valid time/calendar data to exceed 244  $\mu$ s.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set "1" between the setting of the PF bit in Register C (see Figure 16) Periodic interrupts that occur at a rate of greater than  $t_{BUC} + t_{UC}$  allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within  $(t_{PI} \div 2) + t_{BUC}$  to insure that data is not read during the update cycle.

## ■ POWER-DOWN CONSIDERATIONS

In most systems, the HD146818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability according to the specification described in the section regarding Battery Backed-up operation.

The chip enable ( $\overline{CE}$ ) pin controls all bus inputs ( $R/\overline{W}$ , DS, AS,  $AD_0 \sim AD_7$ ).  $\overline{CE}$ , when negated, disallows any unintended modification of the RTC data by the bus.  $\overline{CE}$  also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

During and after the power source conversion, the  $V_{IN}$  maximum specification must never be exceeded. Failure to meet the  $V_{IN}$  maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

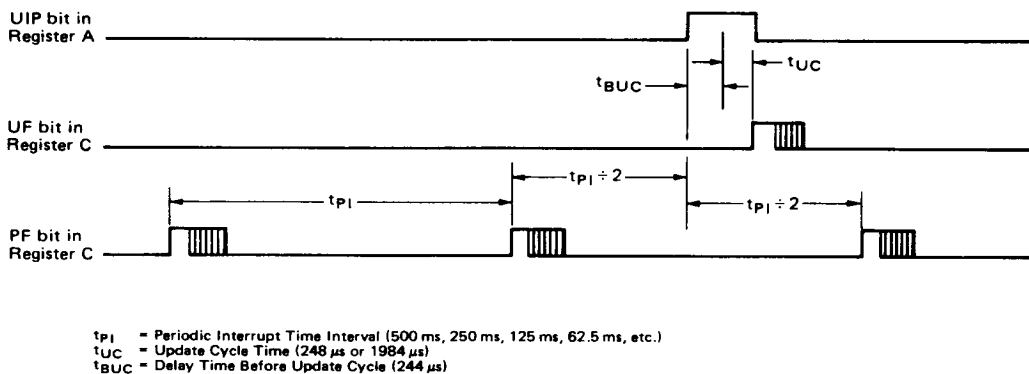


Figure 16 Update-Ended and Periodic Interrupt Relationship



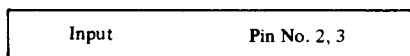
## SIGNAL DESCRIPTIONS

The block diagram in Figure 10, shows the pin connection with the major internal functions of the HD146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

### • V<sub>CC</sub>, V<sub>SS</sub>

DC power is provided to the part on these two pins, V<sub>CC</sub> being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

### • OSC<sub>1</sub>, OSC<sub>2</sub> – Time Base



The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC<sub>1</sub> as shown in Figure 17. The time-base frequency to be used is chosen in Register A.

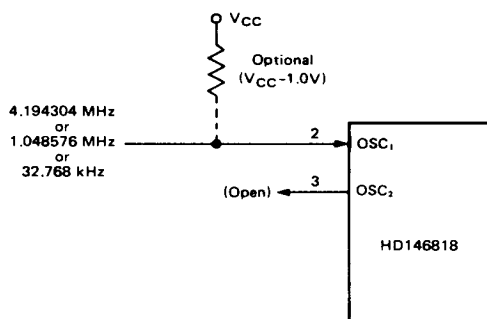
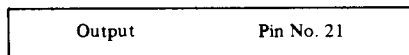


Figure 17 External Time-Base Connection

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 11.

### • CKOUT – Clock Out



The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 5.

### • CKFS – Clock Out Frequency Select



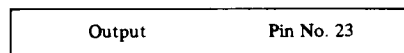
The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V<sub>CC</sub> causes CKOUT to be the same frequency as the time base at the OSC<sub>1</sub> pin. When CKFS is at V<sub>SS</sub>, CKOUT is the OSC<sub>1</sub> time-base frequency divided

by four. Table 5 summarizes the effect of CKFS.

Table 5 Clock Output Frequencies

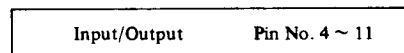
| Time Base (OSC <sub>1</sub> ) Frequency | Clock Frequency Select Pin (CKFS) | Clock Frequency Output Pin (CKOUT) |
|-----------------------------------------|-----------------------------------|------------------------------------|
| 4.194304 MHz                            | "High"                            | 4.194304 MHz                       |
| 4.194304 MHz                            | "Low"                             | 1.048576 MHz                       |
| 1.048576 MHz                            | "High"                            | 1.048576 MHz                       |
| 1.048576 MHz                            | "Low"                             | 262.144 kHz                        |
| 32.768 kHz                              | "High"                            | 32.768 kHz                         |
| 32.768 kHz                              | "Low"                             | 8.192 kHz                          |

### • SQW – Square Wave



The SQW pin can output a signal one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 4. The SQW signal may be turned on and off using a bit in Register B.

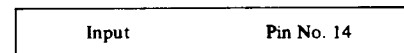
### • AD<sub>0</sub> ~ AD<sub>7</sub> – Multiplexed Bidirectional Address/Data Bus



Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the HD146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the HD146818 latches the address from AD<sub>0</sub> to AD<sub>7</sub>. Valid write data must be presented and held stable during the latter portion of the DS or WR pulses. In a read cycle, the HD146818 outputs 8 bits of data during the latter portion of the DS or RD pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in the HD6801, HD6301 case or RD rises in the other case.

### • AS – Multiplexed Address Strobe



A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the HD146818. The bus control circuit in the HD146818 also latches the state of the DS pin with the falling edge of AS or ALE.

### • DS – Data Strobe or Read



The DS pin has two interpretations via the bus control circuit. When emanating from 6801 family type processor,



# HD146818

DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and  $\phi_2$  ( $\phi_2$  clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second interpretation of DS is that of RD, MEMR or

interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ pin, the processor program normally reads Register C. The RES pin also clears pending interrupts.

When no interrupt conditions are present, the IRQ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an IRQ bus with one pullup at the processor

DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The bus control circuit, within the HD146818, latches the state of the DS pin on the falling edge of AS/ALE. When 6801

## • RES – Reset

|       |            |
|-------|------------|
| Input | Pin No. 18 |
|-------|------------|

The RES pin does not affect the clock, calendar, or RAM

mode. DS must be “Low” during AS/ALE, which is the case with 6801 family multiplexed bus processors. To insure the 8085 mode of this circuit the DS pin must remain “High” during the time AS/ALE is “High”.

## • R/W – Read/Write

|       |            |
|-------|------------|
| Input | Pin No. 15 |
|-------|------------|

The bus control circuit treats the R/W pin in one of two ways. When 6801 family type processor is connected, R/W is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a “High” level on R/W while DS is “High”, whereas a write cycle is a “Low” on R/W during DS

The second interpretation of R/W is as a negative write pulse, WR, MEMW, and I/OW from 8085 type processors. This circuit in this mode gives R/W pin the same meaning as the write (W) pulse on many generic RAMs.

functions. On powerup, the RES pin must be held “Low” for the specified time,  $t_{RLH}$ , in order to allow the power supply to stabilize. Figure 18 shows a typical representation of the RES pin circuit.

When RES is “Low” the following occurs:

- Periodic Interrupt Enable (PIE) bit is cleared to “0”.
- Alarm Interrupt Enable (AIE) bit is cleared to “0”.
- Update ended interrupt Enable (UIE) bit is cleared to “0”.
- Update ended Interrupt Flag (UF) bit is cleared to “0”.
- Interrupt Request status Flag (IRQF) bit is cleared to “0”.
- Periodic Interrupt Flag (PF) bit is cleared to “0”.
- Alarm Interrupt Flag (AF) bit is cleared to “0”.
- IRQ pin is in high-impedance state, and
- Square Wave output Enable (SQWE) bit is cleared to “0”.

## • PS – Power Sense

|       |            |
|-------|------------|
| Input | Pin No. 22 |
|-------|------------|

tion commences PS should be permitted to go "High". Output signal from external power sense circuit will be connected to this input.

# REGISTERS

The HD146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

## Register A (\$0A)

| MSB |     |     |     | LSB |     |     |     | Read/Write<br>Register |
|-----|-----|-----|-----|-----|-----|-----|-----|------------------------|
| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |                        |
| UIP | DV2 | DV1 | DV0 | RS3 | RS2 | RS1 | RS0 | except UIP             |

**UIP** – The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244  $\mu$ s (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

Table 6 Update Cycle Times

| UIP Bit | Time Base (OSC <sub>1</sub> ) | Update Cycle Time (t <sub>uc</sub> ) | Minimum Time Before Update Cycle (t <sub>buc</sub> ) |
|---------|-------------------------------|--------------------------------------|------------------------------------------------------|
| 1       | 4.194304 MHz                  | 248 $\mu$ s                          | —                                                    |
| 1       | 1.048576 MHz                  | 248 $\mu$ s                          | —                                                    |
| 1       | 32.768 kHz                    | 1984 $\mu$ s                         | —                                                    |
| 0       | 4.194304 MHz                  | —                                    | 244 $\mu$ s                                          |
| 0       | 1.048576 MHz                  | —                                    | 244 $\mu$ s                                          |
| 0       | 32.768 kHz                    | —                                    | 244 $\mu$ s                                          |

**DV2, DV1, DV0** – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 3 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins half a second later. These three read/write bits are never modified by the RTC and are not affected by RES.

**RS3, RS2, RS1, RS0** – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 4 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by RES and are never changed by the RTC.

## Register B (\$0B)

| MSB |     |     |     | LSB  |    |       |     | Read/Write<br>Register |
|-----|-----|-----|-----|------|----|-------|-----|------------------------|
| b7  | b6  | b5  | b4  | b3   | b2 | b1    | b0  |                        |
| SET | PIE | AIE | UIE | SQWE | DM | 24/12 | DSE |                        |

**SET** – When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by RES or internal functions of the HD146818.

**PIE** – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the  $\overline{\text{IRQ}}$  pin to be driven "Low". A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A "0" in PIE blocks  $\overline{\text{IRQ}}$  from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still at the periodic rate. PIE is not modified by any internal HD146818 functions, but is cleared to "0" by a RES.

**AIE** – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert  $\overline{\text{IRQ}}$ . An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an  $\overline{\text{IRQ}}$  signal. The RES pin clears AIE to "0". The internal functions do not affect the AIE bit.

**UIE** – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert  $\overline{\text{IRQ}}$ . The RES pin going "Low" or the SET bit going "1" clears the UIE bit.

**SQWE** – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a "0" the SQW pin is held "Low". The state of SQWE is cleared by the RES pin. SQWE is a read/write bit.

**DM** – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RES. A "1" in DM signifies binary data, while a "0" in DM specified binary-coded-decimal (BCD) data.

**24/12** – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

**DSE** – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.



## • Register C (\$0C)

| MSB  |    |    |    | LSB |    |    |    | Read-Only<br>Register |
|------|----|----|----|-----|----|----|----|-----------------------|
| b7   | b6 | b5 | b4 | b3  | b2 | b1 | b0 |                       |
| IRQF | PF | AF | UF | 0   | 0  | 0  | 0  |                       |

**IRQF** — The interrupt request flag (IRQF) is set to a “1” when one or more of the following are true:

PF = PIE = “1”

AF = AIE = “1”

UF = UIE = “1”

i.e.,  $IRQF = PF \cdot PIE + AF \cdot AIE + UF \cdot UIE$

Any time the IRQF bit is a “1”, the  $\overline{IRQ}$  pin is driven “Low”. All flag bits are cleared after Register C is read by the program or when the  $\overline{RES}$  pin is low. A program write to Register C does not modify any of the flag bits.

**PF** — The periodic interrupt flag (PF) is a read-only bit which is set to a “1” when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a “1” independent of the state of the PIE bit. PF being a “1” initiates an  $\overline{IRQ}$  signal and the IRQF bit when PIE is also a “1”. The PF bit is cleared by a  $\overline{RES}$  or a software read of Register C.

**AF** — A “1” in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A “1” in the AF causes the  $\overline{IRQ}$  pin to go “Low”, and a “1” to appear in the IRQF bit, when the AIE bit also is a “1”. A  $\overline{RES}$  or a read of Register C clears AF.

**UF** — The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a “1”, the “1” in UF causes the IRQF bit to be a “1”, asserting  $\overline{IRQ}$ . UF is cleared by a Register C read or a  $\overline{RES}$ .

**b3 to b0** — The unused bits of Status Register C are read as “0”s. They can not be written.

## • Register D (\$0D)

| MSB |    |    |    | LSB |    |    |    | Read Only<br>Register |
|-----|----|----|----|-----|----|----|----|-----------------------|
| b7  | b6 | b5 | b4 | b3  | b2 | b1 | b0 |                       |
| VRT | 0  | 0  | 0  | 0   | 0  | 0  | 0  |                       |

**VRT** — The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A “0” appears in the VRT bit when the power-sense pin is “Low”. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the  $\overline{RES}$  pin. The VRT bit can only be set by reading the Register D. For setting this bit, PS signal needs to be “High” level.

**b6 to b0** — The remaining bits of Register D are unused. They cannot be written, but are always read as “0”s.

## ■ NOTE FOR USE

Input Signal, which is not necessary for user's application, should be used fixed to “High” or “Low” level. This is applicable to the following signal pins.

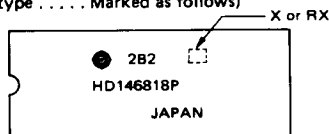
CKFS, PS



**RESTRICTION ON HD146818 USAGE (1)**

The daylight saving function can not be performed on the HD146818P (X type). So do not use this function for the system design.

< Type number > HD146818P (X type . . . . . Marked as follows)

**< Restriction on usage >**

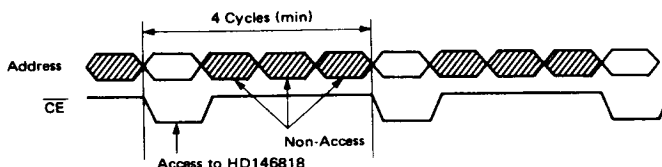
Please set "0" to DSE bit (Daylight Saving Enable bit) on initializing the control register B.  
DSE = "1" is prohibited.

**RESTRICTION ON HD146818 USAGE (2)**

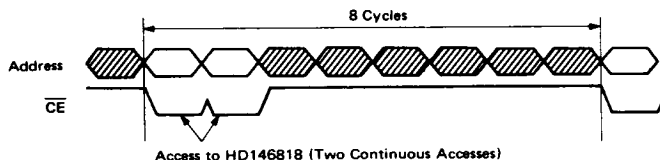
Access to HD146818 needs to be performed under following conditions.

- (i) Chip-enable ( $\overline{CE}$ ) must be asserted to active "Low" level only when MPU performs read/write operation from/into internal RAM (Time and Calendar RAM, Control register, User RAM).
- (ii) User RAM and control register must be accessed in less than 1/4 frequency shown below.  
(Example: After one access, non-access cycles more than three cycles are necessary to be inserted.)

[Example 1]



[Example 2]

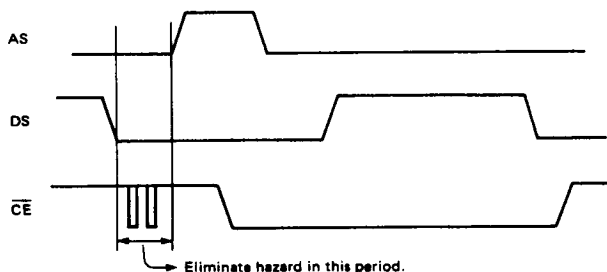


As shown in the above [example 2], when HD146818 is accessed continuously, continuous access must not be executed over fifty times.

- (iii) The application that User RAM is used for program area should be avoided. (Inhibit continuous access.)
- (iv) Minimize the noise by inserting noise bypass condenser between power supply and ground pin ( $V_{CC}-V_{SS}$ ).  
(Insert noise bypass condenser as near HD146818 as possible.)

**RESTRICTION ON HD146818 USAGE (3)**

Chip-enable ( $\overline{CE}$ ) must be stable between falling edge of DS and rising edge of AS shown below. (Address decoder hazard needs to be externally suppressed in this period.)



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