ACPL-P302/W302

0.4 Amp Output Current IGBT Gate Driver Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

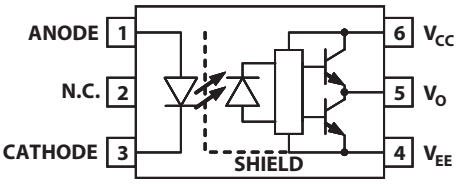
Description

The ACPL-P302/W302 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs.

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- Inverter for home appliances
- Induction cooker
- Switching Power Supplies (SPS)

Functional Diagram



Truth Table	
LED	VO
OFF	LOW
ON	HIGH

Note: A 0.1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Features

- High speed response.
- Ultra high CMR.
- Bootstrappable supply current.
- Available in Stretched SO-6 package
- Package Clearance/Creepage at 8mm (ACPL-W302)
- Safety Approval:
  UL Recognized with 3750 V_{rms} for 1 minute per UL1577.
  CSA Approved.
  IEC/EN/DIN EN 60747-5-2 Approved with V_{IORM} = 630V_{peak} for option 060.

Specifications

- 0.4 A maximum peak output current.
- 0.2 A minimum peak output current.
- 0.7 µs maximum propagation delay over temperature range.
- $I_{CC(max)}$ = 3 mA maximum supply current.
- 10 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1000 V.
- Wide V_{CC} operating range: 10 V to 30 V over temperature range.
- Wide operating temperature range: –40°C to 100°C.

CAUTION: IT IS ADVISED THAT NORMAL STATIC PRECAUTIONS BE TAKEN IN HANDLING AND ASSEMBLY OF THIS COMPONENT TO PREVENT DAMAGE AND/OR DEGRADATION WHICH MAY BE INDUCED BY ESD.

Ordering Information

ACPL-P302 and ACPL-W302 are UL Recognized with3750 Vrms for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-P314 ACPL-W314	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P302-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Example 2:

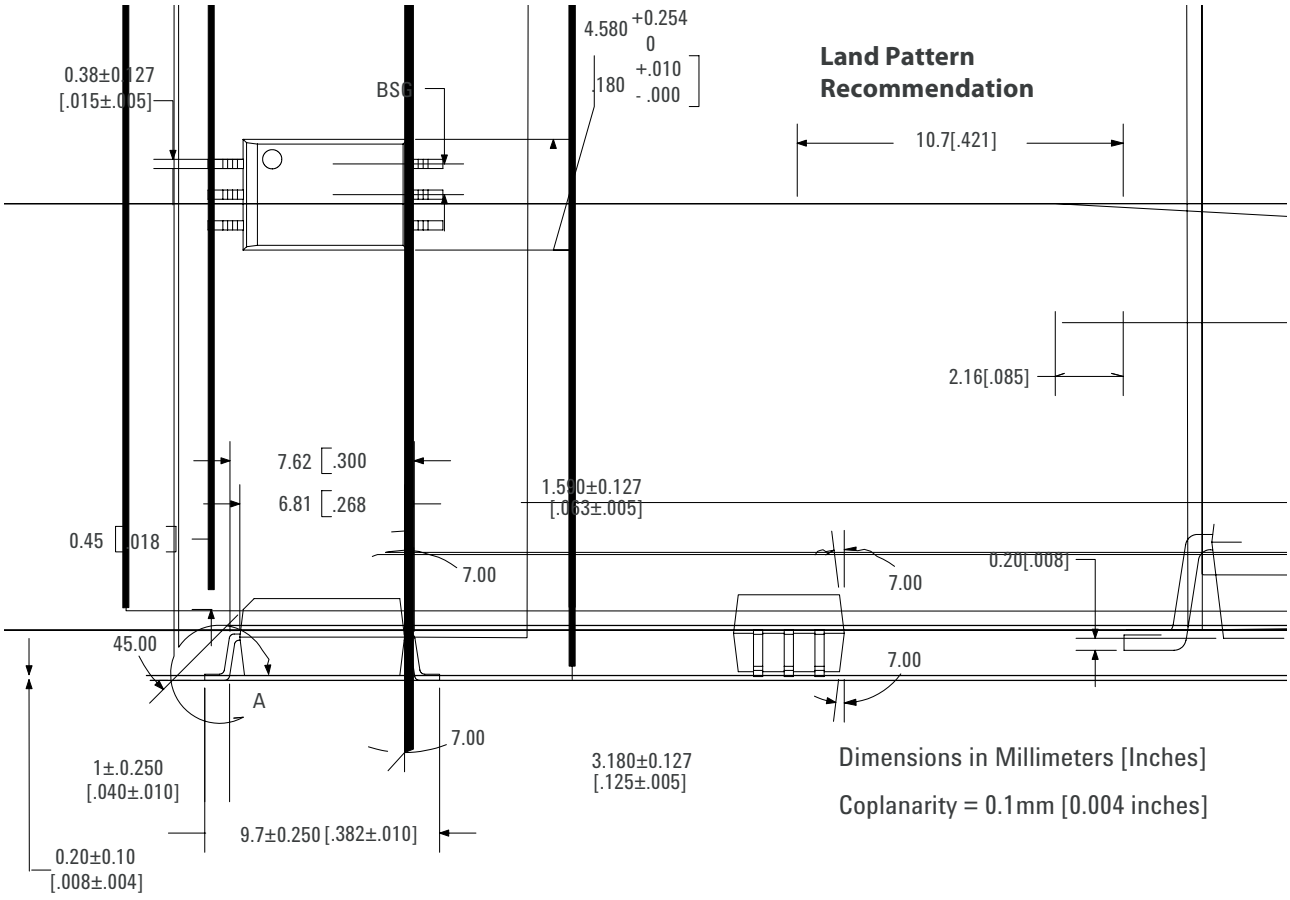
ACPL-P302-000E to order product of Stretched SO-6 Surface Mount package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

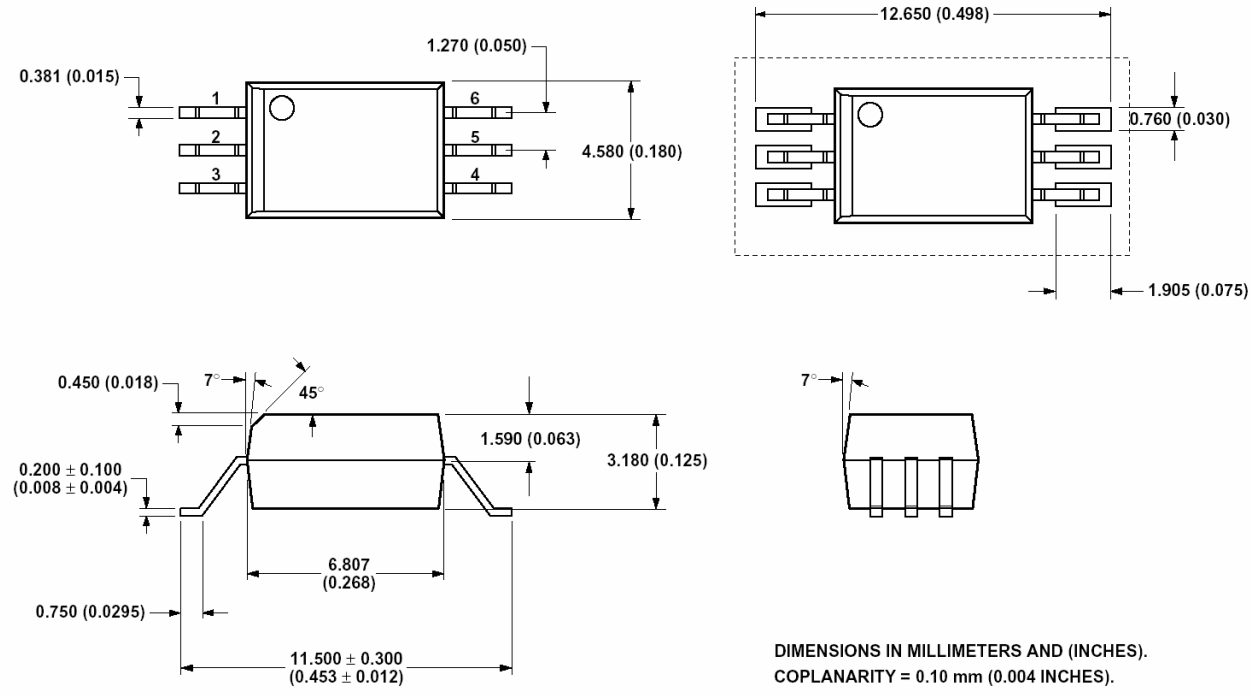
Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawings

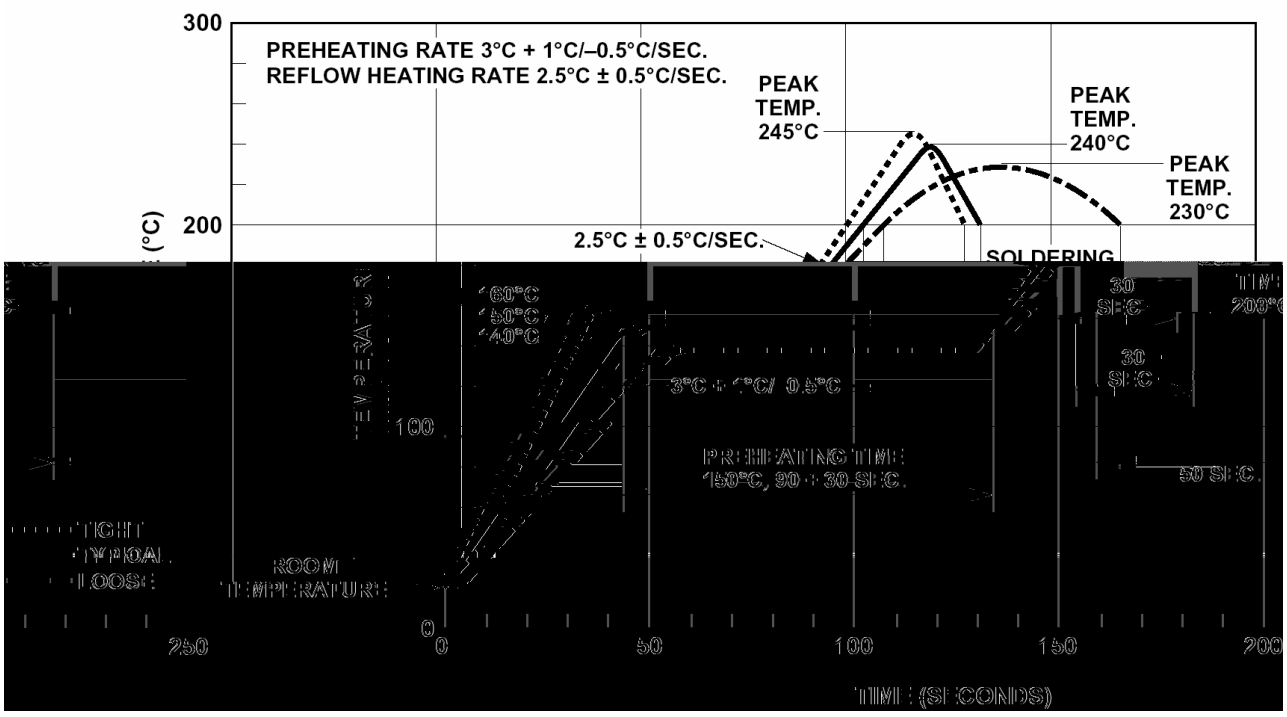
ACPL-P302 Stretched SO-6 Package, 7mm clearance



ACPL-W302 Stretched SO-6 Package

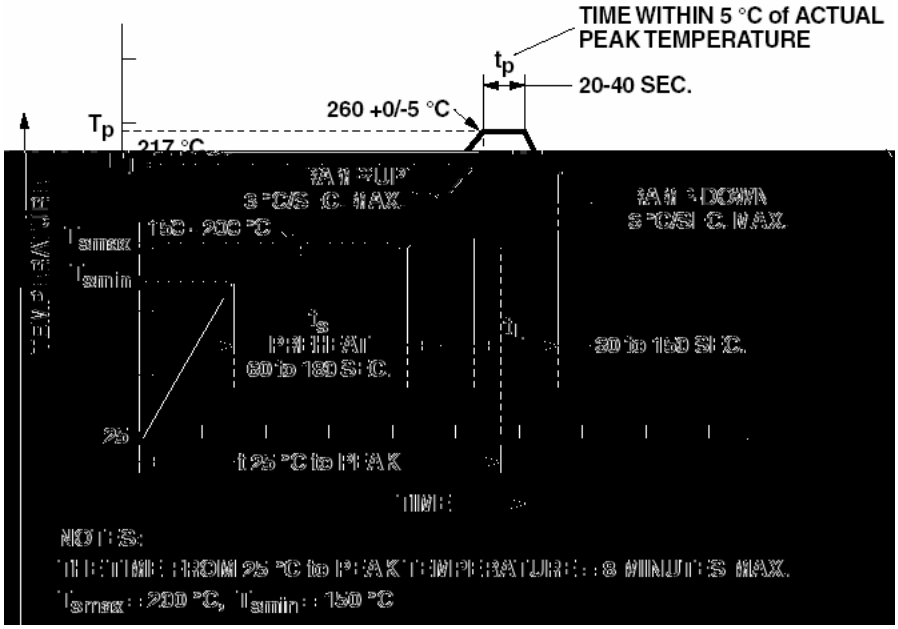


Recommended Solder Reflow Temperature Profile



Note: Non-halide □ux should be used

Recommended Pb-Free IR Profile



Note: Non-halide □ux should be used

Regulatory Information

The ACPL-P302/W302 is pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-2 (Option 060 only)
Approval under:
IEC 60747-5-2 :1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

UL
Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS}. File E55361.

CSA
Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-2 Insulation Characteristics* (ACPL-P302/W302 Option 060)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150V_{rms}		I - IV	
for rated mains voltage ≤ 300V_{rms}		I - III	
for rated mains voltage ≤ 600V_{rms}		I - II	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5=V_{PR}, Type and Sample Test, t_m=60 sec, Partial discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current**	$I_{S, INPUT}$	230	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.

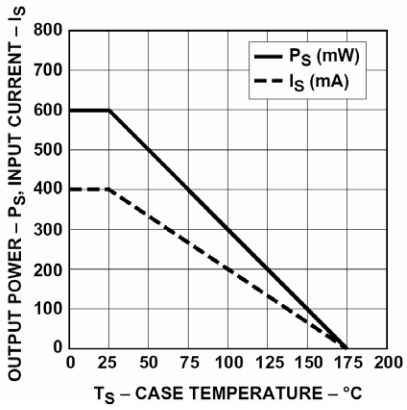


Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P302	ACPL-W302	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		NA	NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current(<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		0.4	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		0.4	A	2
Supply Voltage	V_{CC} - V_{EE}	-0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output Power Dissipation	P_O		250	mW	3
Input Power Dissipation	P_I		45	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Table 4.Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	V_{CC} - V_{EE}	10	30	V	
Input Current (ON)	$I_{F(ON)}$	7	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	
Operating Temperature	T_A	- 40	100	°C	

Table 5. Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.15			A	$V_O = V_{CC}$ - 4		5
		0.2	0.3		A	$V_O = V_{CC}$ - 10	2	2
Low Level Output Current	I_{OL}	0.15			A	$V_O = V_{EE}$ + 2.5		5
		0.2	0.3		A	$V_O = V_{EE}$ + 10	4	2
High Level Output Voltage	V_{OH}	V_{CC}-4	V_{CC}-1.8		V	I_O = -100 mA	1	6, 7
Low Level Output Voltage	V_{OL}		0.4	1	V	I_O = 100 mA	3	
High Level Supply Current	I_{CCH}		0.7	3	mA	I_O = 0 mA	5, 6	14
Low Level Supply Current	I_{CCL}		1.2	3	mA	I_O = 0 mA	5, 6	14
Threshold Input Current Low to High	I_{FLH}			6	mA	I_O = 0 mA, V_O > 5 V	7, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V	I_O = 0 mA, V_O > 5 V		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	14	
Temperature Coefficient ofInput Forward Voltage	DV_F/DT_A		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	R_g = 75W, C_g = 1.5 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 7 mA, V_{CC} = 30 V	8, 9, 10, 11, 12, 15	13
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	µs			13
Propagation Delay Di□erence Between Any Two Parts or Channels	PDD	-0.5		0.5	µs			10
Rise Time	t_R		50		ns			
Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	10			kV/µs	T_A = 25°C, V_{CM} = 1000 V	16	11
Output Low Level CommonMode Transient Immunity	$\|CM_L\|$	10			kV/µs		16	12

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			V_{rms}	T_A = 25°C, RH < 50% for 1 min.		8, 9
Input-Output Resistance	R_{I-O}		10^{12}			V_{I-O} = 500 V		9
Input-Output Capacitance	C_{I-O}		0.6		pF	Freq=1 MHz		

Notes:

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µ

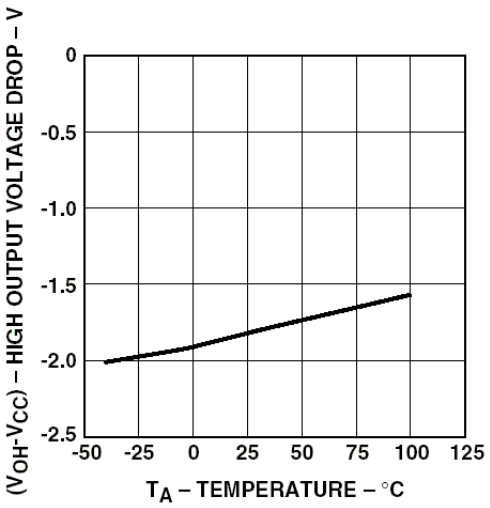


Figure 1. V_{OH} vs. Temperature.

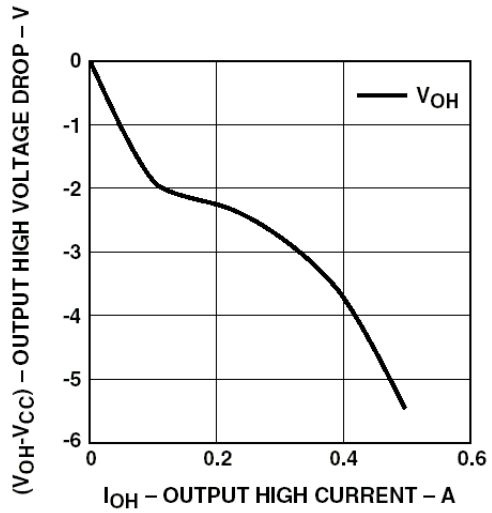


Figure 2. V_{OH} vs. I_{OH}.

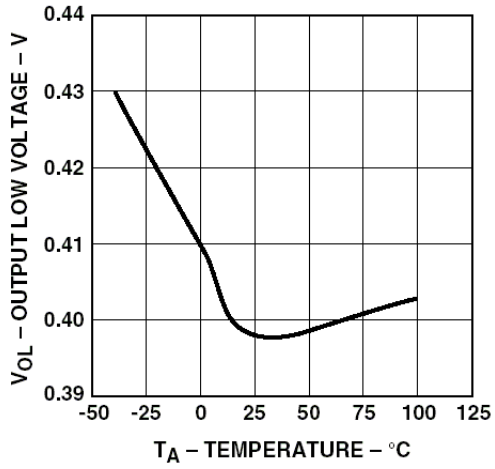


Figure 3. V_{OL} vs. Temperature.

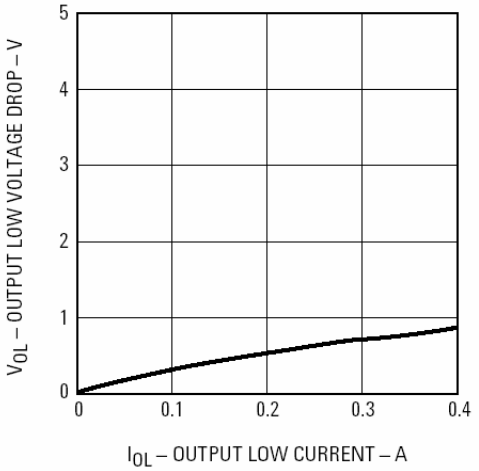


Figure 4. V_{OL} vs. I_{OL}.

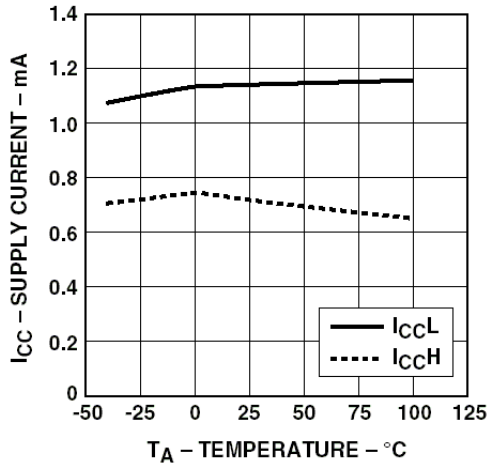


Figure 5. I_{CC} vs. Temperature.

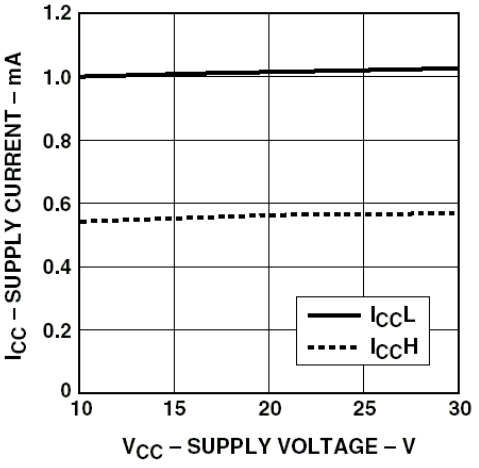


Figure 6. I_{CC} vs. V_{CC}.

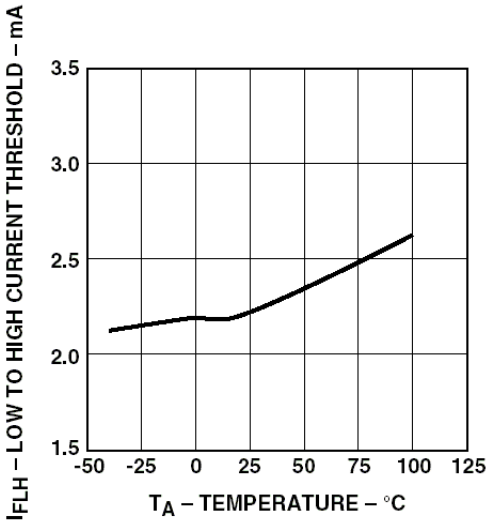


Figure 7. I_{FLH} vs. Temperature.

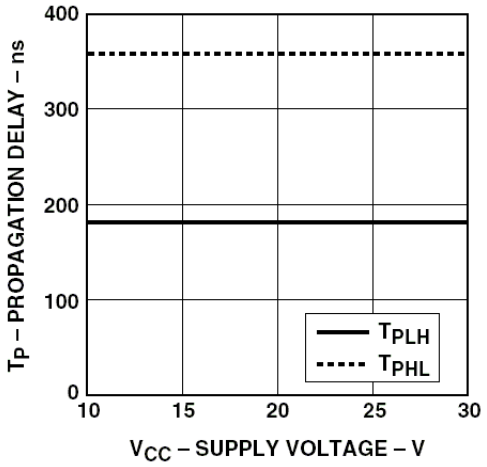


Figure 8. Propagation delay vs. V_{CC}.

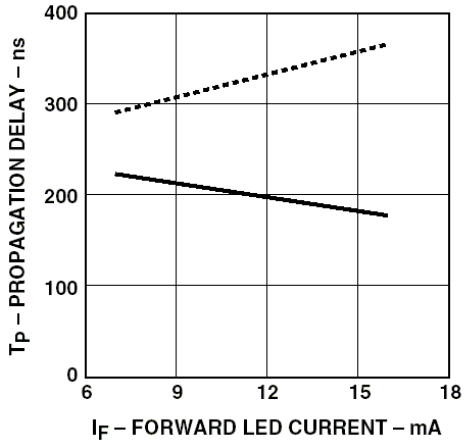


Figure 9. Propagation Delay vs. I_F.

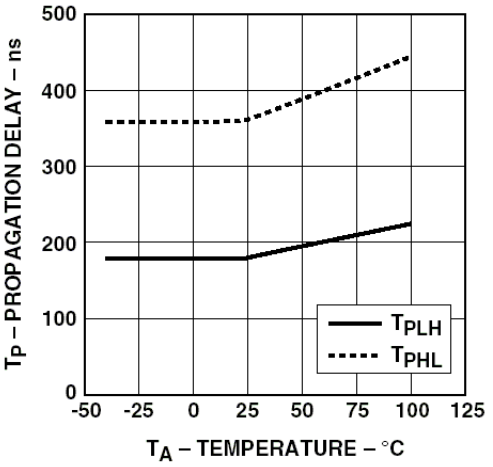


Figure 10. Propagation Delay vs. Temperature.

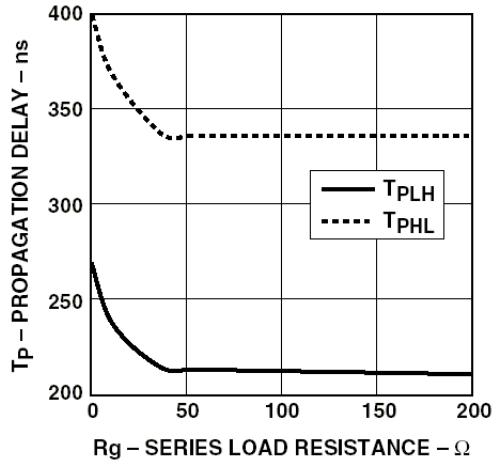


Figure 11. Propagation Delay vs. R_g.

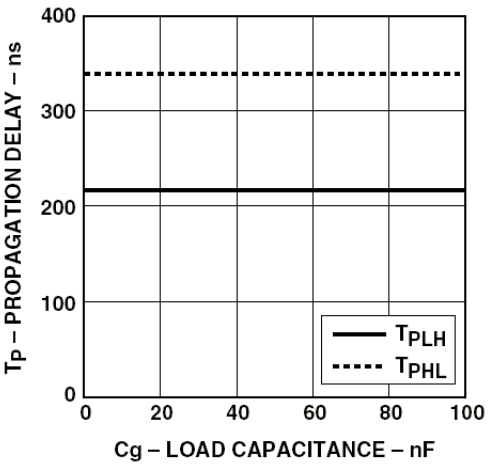


Figure 12. Propagation Delay vs. C_g.

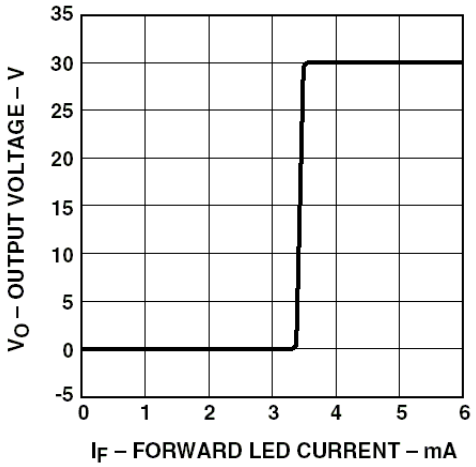


Figure 13. Transfer characteristics.

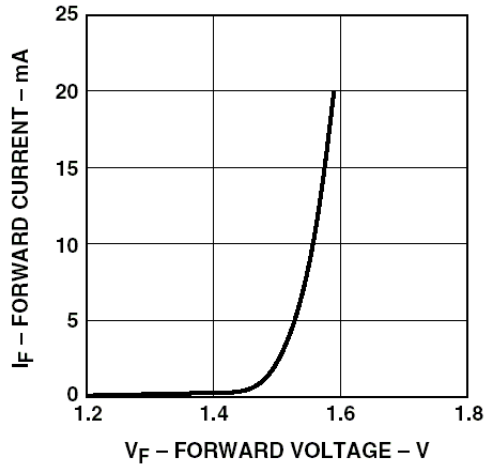


Figure 14. Input Current vs. Forward Voltage.

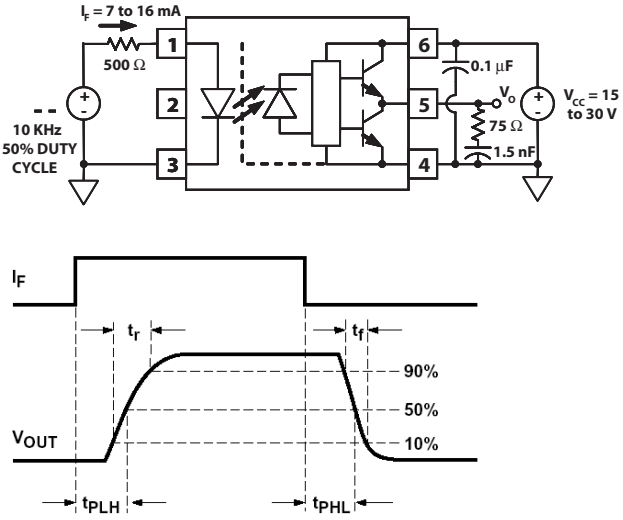


Figure 15. Propagation Delay Test Circuit and Waveforms.

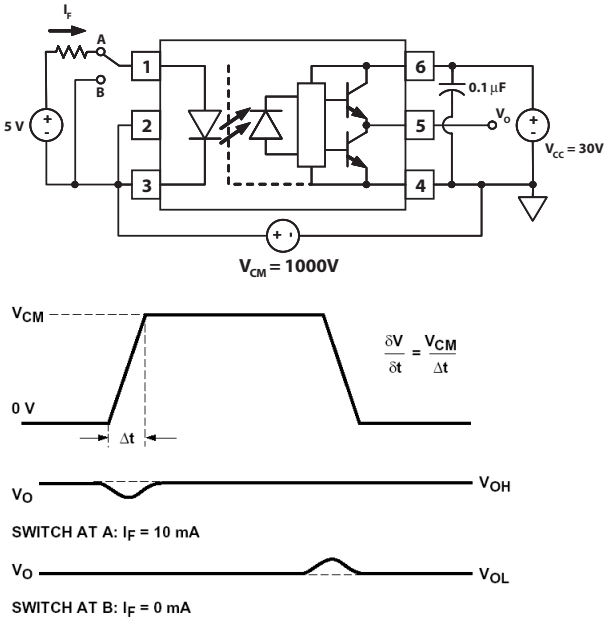


Figure 16. CMR Test Circuit and Waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT □rmly o□, the ACPL-P302/W302 has a very low maximum V_{OL} speci□cation of 1.0 V. Minimizing R_g and the lead inductance from the ACPL-P302/W302 to the IGBT gate and emitter (possibly by mounting the ACPL-P302/W302 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 17. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the ACPL-P302/W302 input as this can result in unwanted coupling of transient signals into the input of ACPL-P302/W302 and degrade performance. (If the IGBT drain must be routed near the ACPL-P302/W302 input, then the LED should be reverse biased when in the o□ state, to prevent the transient signals coupled from the IGBT drain from turning on the ACPL-P302/W302.

Selecting the Gate Resistor (Rg)

Step 1: Calculate R_g minimum from the I_{OL} peak speci□cation. The IGBT and R_g in Figure 17 can be analyzed as a simple RC circuit with a voltage supplied by the ACPL-P302/W302.

$$R_g \geq \frac{V_c - V_o}{I_{OLPEAK}}$$
$$= \frac{2 - 1}{0.4}$$
$$= 57.5\Omega$$

The V_{OL} value of 1 V in the previous equation is the V_{OL} at the peak current of 0.4A. (See Figure 4).

Step 2: Check the ACPL-P302/W302 power dissipation and increase R_g if necessary. The ACPL-P302/W302 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

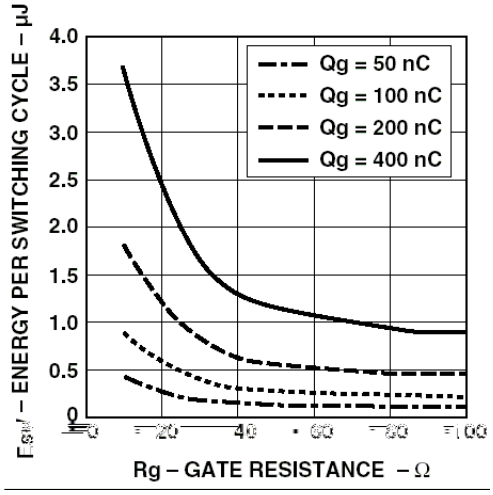


Figure 18. Energy Dissipated in the ACPL-P302/W302 and for Each IGBT Switching Cycle.

$$P_T = P_E + P_O$$
$$P_E = I_F \bullet V_F \bullet DutyCycle$$
$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_c \bullet V_c + E_{SW}(R_g; Q_g) \bullet f$$
$$= (I_{CCBIAS} + K_{ICC} \bullet Q_g \bullet f) \bullet V_c + E_{SW}(R_g; Q_g) \bullet f$$

where $K_{ICC} \cdot Q_g \cdot f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 17 with I_F (worst case) = 10 mA, R_g = 57.5 W, Max Duty Cycle = 80%, Q_g = 100 nC, f = 20 kHz and T_{AMAX} = 85°C:

$$P_E = 10mA \bullet 1.8V \bullet 0.8 = 14mW$$
$$P_O = (3mA + (0.001mA/\Omega \bullet kHz) \bullet 20kHz \bullet 100nC) \bullet 24V +$$
$$0.3\Omega \bullet 20kHz = 126mW \leq 250mW (P_{O(MAX)}@85°C)$$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, R_g = 57.5 W is alright for the power dissipation.

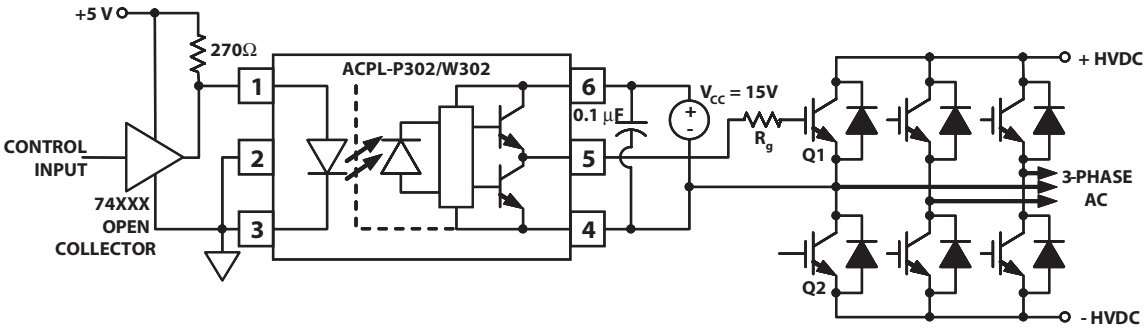


Figure 17. Recommended LED Drive and Application Circuit for ACPL-P302/W302

LED Drive Circuit Cor
formance

Without a detector
pler CMR failure is
of the optocoupler
IC as shown in Fig
CMR performance
transparent Farad
coupled current a
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between the LE
Figure 20. This c
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becomes the m
optocoupler. Th
LED drive circu
state (on or o
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Techniques t
cussed in the

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vi

Equivalent Circuit for Figure 15 D

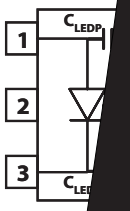


Figure 19. Op
onshielded Optocou-
plers.

Figur
t to Output Capacitance Model for Shielded Optocouplers.

he open collector drive circu
not keep the LED o during a +
the current owing through C_{LED}
LED, and it is not recommended
ultra high CMR_L performance. Th
which like the recommended ap
17), does achieve ultra high CMR pe
the LED in the o state.

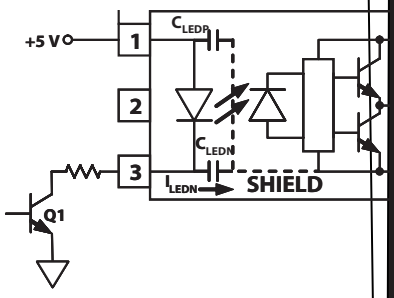


Figure 22. Not Recommended Open Collector Drive C

C ne LED On (CMR_H)

MR LED drive circuit must keep the LED on during
on mode transients. This is achieved by overdriving
ED current beyond the input threshold so that it is not
lled below the threshold during a transient. A minimum
ED current of 7 mA provides adequate margin over the
maximum I_{FLH} of 5 mA to achieve 10 kV/µs CMR.

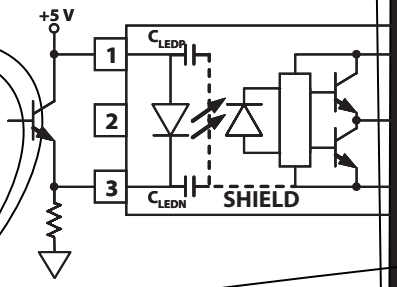
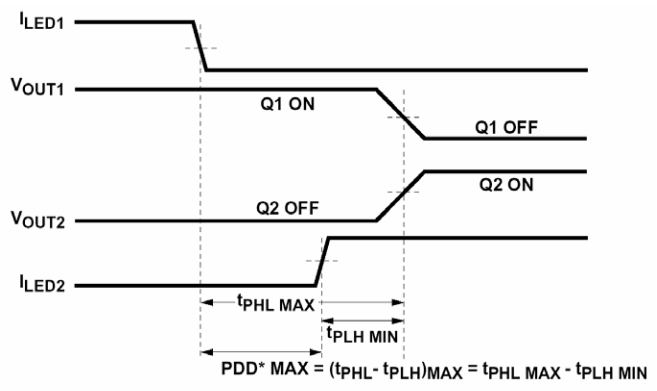


Figure 23. Recommended LED Drive Circuit for Ultra-
gation Delay Specifications.

Dead Time and Propagation Delay Specifications

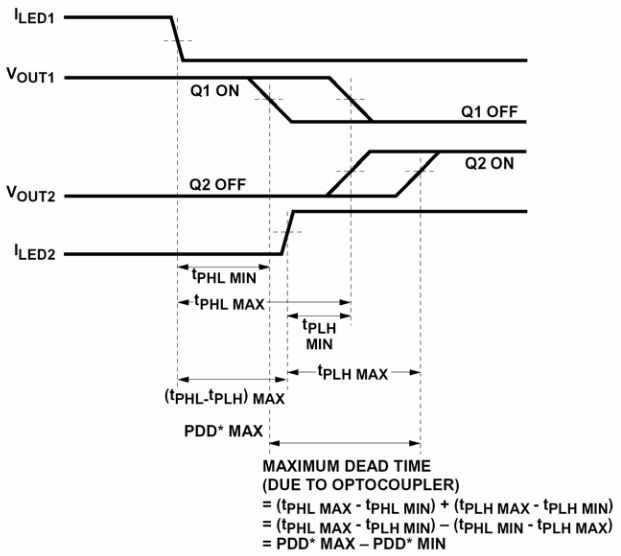
The ACPL-P302/W302 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of -40° to 100°C.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 24. Minimum LED Skew for Zero Dead Time.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 25. The maximum dead time for the ACPL-P302/W302 is 1 µs (= 0.5 µs - (-0.5 µs)) over the operating temperature range of –40°C to 100°C.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 25. Waveforms for Dead Time.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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