PRODUCT SPECIFICATION T-49-19-07

Z86E30
CMOS Z8 OTP CCP™ MICROCONTROLLER

FEATURES

- 8-bit CMOS microcomputer, 28-pin DIP
- Low cost
- 4.5 to 5.5 volt operating range
- Software programmable low EMI mode
- Pull-Up Active/Open Drain programmable on Ports 0 and 2
- EPROM protect programmable
- RAM protect programmable
- RC oscillator programmable
- Low power consumption - 60 mW
- Fast instruction pointer - 0.6 microseconds
- Two standby modes - STOP and HALT
- 24 input/output lines
- All digital inputs, CMOS levels, Schmitt triggered
- 4 Kbytes of one-time PROM
- 236 bytes of RAM
- Three Expanded Register File control re
- Two programmable 8-bit Counter/Timer 6-bit programmable prescaler.
- Six vectored, priority interrupts from six diff
- Clock speeds up to 12 MHz
- Watchdog Timer
- Auto Power-On Reset
- Two Comparators
- On-chip oscillator that accepts a crys resonator, LC, RC or external clock driv

GENERAL DESCRIPTION

The Z86E30 CCP (Consumer Controller Processor) introduces the next level of sophistication to single-chip architecture. The Z86E30 is a member of the Z8 single-chip microcontroller family with 4 Kbytes of EPROM and 236 bytes of RAM. The device is housed in a 28-pin DIP, and is manufactured in CMOS technology. The device offers easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

The Z86E30 architecture is characterized by Zilog's 8-bit microcontroller core with an expanded register file to allow easy access to register mapped peripheral cuits. The CCP offers a flexible I/O scheme register and address space structure, and ancillary features that are useful in many in volume, automotive, peripheral types, and a entific applications.

The device applications demand powerful I/O The CCP fulfills this with 24 pins dedicated output. These lines are grouped into three por per port, and are configurable under softwa provide timing, status signals, and paralle without handshake.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (ERF). The Register File is composed of 236 bytes of general-purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of three control resisters.

To unburden the program from coping with the real-time problems such as counting/timing and input/output data communication, the Z86E30 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figures 1 and 2).

Note: All Signals with a preceding front slash "/", are active Low, e.g.: B//W (Word is active Low); /B/W (BYTE is active Low, only).

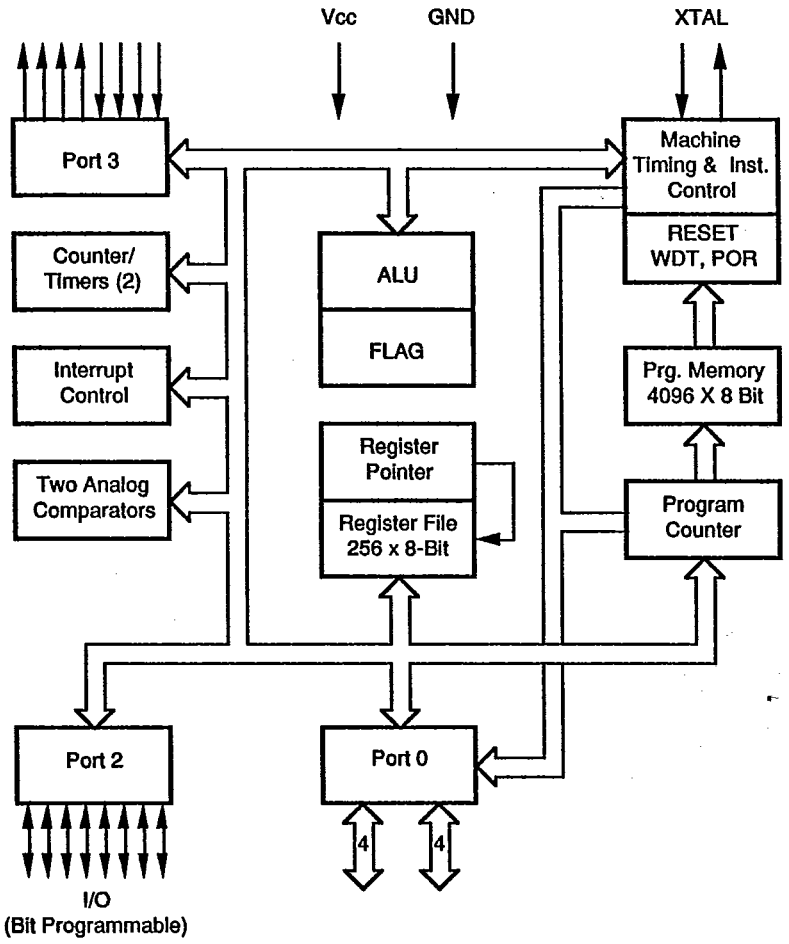

Figure 1. Functional Block Diagram

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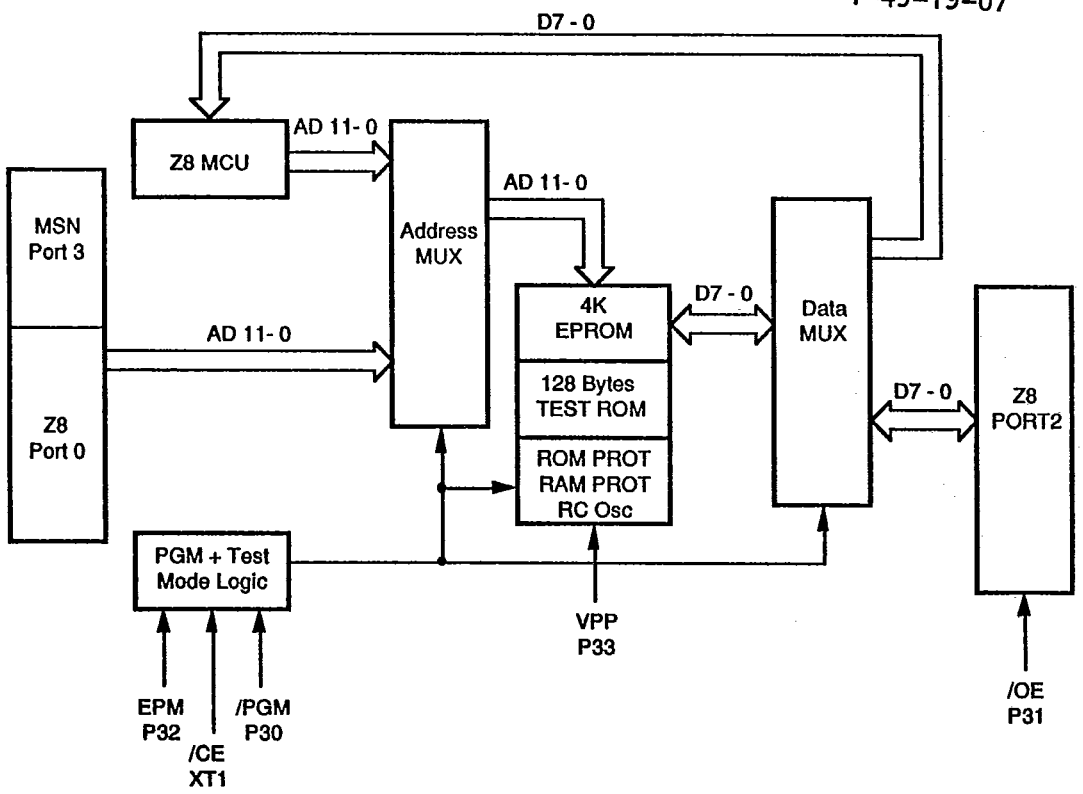

Figure 2. EPROM Programming Block Diagram

PIN DESCRIPTION

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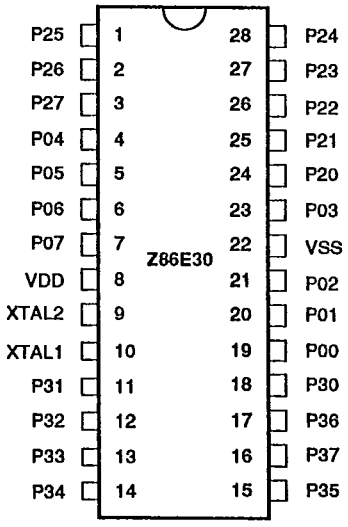
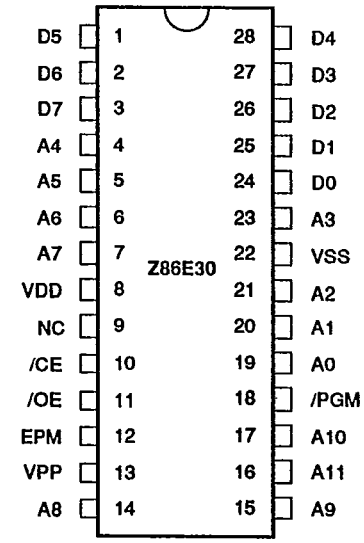


Figure 3. Z86E30 Standard Mode Pin Configuration

Table 1. Z86E30 Standard Mode

Pin #	Symbol	Function	Direction
1-3	P25-7	Port 2 pin 5,6,7	In/Output
4-7	P04-7	Port 0 pin 4,5,6,7	In/Output
8	V_{DD}	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-3	Port 3 pin 1,2,3	Input
14-15	P34-5	Port 3 pin 4,5	Output
16	P37	Port 3 pin 7	Output
17	P36	Port 3 pin 6	Output
18	P30	Port 3 pin 0	Input
19-21	P00-2	Port 0 pin 0,1,2	In/Output
22	V_{ss}	Ground	Input
23	P03	Port 0 pin 3	In/Output
24-28	P20-4	Port 2 pin 0,1,2,3,4	In/Output



Z86E30 EPROM Programming Mode

Figure 4. Z86E30 EPROM Programming Mode Pin Configuration

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-3	D5-7	Data 5,6,7	In/Output
4-7	A4-7	Address 4,5,6,7	Input
8	V_{DD}	Power Supply	Input
9	N/C	No connection	
10	/CE	Chip Select	Input
11	/OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-15	A8-9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	/PGM	Prog. Mode	Input
19-21	A0-2	Address 0,1,2	Input
22	V_{ss}	Ground	Input
23	A3	Address 3	Input
24-28	D0-4	Data 0,1,2,3,4	In/Output

Note: Power connections follow Conventional descriptions below

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PIN FUNCTIONS

EPROM Programming Mode

D7-D0. *Data Bus.* The data can be read from or written to the EPROM through the data bus.

A11-A0. *Address Bus.* During programming, the EPROM address is written to the address bus.

V_{CC}. *Power Supply.* This pin has to supply 5V during the EPROM read mode and 6V during other modes.

/CE. *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE. *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is low, the Data Bus is output. When high, the Data Bus is input.

EPM. *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP}. *Program Voltage.* This pin supplies the program voltage.

/PGM. *Program Mode* (active Low). When this pin is low, the data is programmed to the EPROM through the Data Bus.

Z86E30 Standard Mode

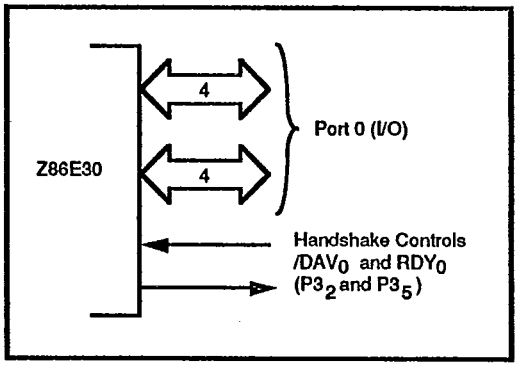
XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network or external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P00-P03 input/output and P04-P07 input/output, separately. The input buffers are Schmitt triggered and nibbles programmed as outputs can be globally programmed as either push-pull or open drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a handshake I/O port.

In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 5).

PIN FUNCTIONS (Continued)



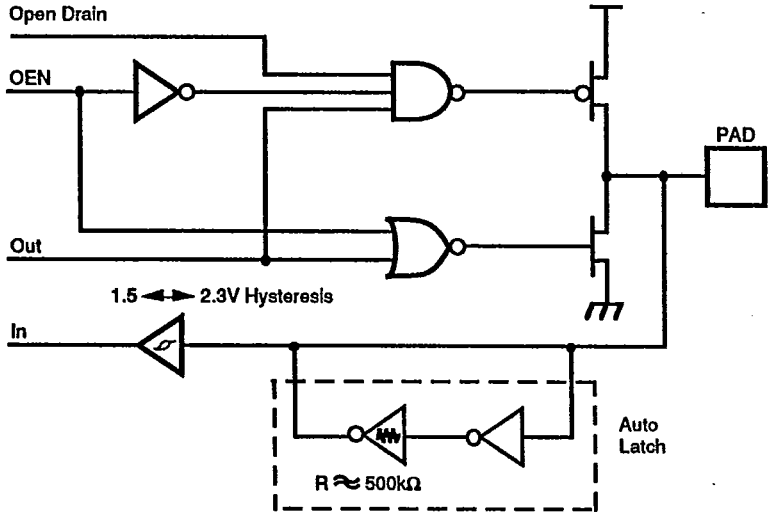


Figure 5. Port 0 Configuration

Port 2 (P20-P27). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt triggered. Bits programmed as outputs can be globally programmed as either push-pull or open drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 6).

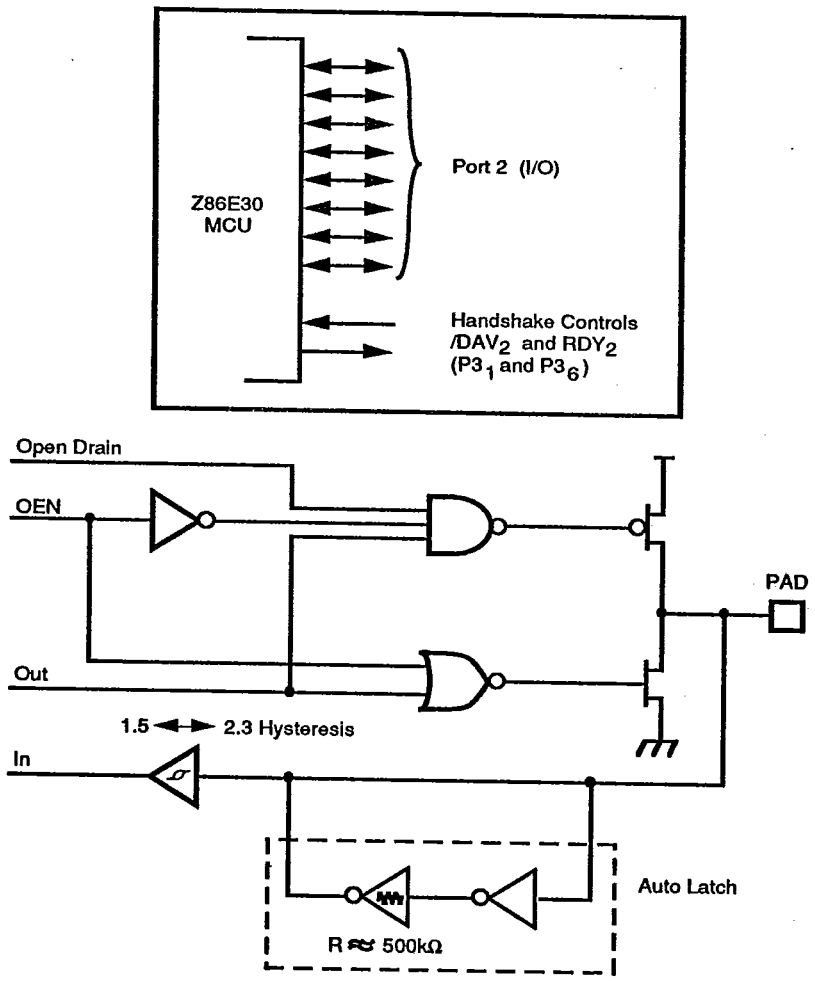


Figure 6. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P30-P37). Port 3 is an 8-bit, CMOS compatible port with four fixed inputs and four fixed outputs. Port 3 consists of four fixed inputs (P30-P33) and four fixed outputs (P34-P37), and can be configured under software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt triggered. Pins P31, P32 and P33 are standard CMOS inputs (no Auto-Latches) and Pins P34, P35, P36 and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33.

The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edge triggered interrupt inputs (Figure 7). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are also available on Port 3 (Table 3).

Note: P30-P33 inputs differ from the Z86C30 because there is no clamping diode to V_{CC} due to the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

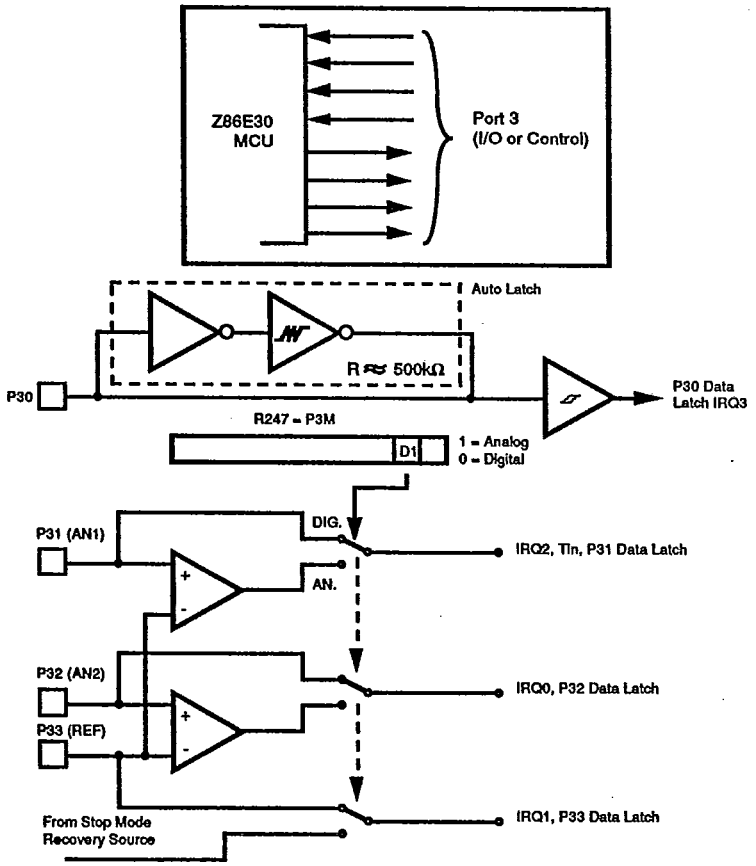


Figure 7. Port 3 Configuration

Table 3. Pin Assignments of Port 3

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT					
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D
P37	OUT					

Comparator Inputs. Port 3, pins P31 and P32 each have a comparator front end. The comparator reference voltage (Pin P33) is common to both comparators. In analog mode, P31 and P32 are the positive inputs of the comparators and P33 is the reference voltage of the comparators.

Auto-Latch. The Auto-Latch puts valid CMOS levels on all CMOS inputs (except P31-P33) that are not externally driven. Whether this is zero or one, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Low EMI Emission. The Z86E30 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- Less than 1.5 mA (typical) current consumption during HALT mode.
- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 ohms (typical).
- Oscillator divide-by-two circuitry is eliminated.
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.

FUNCTIONAL DESCRIPTION

The Z8 CCP incorporates special functions to enhance the Z8's applications in industrial, scientific research, and advanced technologies.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP Mode Recovery Source

Having the Auto Power-on Reset circuitry built in, the Z86E30 does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles. The Z86E30 does not re-Initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP Mode Recovery operation.

Program Memory. The Z86E30 can address up to 4 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Address 12 (000CH) to address 4095 (0FFFH) are reserved for the user program. After reset, the program counter points at the address 000CH which is the starting address of the user program.

FUNCTIONAL DESCRIPTION (Continued)

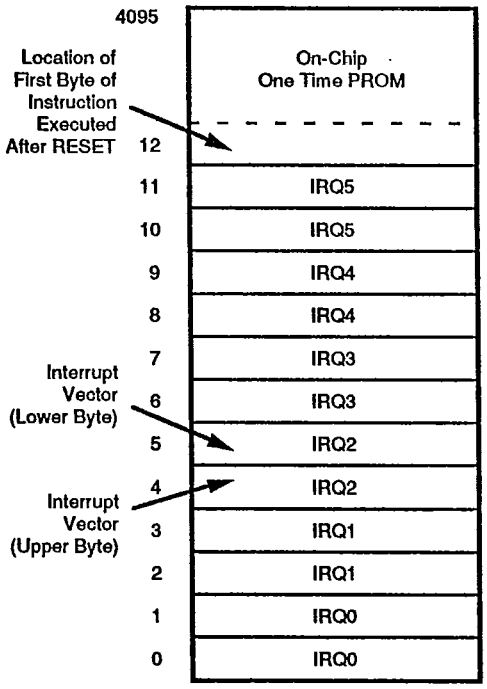


Figure 8. Program Memory Map

EPROM Protect. The 4 Kbytes program memory is a one time PROM. An EPROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions (LDE and LDEI instructions are not available in Z86E30) to program memory in all modes. In EPROM protect mode, the instructions of LDC and LDCI are disabled.

Expanded Register File. The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices, and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 9). These register groups are known as the ERF (Expanded Register File). The low nibble (D0-D3) of the Register Pointer (RP) selects the active ERF group, and the high nibble (D4-D7) of register RP selects the working register group (Figure 10).

Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

Register File. The 256 byte register file consists of 3 I/O port registers, 236 general-purpose registers, and 15 control and status registers (R3 and R240 are reserved), and three system configuration registers in the expanded register group (Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figures 10, 11). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0H-EFH can only be accessed through working registers and indirect addressing modes.

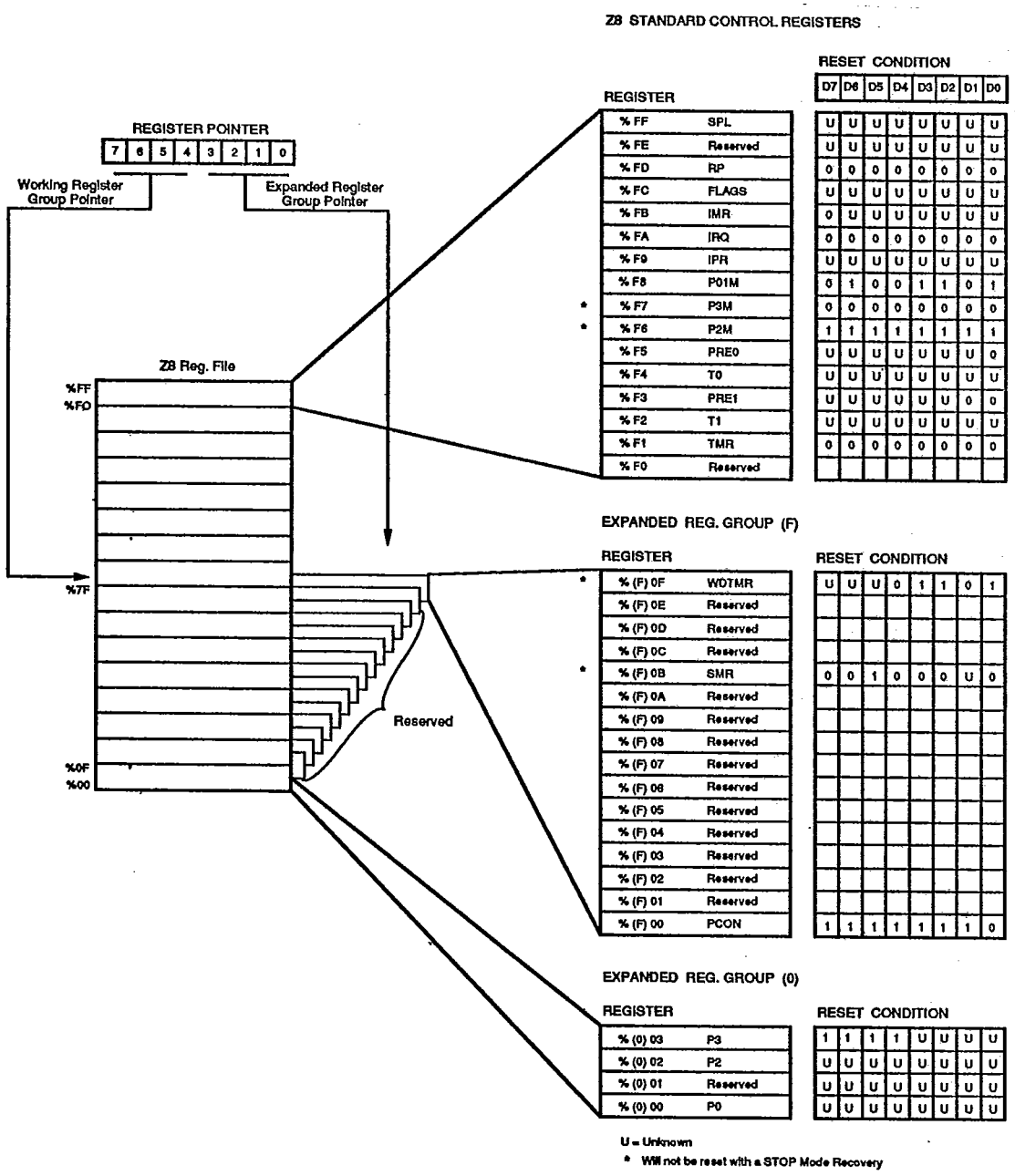


Figure 9. Expanded Register File Architecture

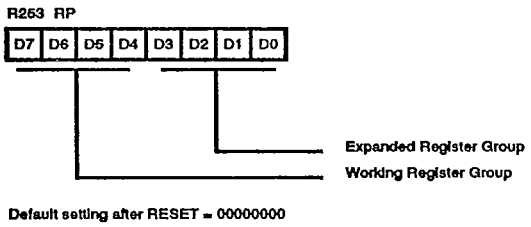


Figure 10. Register Pointer Register

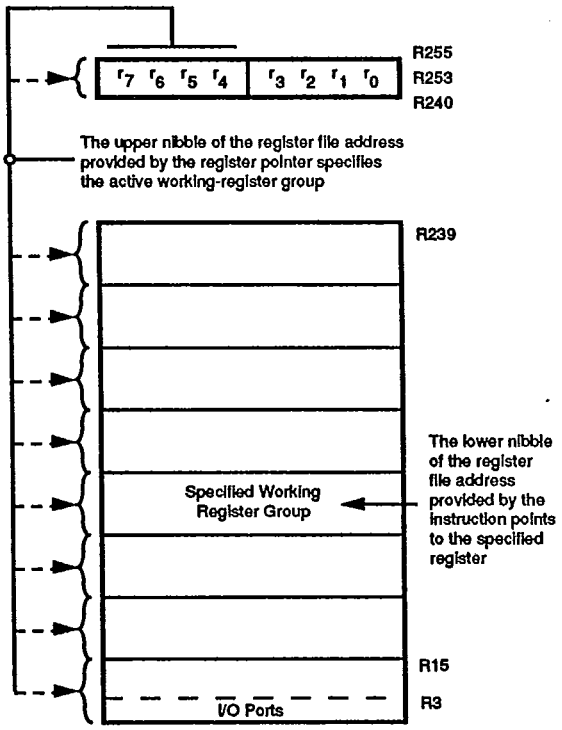


Figure 11. Register Pointer

RAM Protect. The upper portion of the RAM's address space 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected in EPROM Programming Mode. D6 of the IMR Control Register (R251) is used to turn on or turn off the RAM protect. The RAM protect is turned on by setting the D6 of the IMR Control Register (D6=1) and turned off by resetting this bit (D6=0).

Stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 256 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 12).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request-IRQ4 (T0) or IRQ5 (T1) is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that can be retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

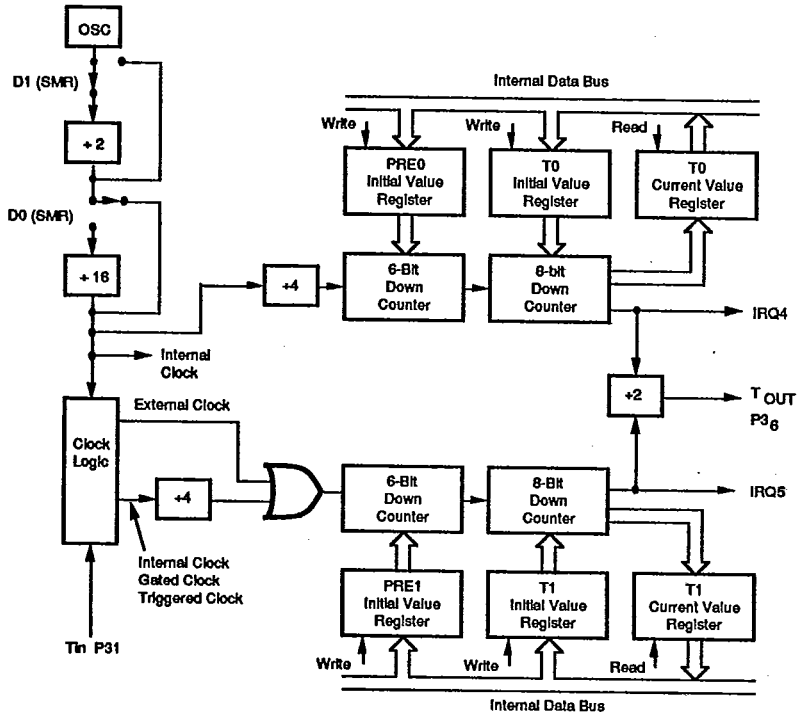


Figure 12. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

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Interrupts. The Z86E30 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 13). The six sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

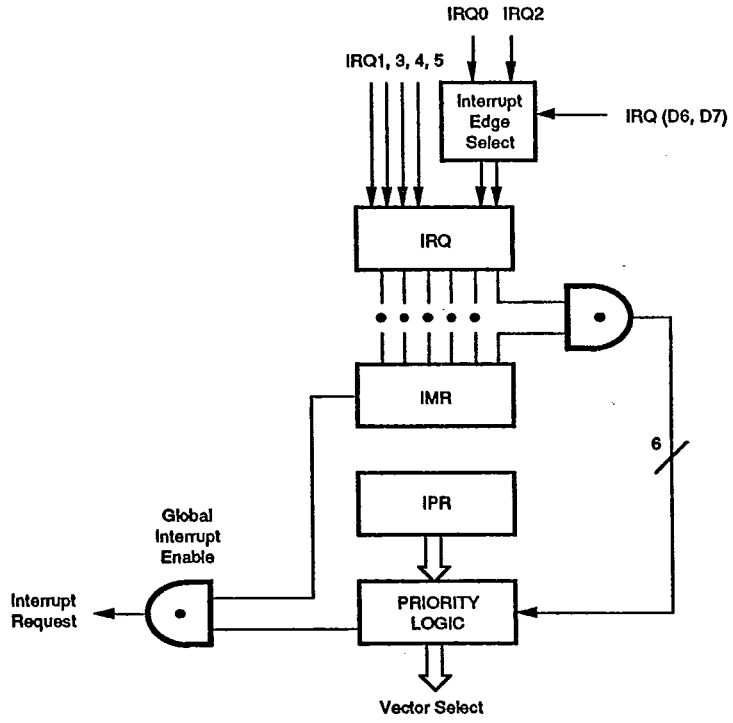

Figure 13. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	/DAV 0, IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	/DAV 2, IRQ 2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ 3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ 4	T0	8, 9	Internal
IRQ 5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E30 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 5.

Table 5. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F=Falling Edge
R=Rising Edge

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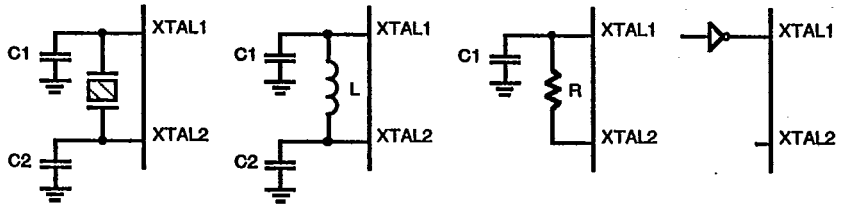
Clock. The Z86E30 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF to 100 pF) from each pin to ground. The RC oscillator option is selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 14).

Note: RC OSC may not reach to 12 MHz



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V VCC (TYP)

C1 = 33 pF *
R = 1k *
f = 6.6 MHz *

External Clock

* Typical value including pin parasitics

Figure 14. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power bad to Power OK status
2. STOP mode recovery (if D5 of SMR=0)
3. WDT timeout

The POR time is a nominal 5 ms. Bit 5 of the Stop Mode Register (SMR) determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The Stop mode is terminated by one of the following resets: WDT timeout, POR, or Stop Mode Recovery Source which is defined by SMR register . This causes the processor to restart the application program at address 000C (HEX). In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP instruction (opcode=FFH) immediately before the appropriate sleep instruction. For example:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

Port Configuration Register (PCON). The PORT Configuration Register (PCON) configures the port's individually for comparator output on Port 3, Open Drain on Port 0, low EMI noise on Port's 0, 2, and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 15).

Note: PCON is not available in Z86C30

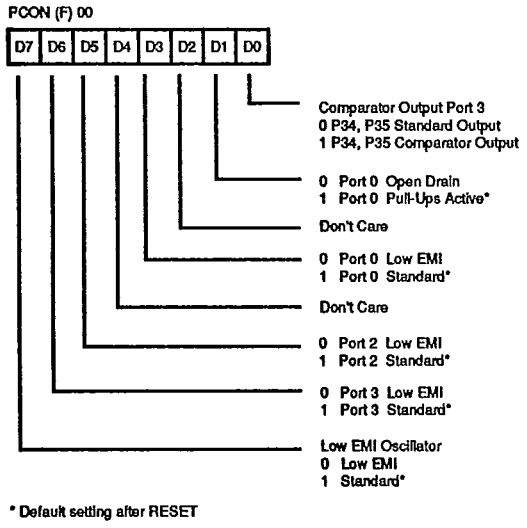


Figure 15. Port Configuration Register (PCON)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 and a 0 releases the Port to its standard I/O configuration.

Port 0 Open Drain (D1). Port 0 is configured as an Open-drain by resetting this bit (D1 = 0) and configured as Pull-up Active by setting D1 = 1. The default value is 1.

Low EMI Port 0 (D3). Port 0 is configured as a Low EMI Port by resetting this bit (D3 =0) and configured as a Standard Port by setting D3 =1. The default value is 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5 = 0) and configured as a Standard Port by setting D5 = 1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6 = 0) and configured as a Standard Port by setting D6 = 1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive.

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Stop Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 16). All bits are Write only except Bit 7 which is a Read only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the STOP Mode Recovery Source. (Table 7). The SMR is located in Bank F of the Expanded Register Group at address 0BH.

SMR (F) 0B

D7	D6	D5	D4	D3	D2	D1	D0

D0 — SCLK/TCLK Divide by 16
0 OFF *
1 ON

D1 — External Clock Divide by 2
0 SCLK/TCLK =XTAL/2*
1 SCLK/TCLK =XTAL

D2, D3, D4 — Stop Mode Recovery Source
000 POR Only *
001 P30
010 P31
011 P32
100 P33
101 P27
110 P2 NOR 0:3
111 P2 NOR 0:7

D5 — Stop Delay
0 OFF
1 ON*

D6 — Stop Recovery Level
0 Low *
1 High

D7 — Stop Flag
0 POR*
1 Stop Recovery

* Default setting after RESET

Figure 16. Stop Mode Recovery Register

FUNCTIONAL DESCRIPTION (Continued)

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SCLK/TCLK divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide By 2 (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI [i.e., D7 (PCON) = 0, D1 (SMR) = 1]. The default setting is 0.

STOP Mode Recovery Source (D2, D3, and D4). These 3 bits of the SMR register specify the wake-up source of the STOP Mode recovery (Figure 17). Table 6 shows the SMR source selected with the setting of D2 to D4. P31-P33 cannot be used to wake up from STOP mode when programmed as analog inputs.

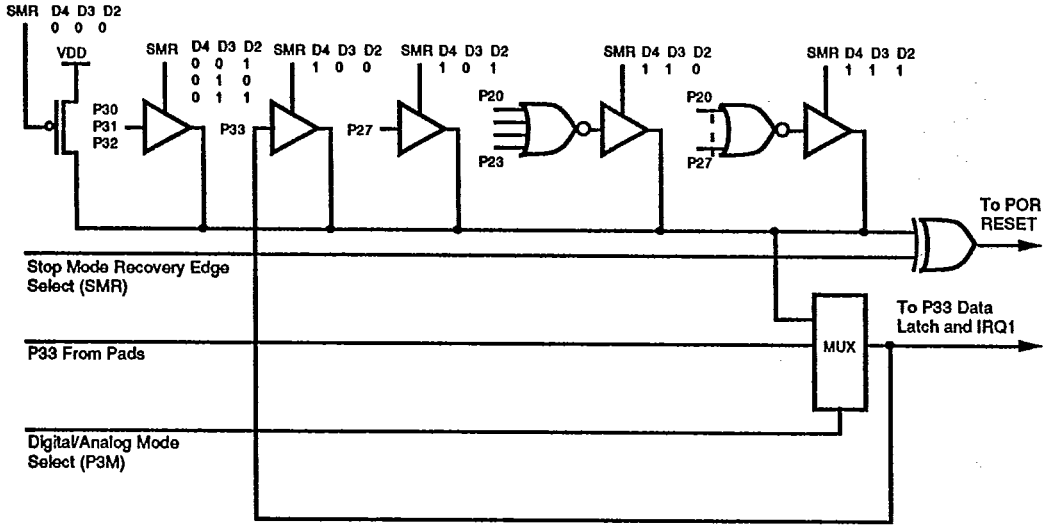

Figure 17. Stop Mode Recovery Source

Table 6. Stop Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

STOP Mode Recovery Delay Select (D5). The 5 ms RESET delay after STOP Mode Recovery is disabled by programming this bit to a zero. A1 in this bit causes a 5 ms RESET delay after STOP Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the STOP Mode Recovery source must be kept active for at least 5 TpC.

STOP Mode Recovery Level Select (D6). A 1 in this bit defines that a high level on any one of the recovery sources wakes the Z86E30 from STOP Mode. A 0 defines the low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit indicates that the device has been reset by POR (cold). A 1 in this bit indicates the device was awakened by a SMR source (warm).

Watch Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction. It is refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled when it has been enabled. The WDT is driven either by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit-4 of the WDT register.

WDT Timeout Period (D0 and D1). Bits 0 and 1 control the

WDT During the HALT Mode (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates that the WDT is active during HALT. A 0 disables the WDT in HALT mode. The default value is 1.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 disables the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select

FUNCTIONAL DESCRIPTION (Continued) T-49-19-07

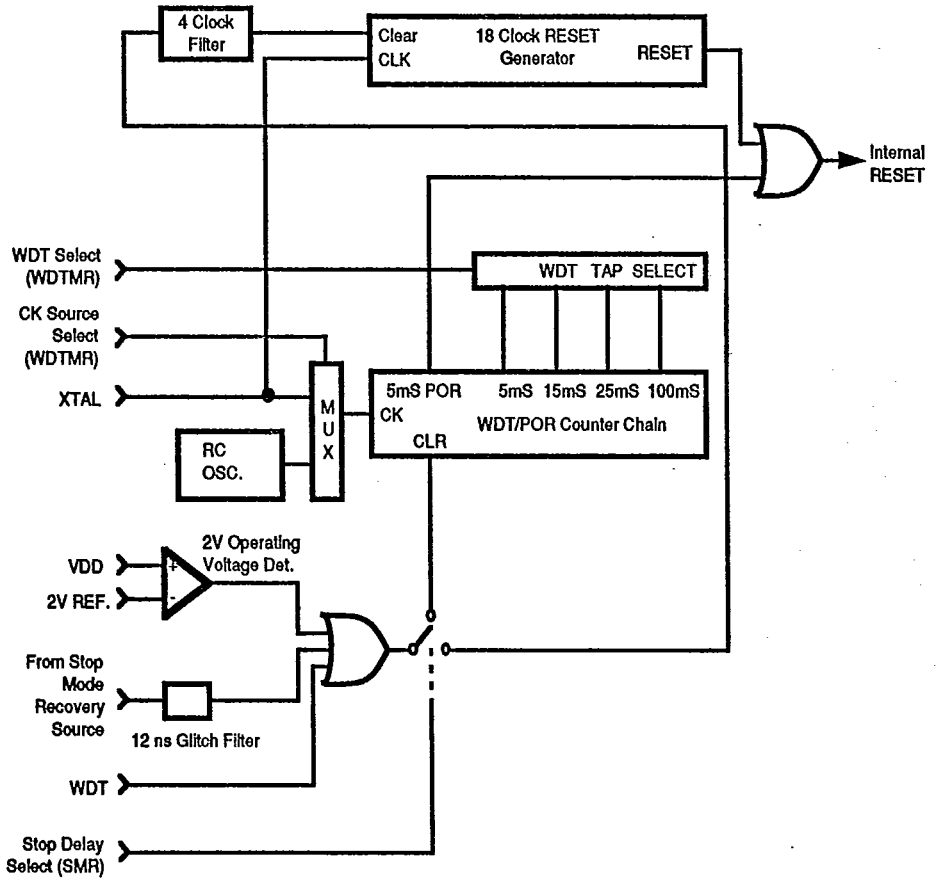

Figure 19. Resets and WDT

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Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{RST} (Auto Reset Voltage - Figure 26).

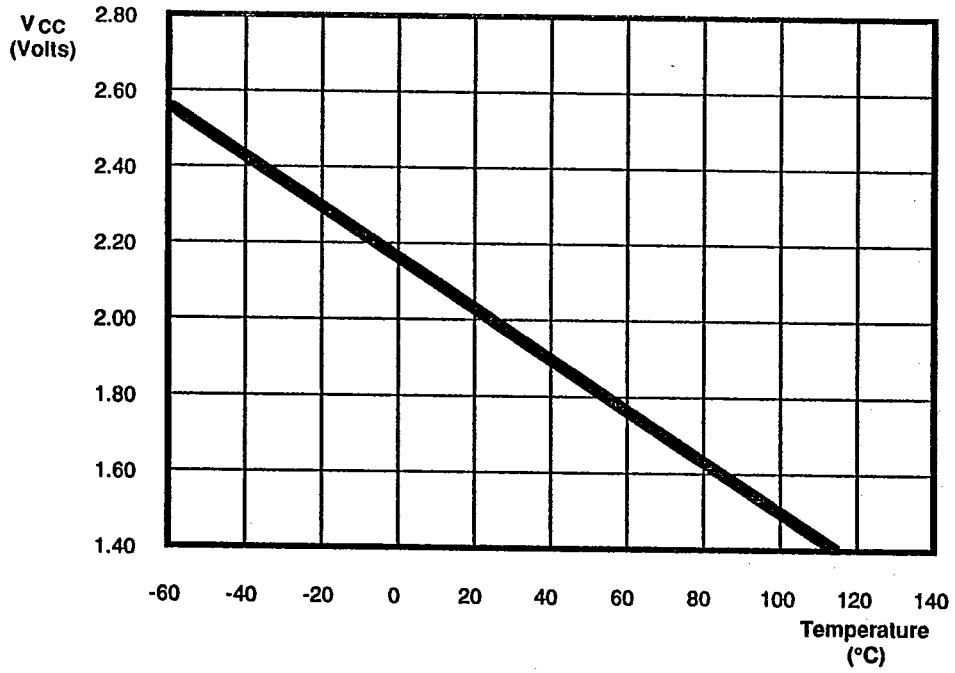

Figure 20. Typical Z86E30 V_{RST} Voltage vs. Temperature

EPROM Programming Mode

Table 8 shows the programming voltages of each programming mode. Table 9, Figures 21, 22, and 23 show the programming timing of each programming mode. Figure 24 shows the flow-chart of an Intelligent Programming Algorithm, which is compatible with a 2764A EPROM (Z86E30 is 4K EPROM, 2764A is 8K EPROM). Figure 25 shows the circuit diagram of the Z86E30 programming adaptor which adapts from 2764A to Z86E30. Since the EPROM size of Z86E30 differs from 2764A, the programming address range should be set from 0000H to 0FFFH. Otherwise, the upper 4K of data (1000H-1FFFH) will overwrite the lower 4K of data.

Table 8. EPROM Programming Table

Programming Modes	V_{PP} (P33)	EPM (P32)	/CE (XTAL1)	/OE (P31)	/PGM (P30)	ADDR	DATA (PORT2)	V_{CC}
EPROM READ	X	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	Data Out	5.0V
PROGRAM	V_{PP}	X	V_{IL}	V_{IH}	V_{IL}	Addr	Data In	6.0V
PROGRAM VERIFY	V_{PP}	X	V_{IL}	V_{IL}	V_{IH}	Addr	Data Out	6.0V
EPROM PROTECT	V_{PP}	V_H	V_H	V_{IH}	V_{IL}	X	X	6.0V
RAM PROTECT	V_{PP}	V_{IH}	V_H	V_{IL}	V_{IL}	X	X	6.0V
RC OSCILLATOR	V_{PP}	V_{IL}	V_H	V_{IH}	V_{IL}	X	X	6.0V

Notes:
V_{PP} = 12.5V ± 0.5V
V_H = 12.5V ± 0.5V
X = TTL Level (irrelevant)
V_{IH} = 5.0V
V_{IL} = 0V

Table 9. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85	78.75	ms
12	EPM Setup Time	2		µs
13	OE Setup Time	2		µs
14	Address to OE Setup Time	2		µs
15	Option Bit Program Pulse Width		78.75	ms

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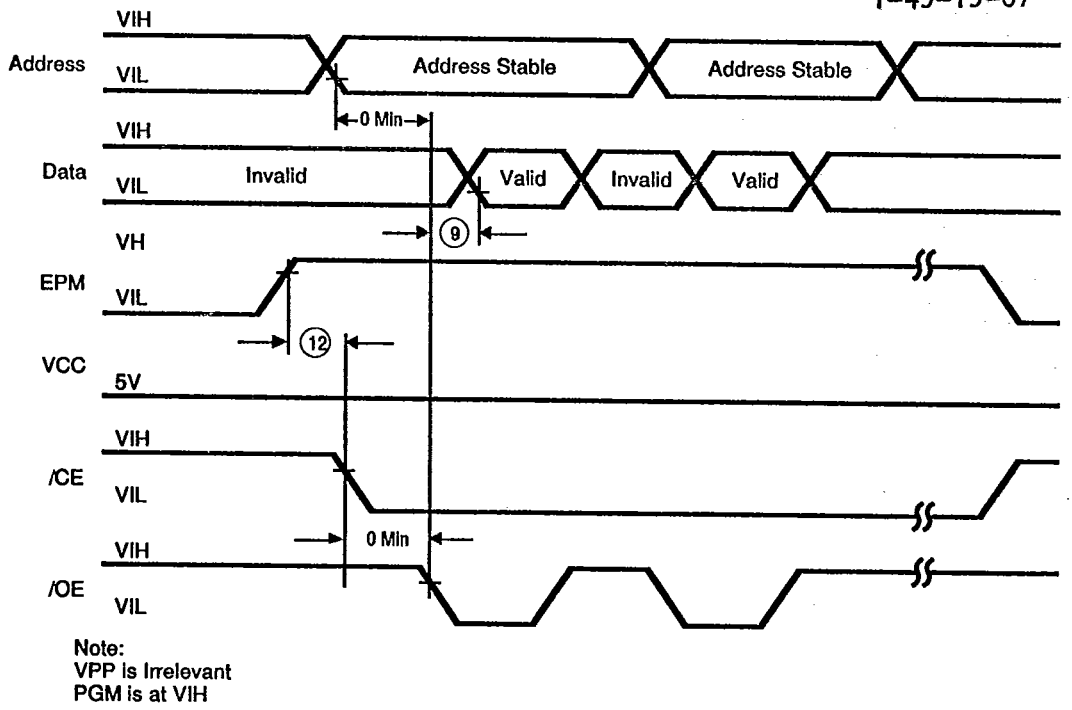

Note:
VPP is Irrelevant
PGM is at VIH

Figure 21. EPROM READ Mode Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

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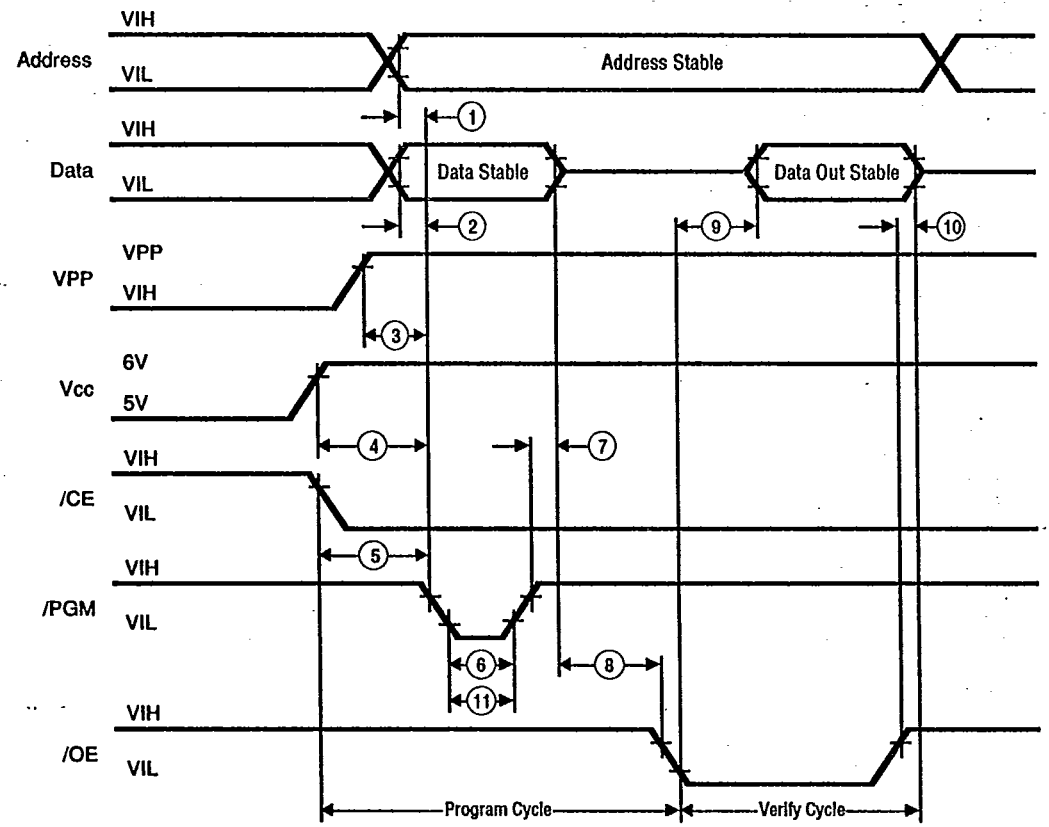

Figure 22. Timing Diagram of EPROM Program and Verify Modes

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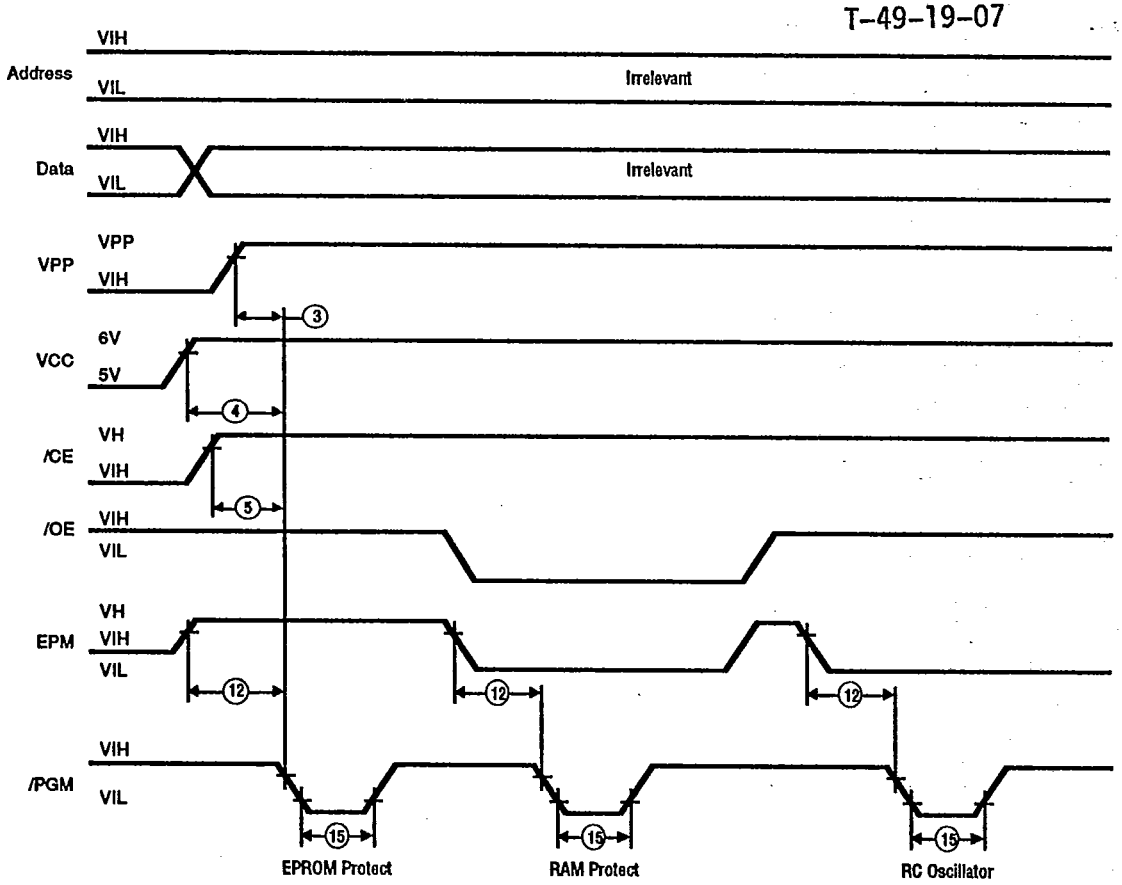

Figure 23. Timing Diagram of EPROM Protect, RAM Protect, and RC OSC Modes

FUNCTIONAL DESCRIPTION (Continued)

T-49-19-07

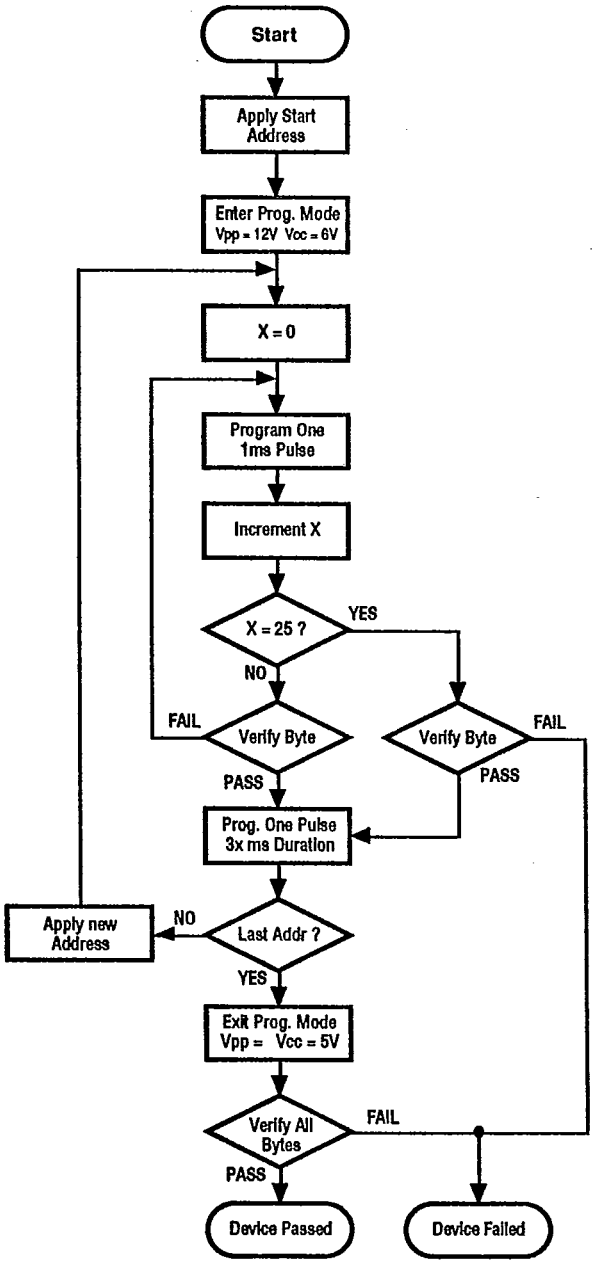

Figure 24. Z86E30 Programming Algorithm

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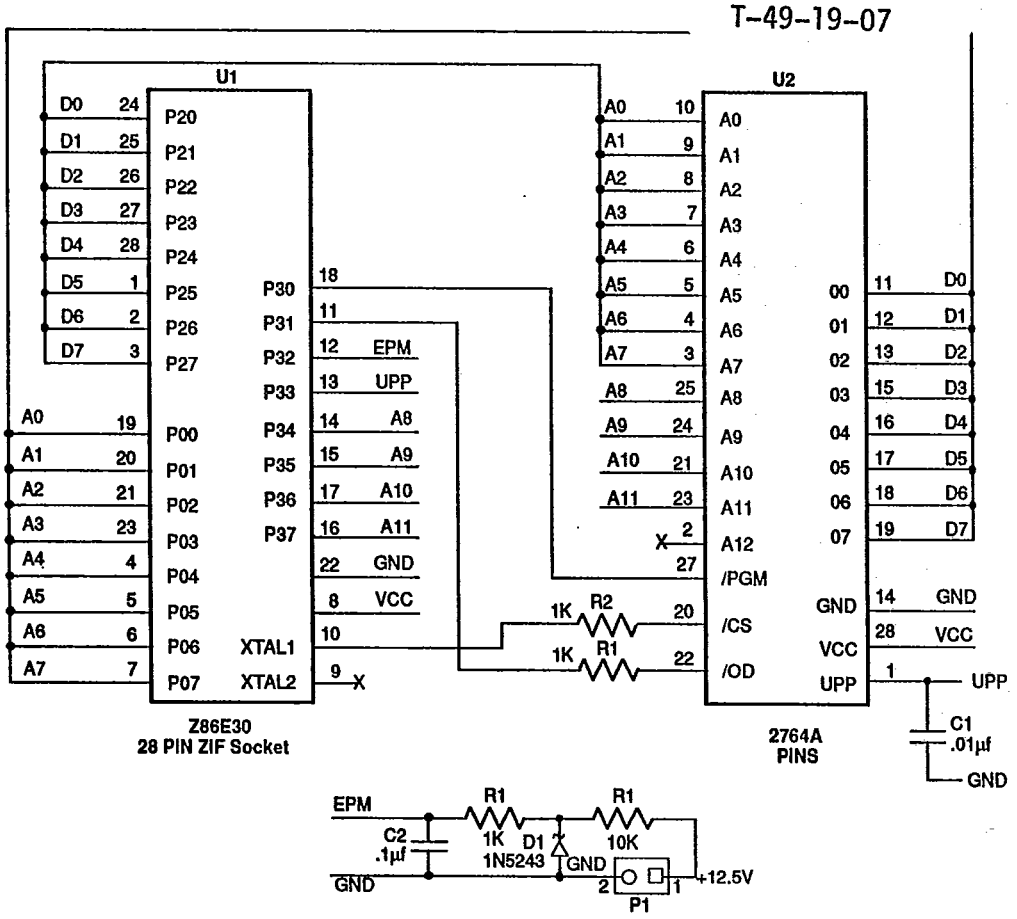

Note: The programming address has to be set to 0000H -0FFFH (lower 4K byte memory)

Figure 25. Z86E30 Programming Adaptor Circuitry

STANDARD TEST CONDITIONS

T-49-19-07

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 26)

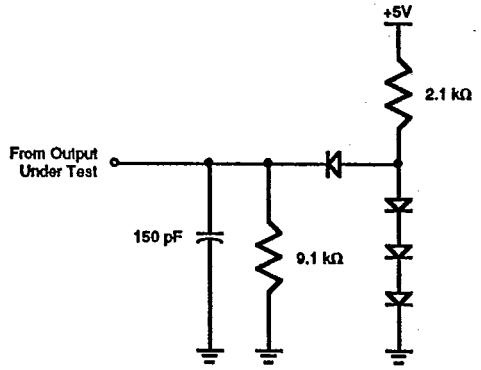

Figure 26. Test Load Configuration

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

V_{CC} SPECIFICATION

V_{CC} 5.0V ± 0.5V

DC ELECTRICAL CHARACTERISTICS

T-49-19-07

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
	Max Input Voltage	4.5V	V_{CC}+0.5V			V	250 µA	
		5.0V	V_{CC}+0.5V			V	250 µA	
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3V	3.3	V	Driven by External Clock Generator	
		5.0V	0.7 V_{CC}	V_{CC}+0.3V	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.0V	V_{SS}-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}-0.3	0.2 V_{CC}	0.7	V		
		5.0V	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltge	4.5V	V_{CC}-0.4		3.8	V	I_{OH} = -2.0 mA	
		5.0V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.2	V	I_{OH} = +4.0 mA	
		5.0V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.5	0.3	V		
		5.0V		1.5	0.3	V	I_{OL} = +12 mA, 3 Pin Max	
Reset Input High Voltage		4.5V	0.7 V_{CC}	V_{CC}+0.3	1.5	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	2.1	V		
Reset Input Low Voltage		4.5V	V_{SS}-0.3	0.2V_{CC}	1.1	V		
		5.0V	V_{SS}-0.3	0.2 V_{CC}	1.7	V		
Comparator Input Offset Voltage		4.5V		50	10	mV		
		5.0V		50	10	mV		
Input Leakage		4.5V	-10	+10	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-10	+10	<1	µA	V_{IN} = 0V, V_{CC}	
Output Leakage		4.5V	-10	+10	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-10	+10	<1	µA	V_{IN} = 0V, V_{CC}	
Reset Input Current		4.5V		50	40	µA	V_{CC} =5.0V, RV_{RL} = 0	
		5.0V		60	45	µA		
Supply Current (Standard Mode)		4.5V		12	8.5	mA	@ 8 MHz	[4,5]
		5.0V		16	15.0	mA	@ 8 MHz	[4,5]
		4.5V		15	11.5	mA	@ 12 MHz	[4,5]
		5.0V		20	18.0	mA	@ 12 MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

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Symbol	Parameter	V_{cc} Note[3]	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
I_{cc1}	Standby Current (Standard Mode)	4.5V		4.0	2.0	mA	HALT Mode V_{IN} = 0V, V_{cc} @ 8 MHz	[4,5]
		5.0V		6.0	3.5	mA	HALT Mode V_{IN} = 0V, V_{cc} @ 8 MHz	[4,5]
		4.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{cc} @ 12 MHz	[4,5]
		5.0V		7.5	4.5	mA	HALT Mode V_{IN} = 0V, V_{cc} @ 12 MHz	[4,5]
		4.5V		2.0	1.25	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.0V		3.0	1.50	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		4.5V		2.0	1.35	mA	Clock Divide by 16 @ 12 MHz	[4,5]
		5.0V		3.0	1.70	mA	Clock Divide by 16 @ 12 MHz	[4,5]
I_{cc}	Supply Current (Low EMI Mode)	4.5V		6.0	4.0	mA	@ 2 MHz	[4,5]
		5.0V		7.5	5.0	mA	@ 2 MHz	[4,5]
		4.5V		9.5	6.0	mA	@ 4 MHz	[4,5]
		5.0V		12.0	8.0	mA	@ 4 MHz	[4,5]
I_{cc1}	Standby Current (Low EMI Mode)	4.5V		1.6	0.8	mA	@ 2 MHz	[4,5]
		5.0V		2.0	1.0	mA	@ 2 MHz	[4,5]
		4.5V		2.4	1.2	mA	@ 4 MHz	[4,5]
		5.0V		3.0	1.5	mA	@ 4 MHz	[4,5]
		4.5V		1.0	0.50	mA	Clock Divide by 16 @ 2 MHz	[4,5]
		5.0V		2.0	0.75	mA	Clock Divide by 16 @ 2 MHz	[4,5]
		4.5V		1.0	0.75	mA	Clock Divide by 16 @ 4 MHz	[4,5]
		5.0V		2.0	1.0	mA	Clock Divide By 16 @ 4 MHz	[4,5]
I_{cc2}	Standby Current	4.5V		10	2	µA	STOP Mode V_{IN} = 0V, V_{cc} WDT is not Running	[6]
		5.0V		10	2	µA	STOP Mode V_{IN} = W_{DT} is not Running	[6]
		4.5V		400	250	µA	STOP Mode V_{IN} = 0V, V_{cc} WDT is Running	[6]
		5.0V		800	450	µA	STOP Mode V_{IN} = 0V, V_{cc} WDT is Running	[6]

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Symbol	Parameter	V_{cc} Note[3]	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
I_{ALL}	Auto Latch Low Current	4.5V		-10	-5	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		-10	-5	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		20	10	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		20	10	µA	$0V < V_{IN} < V_{CC}$	
I_{POR}	Power On Reset	4.5V	4		7.5	ms		
		5.0V	2.5		4.5	ms		
V_{RST}	Auto Reset Voltatge			3.0	2.5	V	2 MHz max Ext. CLK Freq.	[3]

Notes:

[1] I_{CC}:

	Typ	Max	Unit	Freq
Clock Driven on Crystal	3.0 mA	5.0	mA	8 MHz
or XTAL Resonator	0.3 mA	5.0	mA	8 MHz

[2] V_{SS}=0V=GND.
[3] 5.0V ± 0.5V, 4.5V
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1=CL2=100 pF.
[6] Same as note [4] except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS
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Additional Timing Diagram (Standard Mode)

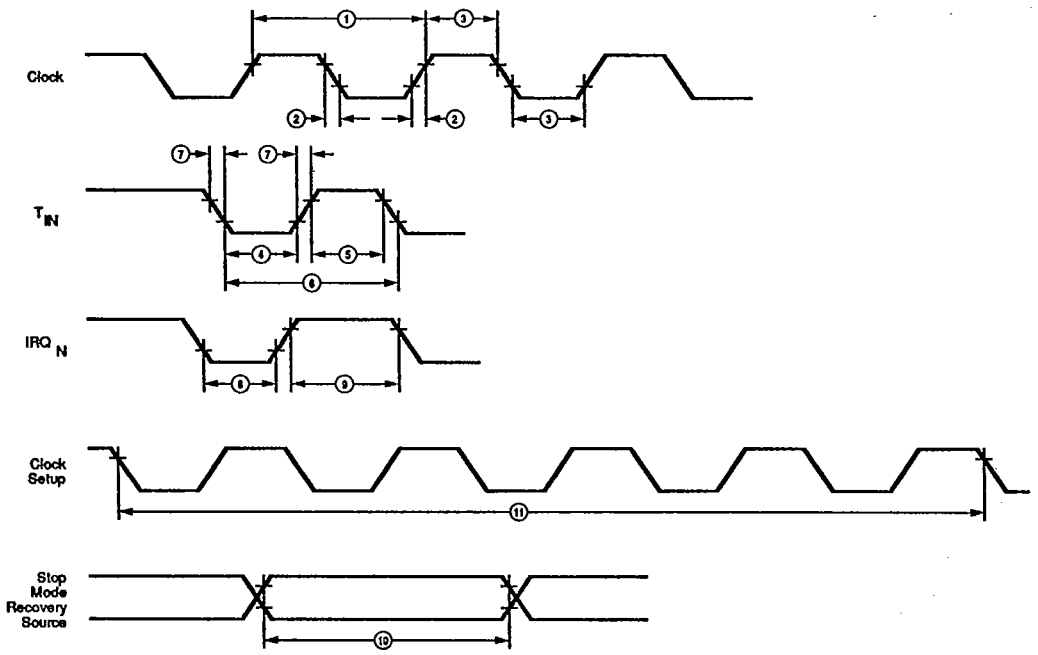

Figure 27. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (Standard Mode)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	100000	83	100000	ns	[1]
			5.0V	125	100000	83	100000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		15	ns	[1]
			5.0V		25		15	ns	[1]
3	TwC	Input Clock Width	4.5V	37		26		ns	[1]
			5.0V	37		26		ns	[1]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1]
			5.0V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	3TpC		3TpC			[1]
			5.0V	3TpC		3TpC			[1]

AC ELECTRICAL CHARACTERISTICS

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Additional Timing Table (Standard Mode – Continued)

No	Symbol	Parameter	V_{cc} Note [6]	T_A = 0°C to +70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1]
			5.0V	8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timers	4.5V		100		100	ns	[1]
			5.0V		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	[1,2]
			5.0V	70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	4.5V	3TpC		3TpC			[1,3]
			5.0V	3TpC		3TpC			[1,3]
9	TwIH	Int. Request Input High Time	4.5V	3TpC		3TpC			[1,2]
			5.0V	3TpC		3TpC			[1,2]
10	Twsm	STOP Mode Recovery Width Spec	4.5V	12		12		ns	
			5.0V	12		12		ns	
			4.5V	5TpC					Reg. SMR - D5=0 No Delay
			5.0V	5TpC					
			4.5V	5TpC					Reg. SM - D5=1 with Delay
			5.0V	5TpC					
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		[4]
			5.0V		5TpC		5TpC		[4]
12	Twdt	Watchdog Timer Delay Time	4.5V	10		10		ms	D0 = 0 [5] [7]
			5.0V	5		5		ms	D1 = 0 [5] [7]
			4.5V	20		20		ms	D0 = 1 [5] [8]
			5.0V	15		15		ms	D1 = 0 [5] [8]
			4.5V	35		35		ms	D0 = 0 [5] [9]
			5.0V	25		25		ms	D1 = 1 [5] [9]
			4.5V	175		175		ms	D0 = 1 [5] [10]
			5.0V	100		100		ms	D1 = 1 [5] [10]

Notes:
[1] Timing Reference uses 0.9 V_{cc} for a logic 1 and 0.1 V_{cc} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 0.
[5] Reg. WDTMR.
[6] 5.0V ± 0.5V, 4.5V
[7] Reg.WDTMR D1=0, D0=0
[8] Reg. WDTMR D1=0, D0=1
[9] Reg. WDTMR D1=1, D0=0
[10] Reg.WDTMR D1=1, D0=1

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

T-49-19-07

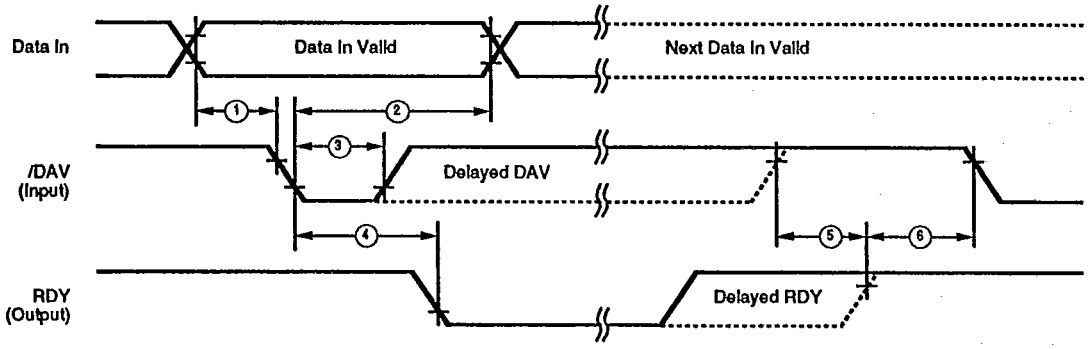

Figure 28. Input Handshake Timing

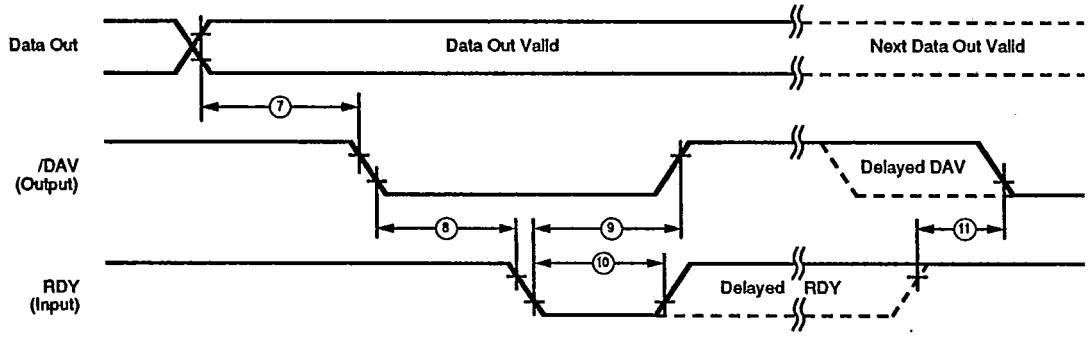

Figure 29. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table - Standard Mode

T-49-19-07

No	Symbol	Parameter	V_{cc} Note [1]	Standard Mode 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	4.5V	0	0			IN
			5.0V	0	0			IN
	ThDI(DAV)	Data In Hold Time	4.5V	160	160			IN
			5.0V	115	115			IN
	TwDAV	Data Available Width	4.5V	155	155			IN
			5.0V	110	110			IN
	TdDAVI (RDY)	DAV Fall to RDY Fall Delay	4.5V		160		160	IN
			5.0V		115		115	IN
	TdDAVId (RDY)	DAV Rise to RDY Rise Delay	4.5V		120		120	IN
			5.0V		80		80	IN
	TdDO(DAV)	RDY Rise to DAV Fall Delay	4.5V	0		0		IN
			5.0V	0		0		IN
	TcLDAV0 (RDY)	Data Out to DAV Fall Delay	4.5V	63		42		OUT
			5.0V	63		42		OUT
	TcLDAV0 (RDY)	DAV Fall to RDY Fall Delay	4.5V	0		0		OUT
			5.0V	0		0		OUT
	TdRDY0 (DAV)	RDY Fall to DAV Rise Delay	4.5V		160		160	OUT
			5.0V		115		115	OUT
	TwRDY	RDY Width	4.5V	110		110		OUT
			5.0V	80		80		OUT
	TdRDY0d (DAV)	RDY Rise to DAV Fall Delay	4.5V	110			110	OUT
			5.0V	80			80	OUT

e:

ard operating temperature range 0°C to +70°C.

EXPANDED REGISTER FILE CONTROL REGISTERS

T-49-19-07

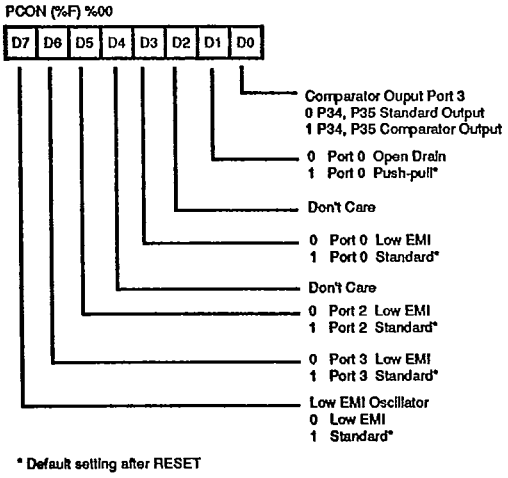

Figure 30. Port Configuration Register

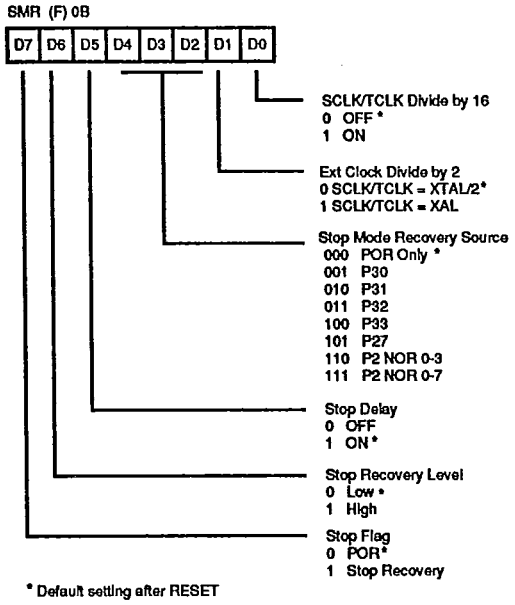

Figure 31. Stop Mode Recovery Register

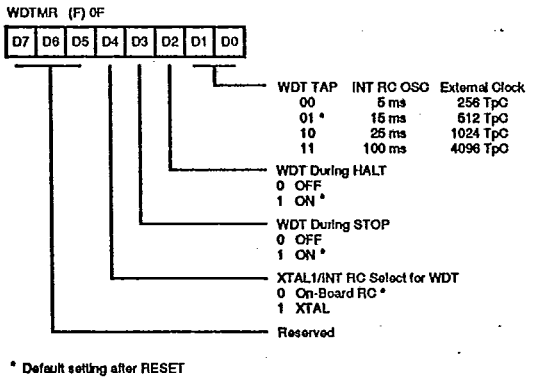

Figure 32. Watchdog Timer Mode Register
Z8 Control Register Diagrams

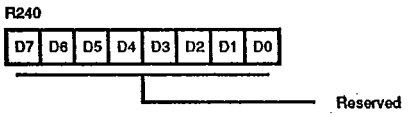

Figure 33. Reserved

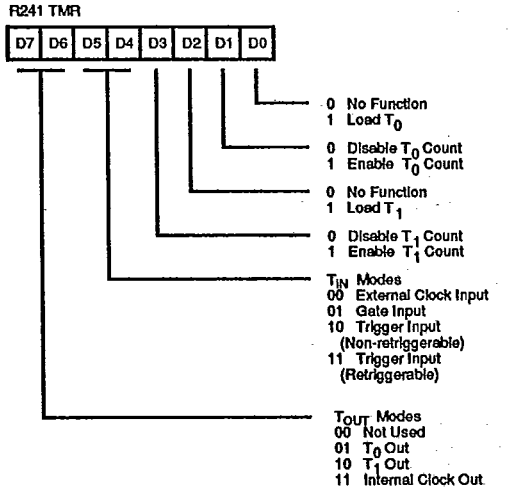

Figure 34. Timer Mode Register
(F1H: Read/Write)

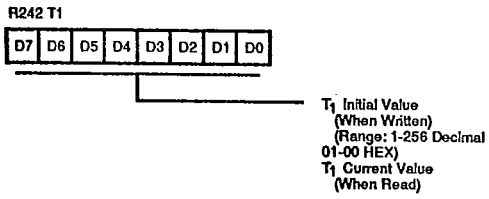

Figure 35. Counter Timer 1 Register
(F2H: Read/Write)

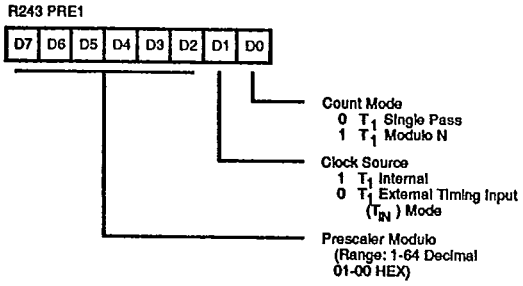

Figure 36. Prescaler 1 Register
(F3H: Write Only)

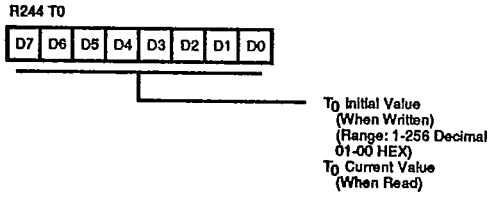

Figure 37. Counter/Timer 0 Register
(F4H: Read/Write)

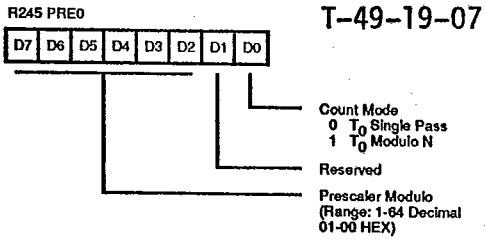

Figure 38. Prescaler 0 Register
(F5H: Write Only)

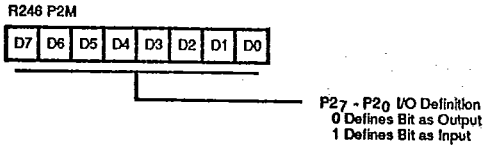

Figure 39. Port 2 Mode Register
(F6H: Write Only)

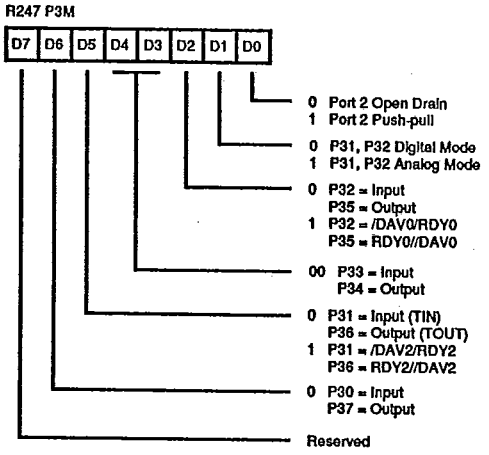

Figure 40. Port 3 Mode Register
(F7H: Write Only)

EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)

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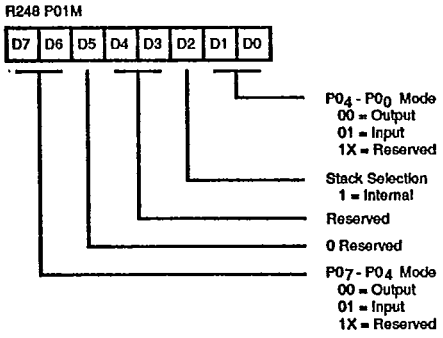

Figure 41. Port 0 and 1 Mode Register (F8H: Write Only)

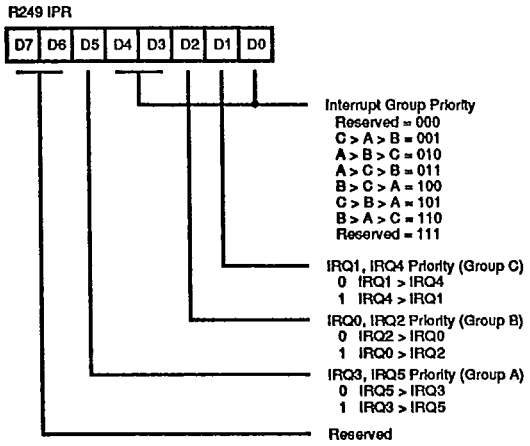

Figure 42. Interrupt Priority Register (F9H: Write Only)

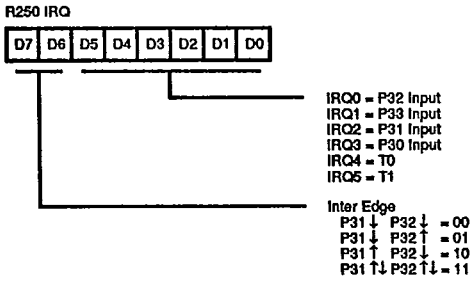

Figure 43. Interrupt Request Register (FAH: Read/Write)

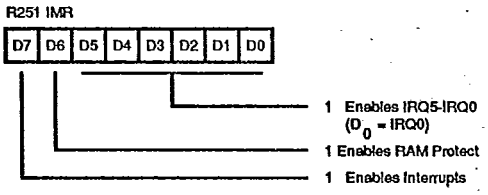

Figure 44. Interrupt Mask Register (FBH: Read/Write)

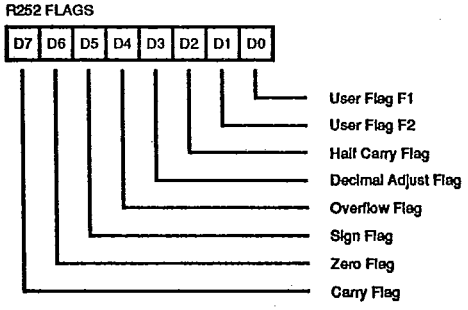

Figure 45. Flag Register (FCH: Read/Write)

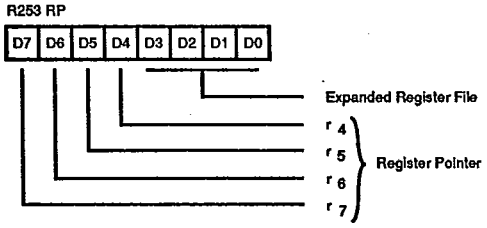

Figure 46. Register Pointer (FDH: Read/Write)

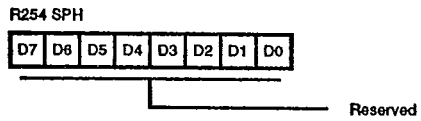

Figure 47. Reserved

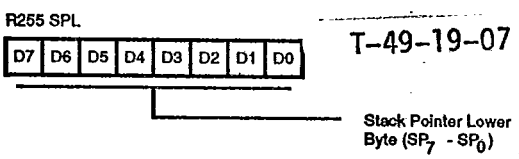

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Figure 48. Stack Pointer (FFH: Read/Write)

INSTRUCTION SET NOTATION

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Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

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Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS

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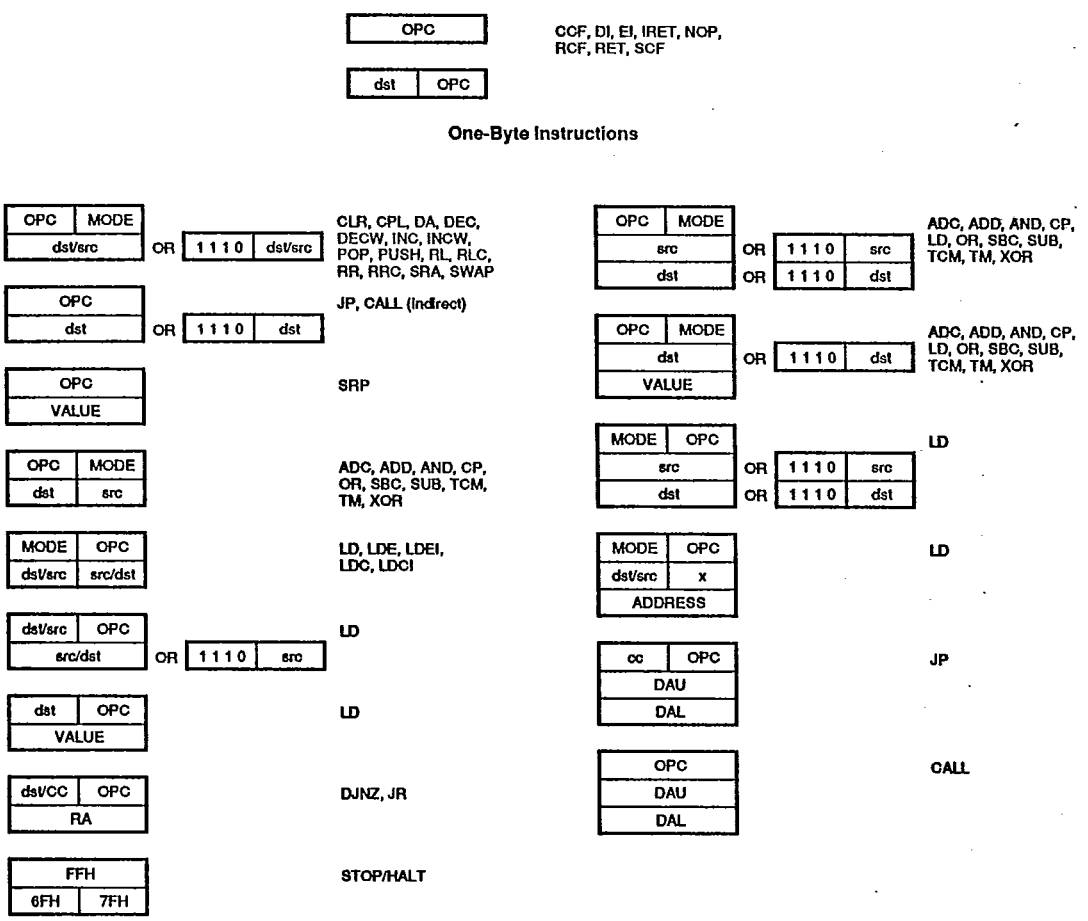

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

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Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	† R IR	A[ ] 40 41	6[ ] A3	*	*	*	*	-	-
DA dst dst←DA dst	R IR	00 01	40 41	-	*	*	*	-	-
DEC dst dst←dst - 1	R IR	00 01	00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR	80 81	80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA r = 0 - F	rA	rA	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r Ir R R R IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

T-49-19-07

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	-	-	-	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

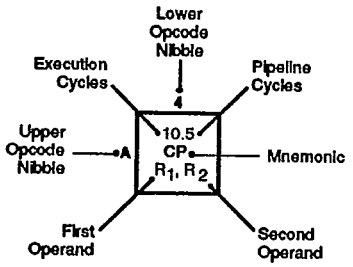
Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

T-49-19-07

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI Ir1, Irr2												6.1 DI
9	6.5 RL R1	6.5 RL IR1	12.0 LDE r2, Irr1	18.0 LDEI Ir2, Irr1												6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2				10.5 LD r1,x,R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r2, Irr1	18.0 LDCI Ir2, Irr1	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP
Bytes per Instruction	2		3				2						3		1	



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

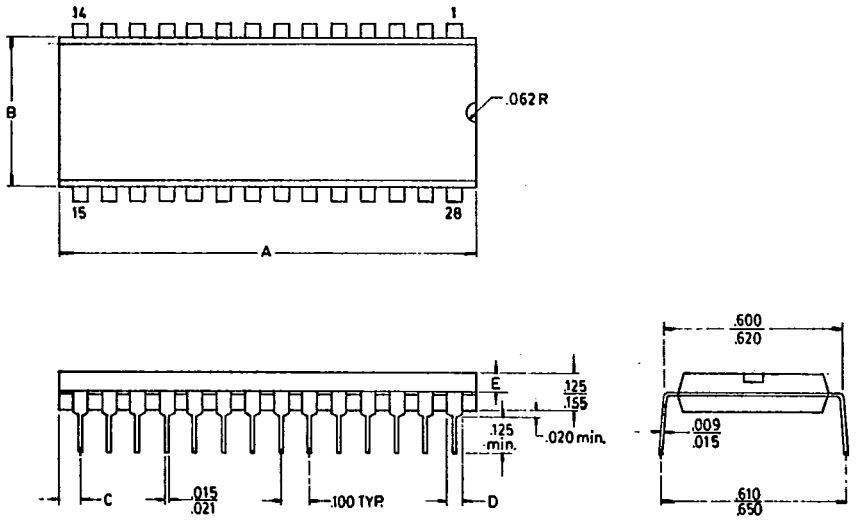
Sequence:
Opcode, First Operand, Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

T-49-19-07



28-Pin Dual In-Line Package (DIP)

ORDERING INFORMATION

Z86E30

T-49-19-07

n ordering the part(s) desired.

°C to +70°C, Plastic Standard Flow

Product Number
Zilog Prefix

12 MHz
28-Pin DIP
Z86E3012PSC

28-Pin Cerdip
Z86E3012KSE

For fast results, contact your local Zilog sales office for assistance i

Codes

Package
P = Plastic DIP
K= Cerdip Window

Temperature
S = 0°C to +70°C

Speed
12 = 12 MHz

Environmental
C = Plastic Standard
E = Hermetic Standard

Example:
Z 86E30 12 P S C is an 86E30 12 MHz, DIP, C

- C — Environmental Flow
- S — Temperature
- P — Package
- 12 — Speed
- 86E30 — Product Number
- Z — Zilog Prefix