19-2912; Rev 1; 2/07

EVALUATION KIT AVAILABLE

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation



## General Description

The MAX1874 charges a single-cell Li+ battery from both USB and AC adapter sources. It also includes battery-to-input power switchover, so the system can be powered directly from the power source rather than from the battery.

In its simplest application, the MAX1874 needs no external MOSFET or diodes, and accepts input voltages up to 6.5V; however, DC input overvoltage protection up to 18V can be added with a single SOT PFET.

On-chip thermal limiting simplifies printed circuit board (PCB) layout and allows optimum charging rate without the thermal limits imposed by worst-case battery and input voltage. When the MAX1874 thermal limit is reached, the charger does not shut down but simply reduces charging current.

Ambient or battery temperature can be monitored with an external thermistor. When the temperature is out of range, charging pauses.

Other features include a $\overline{CHG}$ output to indicate when battery current tapers below a predetermined level. DC power-OK ($\overline{DCOK}$), USB power-OK ($\overline{UOK}$), and power-on (PON) outputs indicate when valid power is present. These outputs drive logic or power-selection MOSFETs to disconnect the charging sources from the load and to protect the MAX1874 from overvoltage.

The MAX1874 contains no logic for communication with the USB host. It must receive instructions from a local microcontroller. The MAX1874 is available in a 16-pin 5mm × 5mm thin QFN package and operates over the -40°C to +85°C temperature range.

## Applications

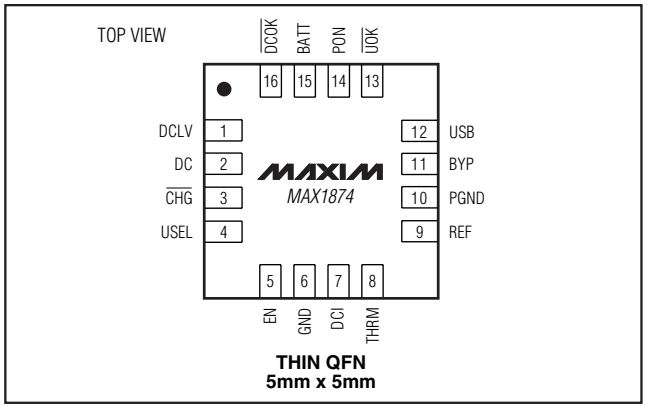
PDAs

Cell Phones

Wireless Appliances

Digital Cameras

## Pin Configuration




THIN QFN
5mm x 5mm

## Features

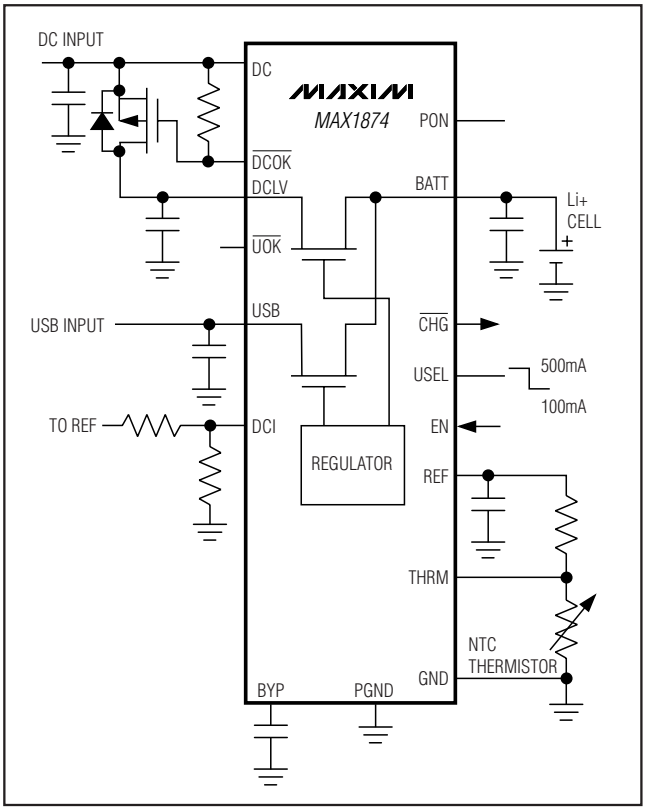
- ♦ Charge from USB* or AC Adapter
- ♦ Automatic Switchover to AC Adapter
- ♦ Thermal Limiting Simplifies Board Design
- ♦ Small, High-Power 16-Pin Thin QFN Package
- ♦ Input Protection Up to 18V
- ♦ Soft-Start
- ♦ Automatic Battery-to-Input Load Switch

*Protected by U.S. Patent #6,507,172.

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| MAX1874ETE | -40°C to +85°C | 16 Thin QFN 5mm x 5mm | T1655-2 |

## Typical Operating Circuit




*Functional Diagram appears at the end of the data sheet.*

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## ABSOLUTE MAXIMUM RATINGS

DC, $\overline{DCOK}$ to GND .....-0.3V to +20V
DCLV, BYP, USB, $\overline{UOK}$, DCI, REF, USEL, THRM, EN, BATT, $\overline{CHG}$, PON to GND .....-0.3V to +7V
PGND to GND .....-0.3V to +0.3V
Continuous Current (DCLV) .....1.1A
Continuous Current (USB) .....0.6A

Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin 5mm × 5mm Thin QFN
(derate 21.3mW/°C above +70°C) .....1.7W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = $V_{USEL}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, Circuit of Figure 2, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT VOLTAGE RANGES AND INPUT CURRENT** | | | | | |
| Maximum DC Input Voltage with Overvoltage Protection | Q2 input MOSFET must be in place; charging occurs only below 6.2V, Figures 3, 4, and 5 | | | 18 | V |
| Maximum DC Input Voltage Without Overvoltage Protection | DC = DCLV, Q2 input MOSFET not on circuit, Figure 2 | | | 6.5 | V |
| Maximum Input Voltage for Charging | | 6.0 | 6.2 | 6.5 | V |
| DC Supply Current | $V_{EN}$ = 0V | | 2 | 4 | mA |
| | $V_{EN}$ = 5V | | 4 | 6 | |
| DCLV Operating Voltage Range | | 4.35 | | 6.00 | V |
| DCLV Shutdown Supply Current | $V_{EN}$ = 0V | | 300 | 500 | µA |
| USB Input Voltage Range | | 4.35 | | 6.50 | V |
| USB Supply Current | $V_{EN}$ = 0V | | 500 | 750 | µA |
| | $V_{EN}$ = 5V, $V_{DC}$ = 0V | | 2 | 3 | mA |
| | $V_{EN}$ = 5V, $V_{DC}$ = 5V | | 160 | 300 | µA |
| DCI Input Current | | | 1 | 100 | nA |
| BYP Output Resistance | (Note 1) | | 5 | | Ω |
| THRM Input Bias Current | | | 1 | 100 | nA |
| **BATTERY VOLTAGE** | | | | | |
| BATT Regulation Voltage | | 4.1685 | 4.20 | 4.2315 | V |
| BATT Prequal Voltage Threshold | BATT rising | 2.8 | 3 | 3.2 | V |
| Prequal Threshold Hysteresis | | | 70 | | mV |
| USB Charging Headroom | $I_{USB}$ = 100mA | | 100 | | mV |
| | $I_{USB}$ = 500mA | | 200 | | |
| DC Charging Headroom | $I_{DCIN}$ = 800mA | | 250 | | mV |
| REF Voltage (Buffered Output) | $I_{REF}$ = 0 to 500µA, 4V < $V_{DC}$ or $V_{USB}$ < 6.5V; does not affect BATT regulation accuracy | 2.94 | 3 | 3.06 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = $V_{USEL}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, Circuit of Figure 2, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **BATTERY CHARGING AND PRECHARGE CURRENT** | | | | | |
| DCI Voltage Range | | 0.1 x $V_{REF}$ | | $V_{REF}$ | V |
| DCI Voltage to BATT Current | $V_{DCI}$ = $V_{REF}$ | 950 | 1000 | 1050 | mA |
| | $V_{DCI}$ = $V_{REF}$ / 2 | 490 | 520 | 550 | |
| USB Charging Current | USEL = high | | 455 | 495 | mA |
| | USEL = low | | 82 | 95 | |
| Soft-Start Current-Ramp Time | Measured from 10% to 90% | | 7 | | ms |
| Prequal Charging Current | $V_{BATT}$ = 2.5V | 35 | 55 | 70 | mA |
| BATT Input Current | No DC or USB power, $V_{BATT}$ = 4.2V | | 5 | 7.5 | µA |
| BATT Shutdown Current | EN = GND, USB- and/or DC-powered | | 1 | 2 | µA |
| **THERMISTOR MONITOR AND DIE-TEMPERATURE REGULATION** | | | | | |
| THRM COLD Trip Level | (Note 2) | 0.72 | 0.74 | 0.76 | $V_{REF}$ |
| THRM HOT Trip Level | (Note 2) | 0.28 | 0.29 | 0.30 | $V_{REF}$ |
| THRM Disable Threshold | | 50 | 100 | 150 | mV |
| Internal Die Thermal Limit | | | +105 | | °C |
| **LOGIC INPUT/OUTPUTS AND GATE DRIVERS** | | | | | |
| PON High Output Resistance | PON pulled up to active input (DCLV or USB), $V_{DCLV}$ or $V_{USB}$ = 5V | | 25 | | Ω |
| PON Low Output Resistance | PON resistance to GND, $V_{DCLV}$ = $V_{USB}$ = 0 | | 120 | | kΩ |
| $\overline{DCOK}$ Low Output Resistance | $\overline{DCOK}$ pulled low | | 25 | | Ω |
| $\overline{DCOK}$ Off-Leakage Current | $V_{\overline{DCOK}}$ = 12V, $V_{DC}$ = 0V | | | 1 | µA |
| $\overline{UOK}$ Output Resistance | $\overline{UOK}$ resistance to GND, $V_{DC}$ = 0 | | 25 | | Ω |
| $\overline{UOK}$ Off-Leakage Current | $V_{\overline{UOK}}$ = 6.5V | | | 1 | µA |
| $\overline{CHG}$ Threshold to Indicate Battery Full, Battery Current Falling (Note 3) | DC input (% of charge current set at DCI) | 8 | 12.5 | 19 | % |
| | USB input, USEL = 5V (% of USB charging current) | 20 | 25 | 30 | |
| | USB input with USEL = 0 | | Voltage mode | | |
| $\overline{CHG}$ Logic-Low Output | Sinking 10mA sink | | | 0.4 | V |
| $\overline{CHG}$ Leakage Current | $V_{\overline{CHG}}$ = 6.5V | | | 1 | µA |
| EN, USEL Logic-Input High Level | | 1.6 | | | V |
| EN, USEL Logic-Input Low Level | | | | 0.4 | V |
| EN, USEL Input Bias Current | | | | 1 | µA |

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## ELECTRICAL CHARACTERISTICS (continued)

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = $V_{USEL}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, Circuit of Figure 2, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TIMING** | | | | | |
| DC Rising to $\overline{DCOK}$ Falling | USB = open, DC rising to 5V | | 20 | | ms |
| USB Rising to $\overline{UOK}$ Falling | DC = open, USB rising to 5V | | 20 | | ms |
| DC Falling to $\overline{DCOK}$ Going Open-Drain Propagation Delay | USB = open, 1kΩ pullup | | 2 | | µs |
| USB Falling to $\overline{UOK}$ Going Open-Drain Propagation Delay | DC = open, 10kΩ pullup | | 2 | | µs |
| DC Rising to PON Rising (90%) | USB = open, DC step to 5V, BATT = 3.6V, 100kΩ pulldown | | 20 | | ms |
| USB Rising to PON Rising (90%) | DC = open, $V_{USB}$ step to 5V, $V_{BATT}$ = 3.6V, 100kΩ pulldown | | 20 | | ms |
| DC Falling to PON Going Open-Drain Propagation Delay | USB = open, 100kΩ pulldown | | 2 | | µs |
| USB Falling to PON Going Open-Drain Propagation Delay | DC = open, 100kΩ pulldown | | 2 | | µs |

## ELECTRICAL CHARACTERISTICS

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = $V_{USEL}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, Circuit of Figure 2, **$T_A$ = -40°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT VOLTAGE RANGES AND INPUT CURRENT** | | | | | |
| Maximum DC Input Voltage with Overvoltage Protection | Q2 input MOSFET must be in place; charging occurs only below 6.2V, Figures 3, 4, and 5 | | | 18 | V |
| Maximum DC Input Voltage Without Overvoltage Protection | DC = DCLV, Q2 input MOSFET not on circuit, Figure 3 | | | 6.5 | V |
| Maximum Input Voltage for Charging | | 6.0 | | 6.5 | V |
| DC Supply Current | $V_{EN}$ = 0V | | | 4 | mA |
| | $V_{EN}$ = 5V | | | 6 | |
| DCLV Operating Voltage Range | | 4.35 | | 6.00 | V |
| DCLV Shutdown Supply Current | $V_{EN}$ = 0V | | | 500 | µA |
| USB Input Voltage Range | | 4.35 | | 6.50 | V |
| USB Supply Current | $V_{EN}$ = 0V | | | 750 | µA |
| | $V_{EN}$ = 5V, $V_{DC}$ = 0V | | | 3 | mA |
| | $V_{EN}$ = 5V, $V_{DC}$ = 5V | | | 300 | µA |
| DCI Input Current | | | | 100 | nA |
| THRM Input Bias Current | | | | 100 | nA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = $V_{USEL}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, Circuit of Figure 2, **$T_A$ = -40°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **BATTERY VOLTAGE** | | | | | |
| BATT Regulation Voltage | | 4.1685 | | 4.2315 | V |
| BATT Prequal Voltage Threshold | BATT rising | 2.8 | | 3.2 | V |
| REF Voltage (Buffered Output) | $I_{REF}$ = 0 to 500µA, 4V < $V_{DC}$ or $V_{USB}$ < 6.5V; does not affect BATT regulation accuracy | 2.94 | | 3.06 | V |
| **BATTERY CHARGING AND PRECHARGE CURRENT** | | | | | |
| DCI Voltage Range | | 0.1 x $V_{REF}$ | | $V_{REF}$ | V |
| DCI Voltage to BATT Current | $V_{DCI}$ = $V_{REF}$ | 930 | | 1070 | mA |
| | $V_{DCI}$ = $V_{REF}$ / 2 | 490 | | 565 | |
| USB Charging Current | USEL = high | | | 495 | mA |
| | USEL = low | | | 95 | |
| Prequal Charging Current | $V_{BATT}$ = 2.5V | 40 | | 70 | mA |
| BATT Input Current | No DC or USB power, $V_{BATT}$ = 4.2V | | | 7.5 | µA |
| BATT Shutdown Current | EN = GND, USB and/or DC powered | | | 2 | µA |
| **THERMISTOR MONITOR AND DIE-TEMPERATURE REGULATION** | | | | | |
| THRM COLD Trip Level | (Note 2) | 0.72 | | 0.76 | $V_{REF}$ |
| THRM HOT Trip Level | (Note 2) | 0.28 | | 0.30 | $V_{REF}$ |
| THRM Disable Threshold | | 50 | | 150 | mV |
| **LOGIC INPUT/OUTPUTS AND GATE DRIVERS** | | | | | |
| $\overline{DCOK}$ Off-Leakage Current | $V_{\overline{DCOK}}$ = 12V, $V_{DC}$ = 0V | | | 1 | µA |
| $\overline{UOK}$ Off-Leakage Current | $V_{\overline{UOK}}$ = 6.5V | | | 1 | µA |
| $\overline{CHG}$ Threshold to Indicate Battery Full, Battery Current Falling (Note 3) | DC input (% of charge current set at DCI) | 8 | | 20 | % |
| | USB input, USEL = 5V (% of USB charging current) | 20 | | 30 | |
| $\overline{CHG}$ Logic-Low Output | Sinking 10mA sink | | | 0.4 | V |
| $\overline{CHG}$ Leakage Current | $V_{\overline{CHG}}$ = 6.5V | | | 1 | µA |
| EN, USEL Logic-Input High Level | | 1.6 | | | V |
| EN, USEL Logic-Input Low Level | | | | 0.4 | V |
| EN, USEL Input Bias Current | | | | 1 | µA |

**Note 1:** BYP internally connects to the active power input (DCLV or USB). DCLV takes priority if both inputs are powered.

**Note 2:** These limits guarantee +5°C accuracy with 5% accuracy of thermistor beta (3450 nominal) with 2°C of hysteresis.

**Note 3:** The $\overline{CHG}$ output does not go high unless charge current is below the indicated threshold (as set by DCI) and the charger is in voltage-mode operation. In 100mA USB mode, $\overline{CHG}$ goes high when the charger transitions from current to voltage mode.

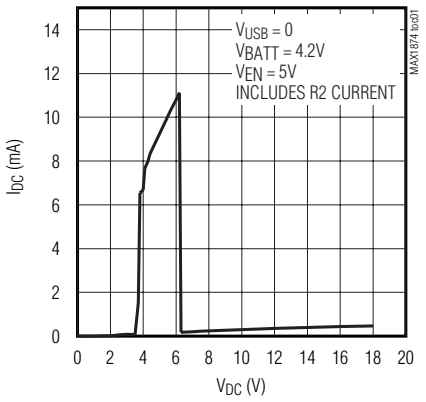
**Note 4:** Specifications to -40°C are guaranteed by design, not production tested.

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

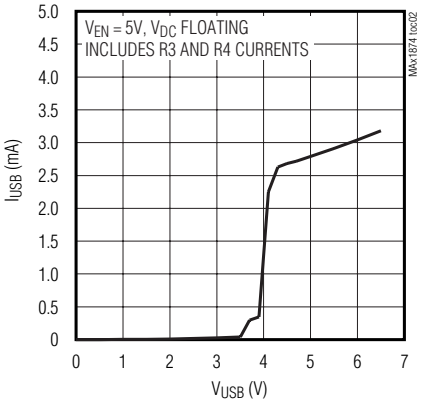
## Typical Operating Characteristics

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, $V_{DCI}$ = $V_{REF}$, $V_{USEL}$ = 5V, Circuit of Figure 4, $T_A$ = +25°C, unless otherwise noted.)

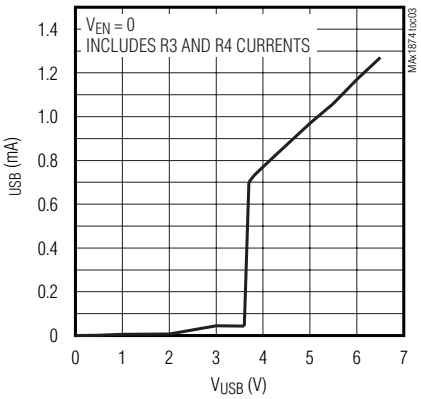
**DC INPUT CURRENT vs. DC INPUT VOLTAGE**



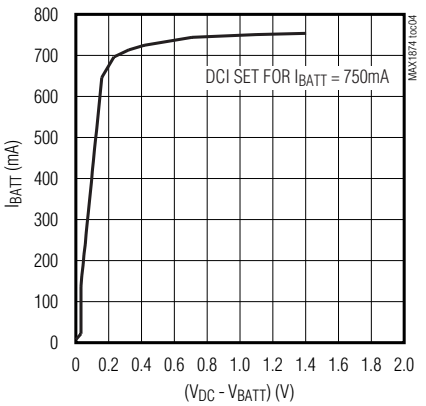

**USB INPUT CURRENT vs. USB INPUT VOLTAGE**



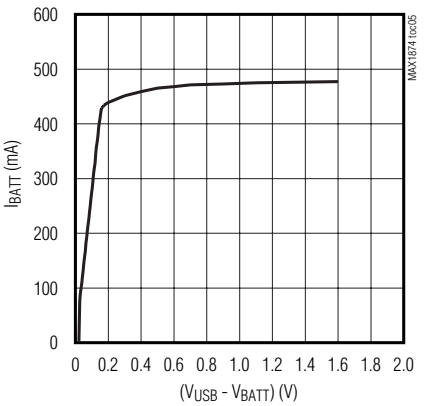

**USB INPUT CURRENT vs. USB INPUT VOLTAGE ($V_{EN}$ = 0)**



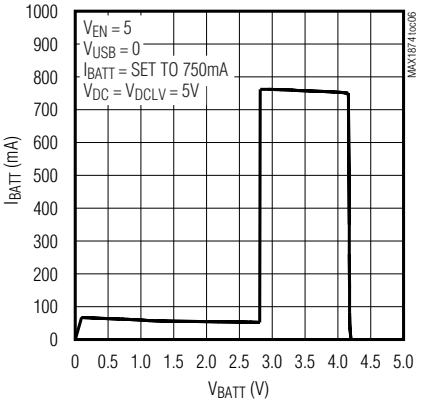

**CHARGE CURRENT vs. DC INPUT-VOLTAGE HEADROOM**



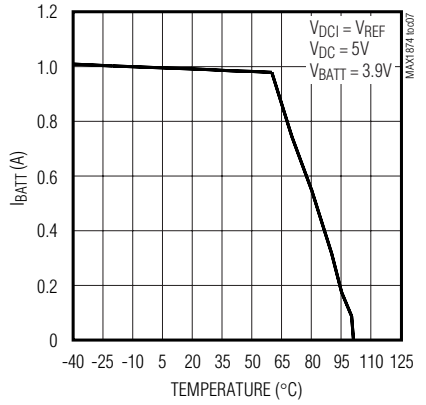

**CHARGE CURRENT vs. USB VOLTAGE HEADROOM**



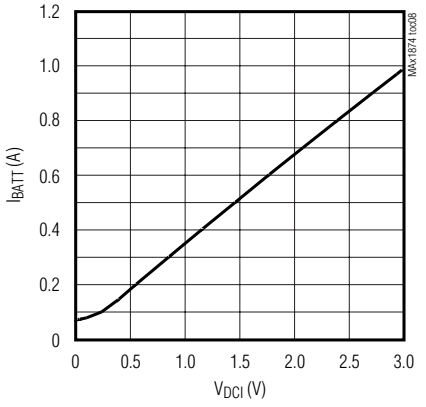

**CHARGE CURRENT vs. BATTERY VOLTAGE ($I_{BATT}$ vs. $V_{BATT}$)**



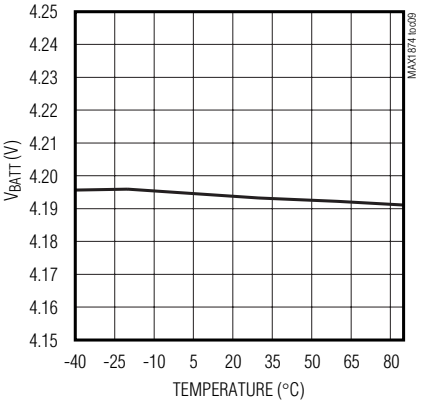

**CHARGE CURRENT vs. TEMPERATURE WITH THERMAL REGULATION**




**CHARGE CURRENT vs. $V_{DCI}$**



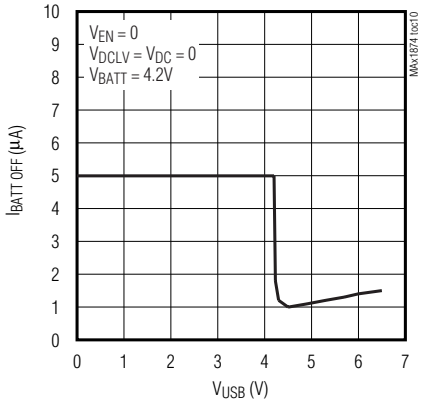

**BATTERY TERMINATION VOLTAGE vs. TEMPERATURE**



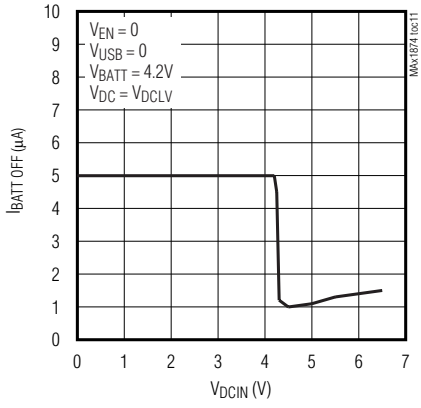
## Typical Operating Characteristics (continued)

($V_{USB}$ = $V_{DC}$ = $V_{DCLV}$ = $V_{EN}$ = 5V, $V_{BATT}$ = 4.2V, $V_{THRM}$ = $V_{REF}$ / 2, $V_{DCI}$ = $V_{REF}$, $V_{USEL}$ = 5V, Circuit of Figure 4, $T_A$ = +25°C, unless otherwise noted.)

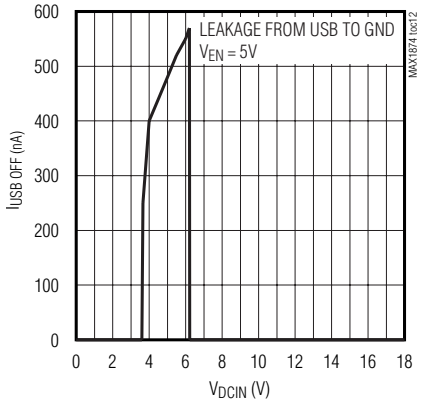
**OFF-BATTERY LEAKAGE vs. USB INPUT VOLTAGE**



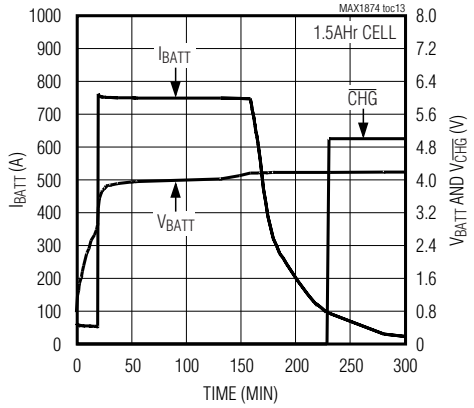

**OFF-BATTERY LEAKAGE vs. DC INPUT VOLTAGE**



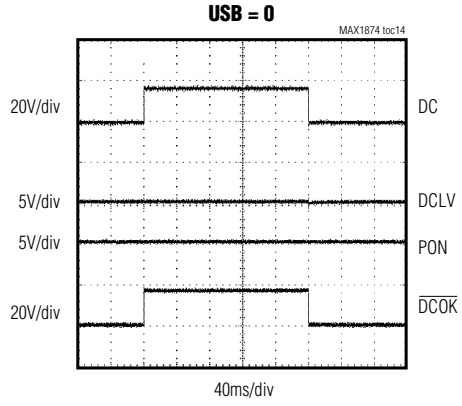

**USB LEAKAGE vs. DC INPUT VOLTAGE**



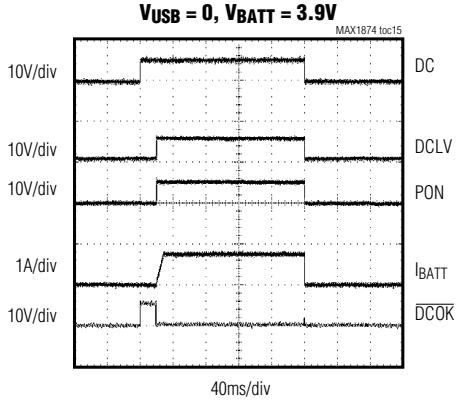

**BATTERY CURRENT AND VOLTAGE vs. TIME**



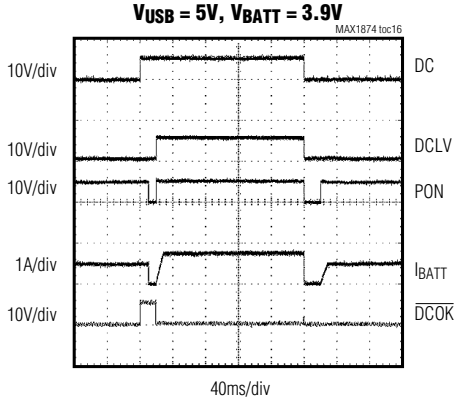

**RESPONSE TO OVERVOLTAGE INPUT USB = 0**



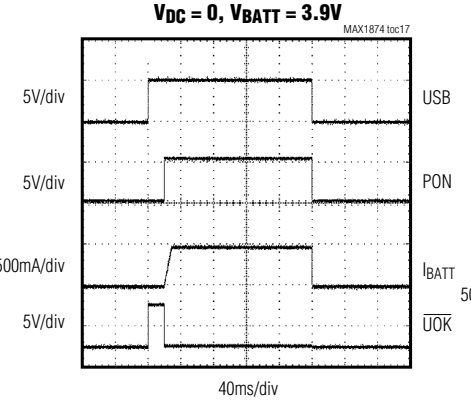

**DC CONNECT WAVEFORMS $V_{USB}$ = 0, $V_{BATT}$ = 3.9V**



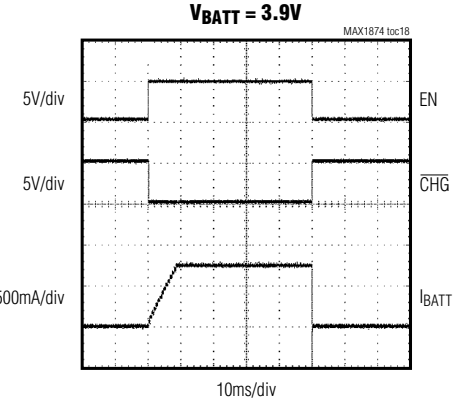

**DC CONNECT WAVEFORMS $V_{USB}$ = 5V, $V_{BATT}$ = 3.9V**




**USB CONNECT WAVEFORMS $V_{DC}$ = 0, $V_{BATT}$ = 3.9V**




**DC STARTUP WAVEFORMS FOR ENABLE $V_{BATT}$ = 3.9V**



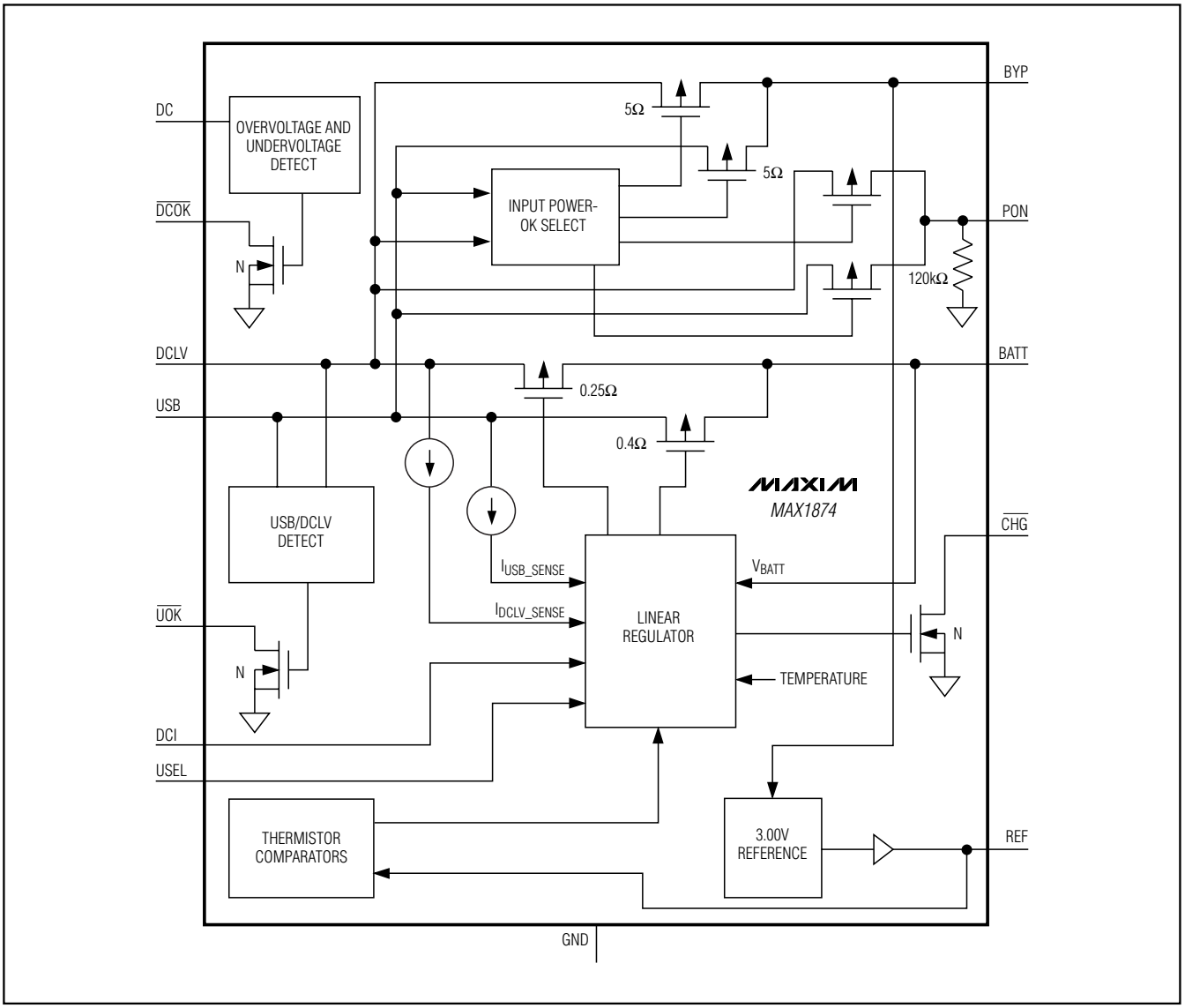
# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | DCLV | Low-Voltage Charger Input. DCLV charges BATT through an internal MOSFET. Maximum operating voltage at this pin is 6.0V. When an overvoltage protection MOSFET is connected, DCLV is connected to DC when the input voltage is suitable for charging. |
| 2 | DC | Voltage-Sense Pin for DC Input from AC Adapter. Maximum operating voltage at this pin is 18V. |
| 3 | $\overline{CHG}$ | $\overline{CHG}$ is an active-low, open-drain output that goes low when the MAX1874 is charging and goes high when both of the following conditions are met (see the *Battery Full ($\overline{CHG}$)* section):<br>1) Charge current drops to a set threshold (Table 2).<br>2) The charger is in voltage mode. |
| 4 | USEL | USEL is a logic input that sets USB source charging current to 500mA when USEL is logic high and to 100mA when USEL is logic low. |
| 5 | EN | Enable/Disable Input. Drive EN high to enable the device. When EN is low, $\overline{UOK}$, $\overline{DCOK}$, PON, and REF remain active. |
| 6 | GND | Ground |
| 7 | DCI | The voltage at this input sets the fast-charge current when the DCLV input is powering the charger. See the *Charging Current* section. |
| 8 | THRM | THRM pauses charging when an externally connected thermistor (10kΩ at +25°C) is at less than 0°C or greater than +50°C. Connect to GND to disable. See the *External Thermistor Monitor (THRM)* section. |
| 9 | REF | 3V Reference Output. Sources up to 500µA to bias $I_{DCI}$ and external thermistor. Bypass with 0.1µF to GND. REF loading does not affect BATT regulation accuracy. |
| 10 | PGND | Power Ground. Connect to GND at a single, low-impedance point. |
| 11 | BYP | BYP powers internal circuitry and switches to the active input (either DCLV or USB). Bypass with a 2.2µF capacitor to GND. |
| 12 | USB | USB Charger Input. Charges BATT through an internal MOSFET. |
| 13 | $\overline{UOK}$ | $\overline{UOK}$ is an active-low, open-drain output that goes low to indicate when the USB input is the valid charging source. |
| 14 | PON | PON is an active-high, open-drain output with an internal 120kΩ resistor to ground that goes high when $V_{DC}$ or $V_{USB} > V_{BATT}$. PON can directly drive an external PFET that disconnects the battery from the system load when power is applied. |
| 15 | BATT | Charge Output. Connect to the positive terminal of the Li+ battery. |
| 16 | $\overline{DCOK}$ | $\overline{DCOK}$ is an active-low, open-drain output that goes low when $3.5V < V_{DC} < 6.2V$. |

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## Functional Diagram



# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## Detailed Description

The MAX1874 charges a single-cell Li+ battery from either USB power sources or AC adapter sources. It contains a complete two-input linear charger that controls both battery charge current and voltage. In addition to all charging functions, the MAX1874 includes voltage-sensing and switchover circuitry that selects the active input source. When both inputs are active, priority is given to the AC adapter (DC). Charging current is regulated with on-chip power MOSFETs, so no external MOSFETs are required for a basic two-input charger. Additional features such as input-voltage protection and battery-load switching can be added with external MOSFETs that are driven directly from MAX1874 outputs.

The MAX1874 also features a thermal regulation loop that adjusts charging current so the die temperature remains below +105°C. See the *Package Thermal Limiting* section. This on-chip thermal control simplifies PCB layout and allows the optimum charging rate to be set without the thermal limits imposed by worst-case battery and input voltage. When the MAX1874 thermal limit is reached, the charger does not shut down but reduces charging current.

In addition to, and separate from, its internal die temperature control, the MAX1874 can also monitor ambient or cell temperature with an external thermistor connected to THRM. When the thermistor temperature is out of range (greater than +50°C or less than 0°C), charging stops until the temperature returns to normal. See the *External Thermistor Monitor (THRM)* section.

Other features include a $\overline{CHG}$ output to indicate battery full (when charge current tapers to a percentage of fast-charge current). $\overline{DCOK}$, $\overline{UOK}$, and power-on (PON) outputs indicate when valid power is present. These outputs can drive overvoltage protection and power selection MOSFETs (Figures 3, 4, and 5).

When charging is stopped or input power is removed, battery leakage is typically 5µA. No input blocking diodes are required to prevent battery drain.

With USB power connected, but without power at the DC input, charge current can be set to either 500mA or 100mA through the USEL input. When power is taken from the DC input, charge current is linearly set by the voltage at DCI. The MAX1874 charge current can also be DAC controlled with the output of a DAC connected to DCI. See the *Charging Current* section.

### Enable (EN)

The enable input, EN, switches the MAX1874 on or off. With EN high, the MAX1874 is on and can begin charging. When EN is low, $\overline{UOK}$, $\overline{DCOK}$, PON, and REF remain active. Charging stops when EN is low, but the chip remains biased and continues to draw current from the input supplies so power-monitoring outputs can remain valid.

### USB-to-Adapter Power Handoff

The MAX1874 can charge from either the USB input or the DC input. It cannot charge from both sources at the same time. The IC automatically selects the active input and charges from that. If both power sources are active, the adapter input (DC) takes precedence. Table 1 describes the switchover between DC and USB.

DC serves as the sense input for the adapter power source. This input senses when DC is above 6.2V (maximum range is 18V) or below 4V. When it senses the DC source is above 6.2V, $\overline{DCOK}$ goes high, indicating an invalid DC input. See the *DC Power-OK ($\overline{DCOK}$)* section.

When power is connected to DC, the MAX1874 requires 20ms to validate the input. Consequently, charging is interrupted for 20ms until it is determined that input power is good. Also, when DC power is removed while valid USB power is present, charging is interrupted for 20ms before transferring to the USB source.

### DC Power-OK ($\overline{DCOK}$)

$\overline{DCOK}$ is an active-low, open-drain output that goes low when $V_{DC}$ is below 6.2V or above 3.5V. $\overline{DCOK}$ can be used as a logic output, but is also designed to drive an external MOSFET (Q2 in Figures 3, 4, and 5). This allows the charger to protect the input from overvoltage up to 18V. Charging is disabled for inputs over 6.2V. An external 1kΩ pullup resistor keeps $\overline{DCOK}$ high (external MOSFET off) until it is certain the voltage is within the

**Table 1. USB and DC Input Selection**

| $V_{DC}$ > 18V OR $V_{USB}$ > 6.5V | 4V < $V_{DC}$ < 6.2V AND 0 < $V_{USB}$ < 6.5V | 4V < $V_{USB}$ < 6.5V AND $V_{DC}$ < 4V OR $V_{DC}$ > 6.2V | $V_{DC}$ < 4V OR $V_{DC}$ > 6.2V, AND $V_{USB}$ < 4V |
|---|---|---|---|
| Exceeds operating input range. Not allowed. See the *Absolute Maximum Ratings* section. | DCLV powers device and supplies charging current. | 1) USB powers device and supplies charging current.<br>2) DCLV disconnected from DC source through external MOSFET (Q2 Figures 3, 4, and 5). | No charging |

***Note:*** *$V_{DC}$ takes precedence when both inputs are valid.*

acceptable range. To verify that the input voltage is stable, $\overline{DCOK}$ has an internal delay of 20ms before connecting power to DCLV. $\overline{DCOK}$ remains operational when EN is low (charger off).

### USB Power-OK ($\overline{UOK}$)

$\overline{UOK}$ is an active-low, open-drain output that goes low to indicate that $V_{USB}$ is valid (greater than 4V). $\overline{UOK}$ remains operational when EN is low (charger off). An external 10kΩ pullup resistor keeps $\overline{UOK}$ high until it is certain that power is within the acceptable range. $\overline{UOK}$ can be used as a logic output, or to control a MOSFET that switches USB power directly to the system load when the MAX1874 is powered from a USB source (Q1 in Figure 4).

### Bypass (BYP)

BYP is the bypass connection for the MAX1874's internal power rail. Bypass to GND with a 2.2µF or greater capacitor. The voltage at BYP is supplied from either DCLV or USB through an internal 5Ω switch network.

### Power On (PON)

PON goes high when $V_{DC}$ or $V_{USB}$ is within its normal operating range. PON can be used as a logic output to indicate power is connected or can drive an external P-channel MOSFET that switches the system load from the battery to an external source when power is applied. See Q3 in Figures 4 and 5.

### Charging Current

#### Precharge Current

When the MAX1874 is powered with a battery connected, the IC first detects if the cell voltage is ready for full charge current. If the cell voltage is less than the prequal level (3V typ), the battery is precharged with a 50mA current until the cell reaches the proper level. The full charging current, as set by USEL or DCI, is then applied.

#### USEL

The charging current from the USB source is selected by USEL. A USB source can supply a maximum of 100mA or 500mA. USB hosts and powered hubs typically supply 500mA, while unpowered hubs supply 100mA. A logic low on USEL selects a 100mA maximum charging current. A logic high on USEL selects a 500mA maximum charging current.

#### DCI

When charging from the DCLV input, the voltage at DCI sets the charge current. The voltage-to-current transfer ratio from DCI to BATT is $1A/V_{REF}$. The DCI pin should be connected to a resistive divider from REF to DCI to GND (R5 and R6 in Figures 2 and 4). In this configuration, $I_{BATT}$ is as follows:

$$I_{BATT} = [R6 / (R5 + R6)] \text{ Amps}$$

R5 and R6 should total 25kΩ or more to minimize loading on REF. Connecting DCI directly to REF results in a 1A charge current.

### Battery Full ($\overline{CHG}$)

$\overline{CHG}$ is low when the MAX1874 is charging in either the prequal or full-charging state. $\overline{CHG}$ then goes high when the charging current falls below a percentage of the set fast-charge current (Table 2) **and** the charger is in voltage mode ($V_{BATT}$ near 4.2V). The $\overline{CHG}$ current threshold is a function of the charger mode. When charging from a DC source, $\overline{CHG}$ goes high when $I_{BATT}$ falls to 12.5% of the current set by $V_{DCI}$ **and** the charger is in voltage mode ($V_{BATT}$ near 4.2V). When charging from a USB source with USEL high, $\overline{CHG}$ goes high when $I_{BATT}$ falls to 125mA **and** the charger is in voltage mode. If the MAX1874 is charging from a USB source with USEL low, $\overline{CHG}$ goes high when the charger enters voltage mode.

### Package Thermal Limiting

On-chip thermal limiting in the MAX1874 simplifies PCB layout and allows charging rates to be automatically optimized without constraints imposed by worst-case minimum battery voltage, maximum input voltage, and maximum ambient temperature. When the MAX1874 thermal limit is reached, the charger does not shut down but simply reduces charging current. This allows the board design to be optimized for compact size and typical thermal conditions. The MAX1874 reduces charging current to keep its die temperature below +105°C.

**Table 2. $\overline{CHG}$ Battery Full Indication**

| CHARGING SOURCE | CHARGE CURRENT THRESHOLD FOR $\overline{CHG}$ GOING HIGH |
|---|---|
| DCLV Charging | 12.5% of Charge Current Set by DCI *and* Charger in Voltage Mode |
| USB Charging 500mA (USEL high) | 125mA *and* Charger in Voltage Mode |
| USB Charging 100mA (USEL low) | Charger in Voltage Mode |

***Note:*** *$\overline{CHG}$ does not go high when charge current is reduced by the thermal regulation loop.*

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

The MAX1874's thin QFN package includes a bottom metal plate that reduces thermal resistance between the die and the PCB. The external pad should be soldered to a large ground plane. This helps dissipate power and keeps the die temperature below the thermal limit. The MAX1874 thermal resistance from the die to the package thermal pad is typically 5°C/W. The thermal resistance of 1in$^2$ of 1oz copper on typical FR4 PC board material in free air is +42°C/W (typ). Consequently, the PC board pad area dominates the MAX1874's ability to dissipate heat. The MAX1874's thermal regulator is set for a +105°C die temperature. With the example thermal resistance of +47°C/W, the MAX1874 charge-current thermal limiting can be expected to occur when dissipating approximately 1.7W at +25°C ambient, and when dissipating approximately 0.75W at +70°C ambient.

The power dissipated in the charger is $P_{DISS} = [V_{IN}$ (either $V_{USB}$ or $V_{DCLV}$) - $V_{BATT}] \times I_{CHARGE}$. Power dissipation drops as the battery voltage rises, so thermal-charge current limiting, if it occurs, typically releases soon after charging begins and has little impact on charge time.

### External Thermistor Monitor (THRM)

The MAX1874 features an internal window comparator to monitor battery pack temperature or ambient temperature with an external negative temperature coefficient thermistor. In typical systems, temperature is monitored to prevent charging at ambient temperature extremes (below 0°C or above +50°C). When the temperature moves outside these limits, charging is stopped. If the $V_{THERM}$ returns to within its normal window, charging resumes. Connect THRM to GND when not using this feature. The THRM block diagram is detailed in Figure 1. Note that the temperature monitor at THRM is entirely separate from the on-chip temperature limiting discussed in the *Package Thermal Limiting* section.

The input thresholds for the THRM input are 0.74 × $V_{REF}$ for the COLD trip point and 0.29 × $V_{REF}$ for the HOT trip point.

## Applications Information

### Input Overvoltage Protection Switch

The DCLV input from an AC adapter or other source can be protected against overvoltage of up to 18V by connecting an external P-channel MOSFET (Q2 in Figures 3, 4, and 5) between DC and DCLV. When $V_{DC}$ exceeds 6.2V, the $\overline{DCOK}$ output turns the P-channel MOSFET off. On power-up, $\overline{DCOK}$ remains high until it has been verified that $V_{DC}$ is in range. If protection above 6.5V is not needed, then the MOSFET from the DC to DCLV can be omitted (Figure 2).

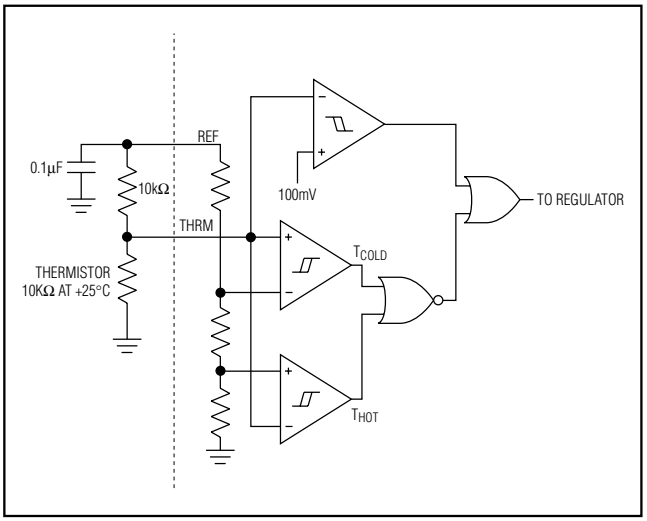



*Figure 1. Thermistor Sensing Block Diagram*

### Battery-Load Switch

When input power is connected to the charger, some systems prefer that the battery is disconnected from the load and that system load current is taken directly from the DC input or USB source. This is an alternative to the basic case where the system load is permanently connected to the battery. The later setup is lower cost but has the disadvantage that if the battery is completely discharged, the system might not be ready to operate immediately, or might have limited functionality immediately upon plugging in the charger. If the battery has a load-disconnect switch, the system is more complex, but operation does not depend on the state of the battery. When system power is taken from the DC or USB input source, use D1, D2, Q1, and Q2 (Figure 4).

A partial approach to battery-load switching can connect the AC power adapter (DC) directly to the load, but not USB power (Figure 5). This can be useful when USB power is insufficient to fully power the system and charge the battery. When DC is powered, D2 provides a direct connection to the system and Q3 disconnects the battery. The battery does not power the load while it is charging. When only USB is connected, there is no bypass path from USB to the system. The battery is charged from the BATT output, and any system power is drawn from the battery through D5. If the system load exceeds the current supplied by the charger from USB (500mA or 100mA), then the battery can still discharge. In addition, if the system load does not allow the BATT current to fall below the USB battery full current threshold listed in Table 2, then $\overline{CHG}$ does not go high to indicate a full battery.

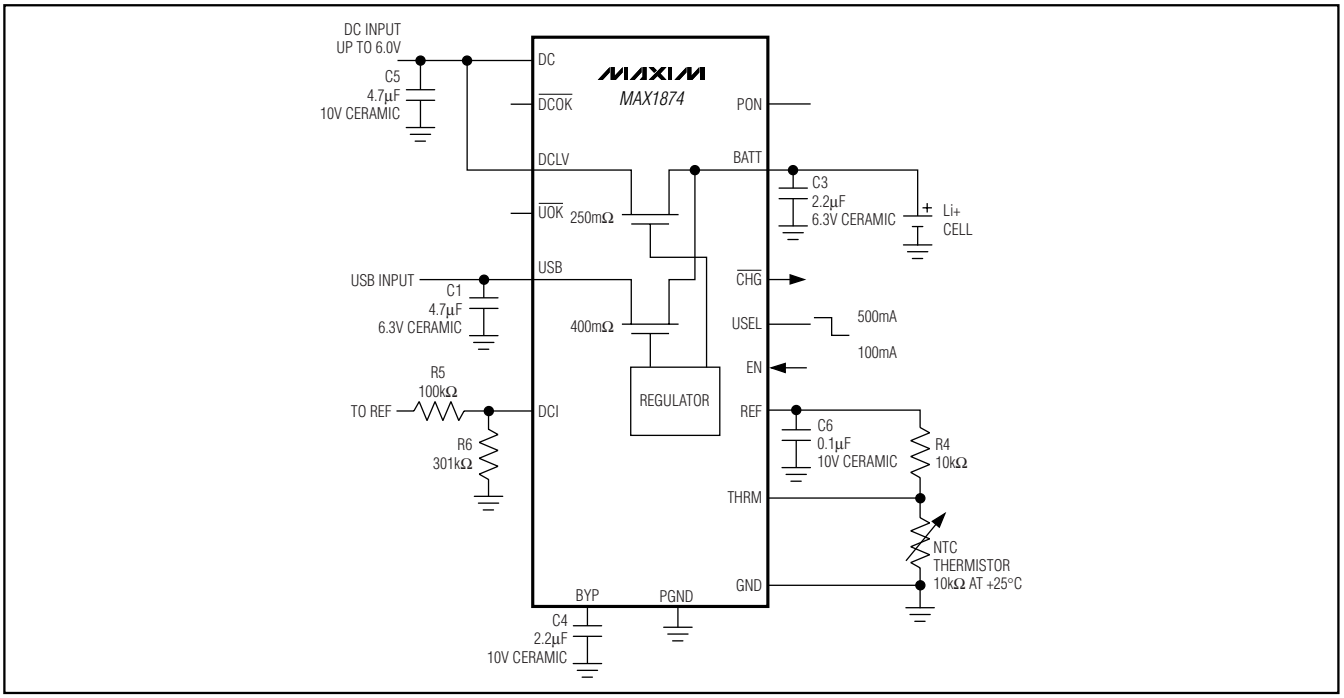



*Figure 2. A Minimal Circuit that Assumes System Load Is Only Connected to the Battery. The circuit has a 6.5V maximum input and disables charging for inputs over 6.2V.*

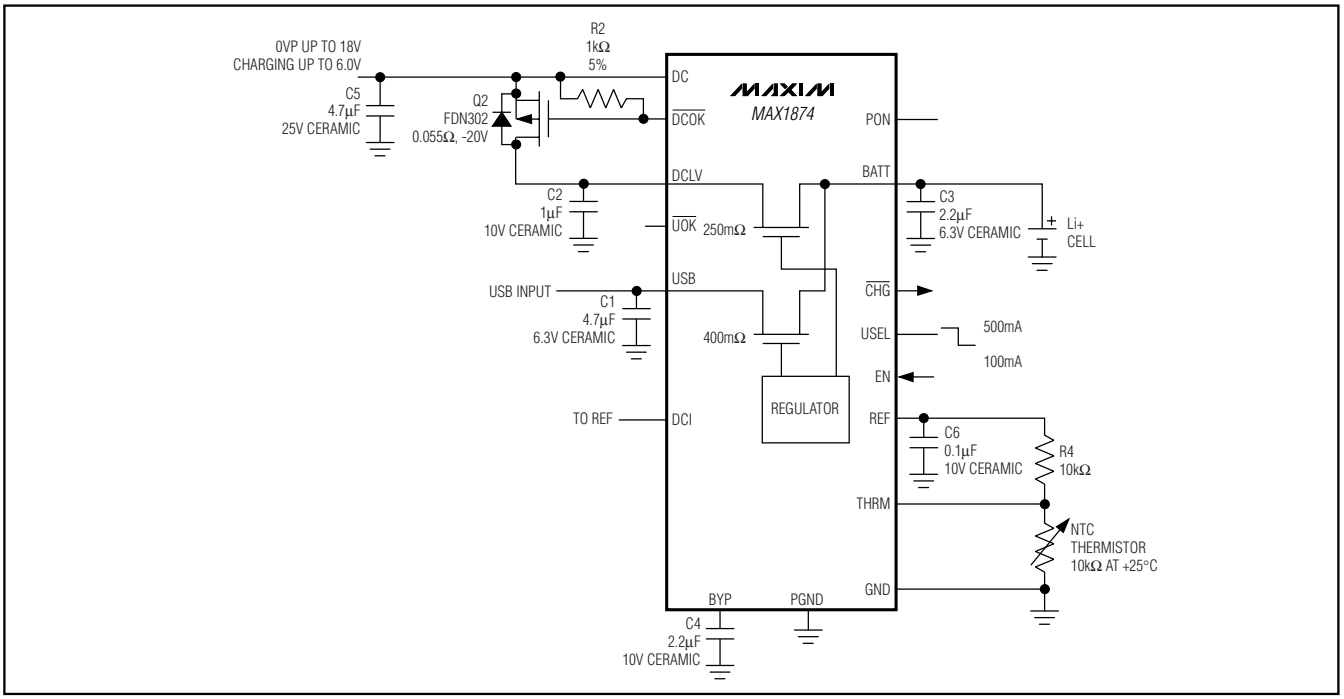



*Figure 3. A circuit with overvoltage protection MOSFET (Q2) on DC input withstands up to 18V from the AC adapter and disables charging at inputs over 6.2V.*

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

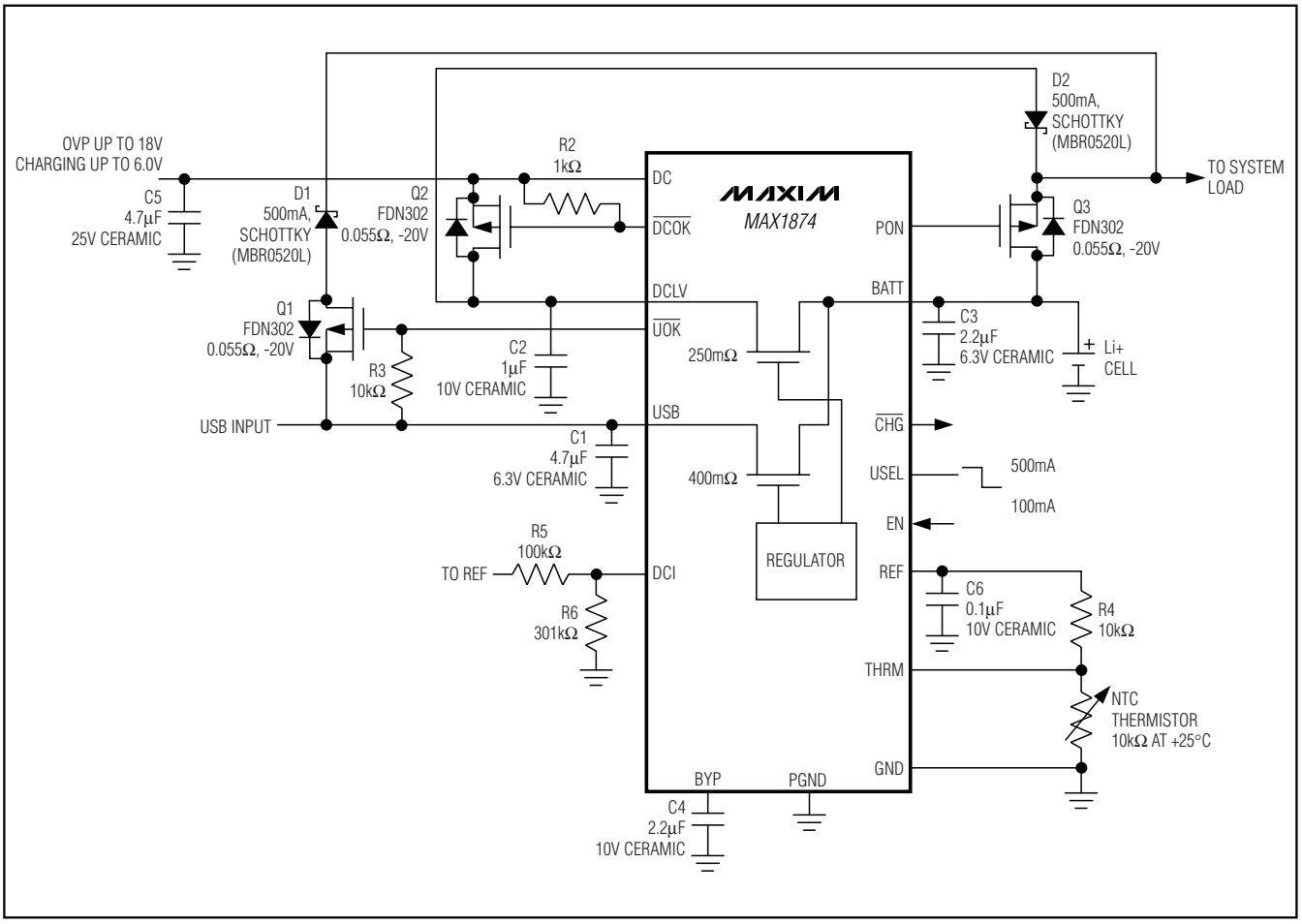



*Figure 4. Full-Featured Circuit. Overvoltage protection MOSFET (Q2) on DC withstands up to 18V from the AC adapter, but disables charging at inputs over 6.2V. Output switch-over MOSFET (Q3) disconnects the battery from the system load when input power is applied. The input can power the system through D1, D2, Q1, and Q2 when either USB or AC power is present.*

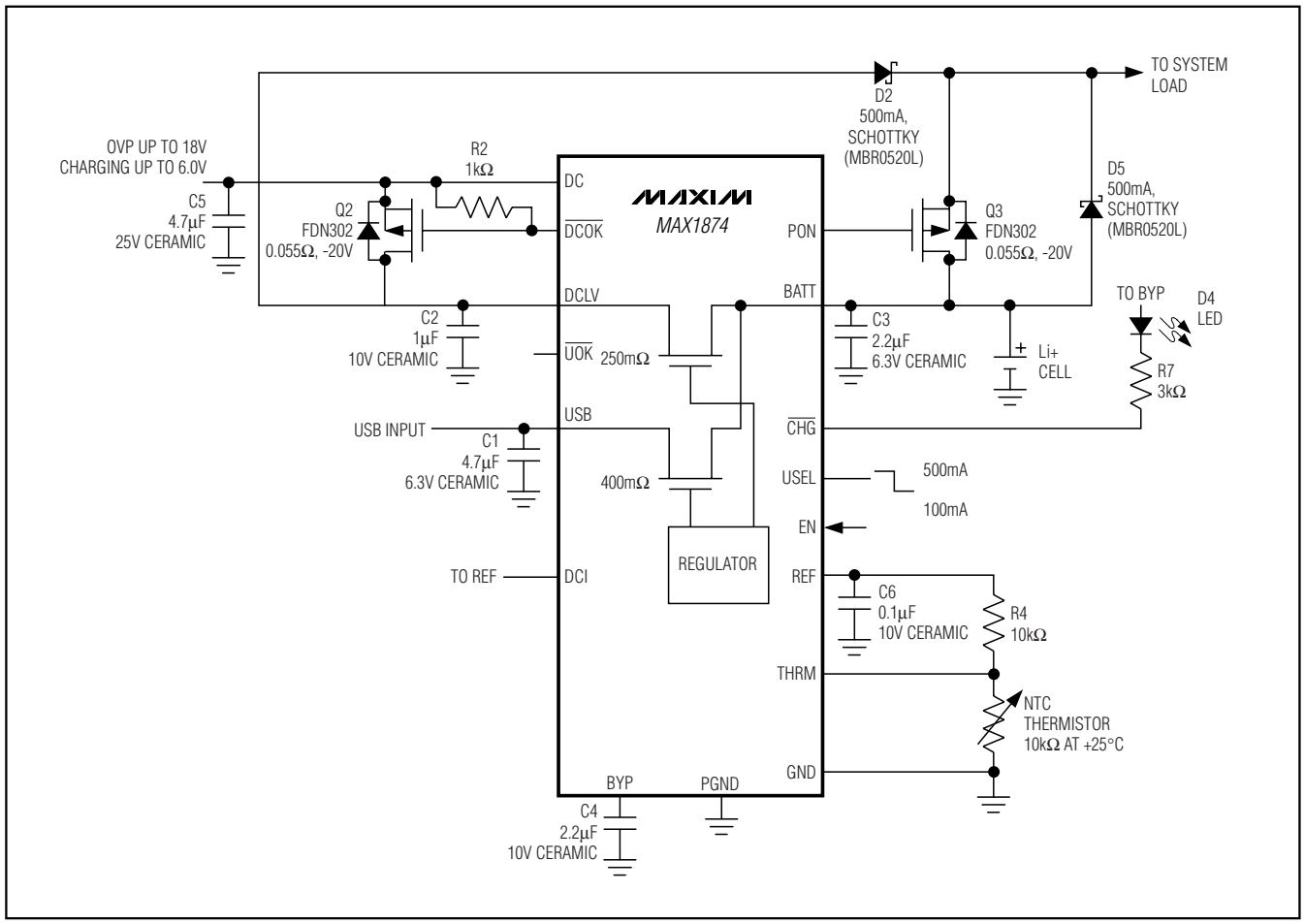



*Figure 5. Partial-Battery Load Switching. AC adapter power is routed directly to the battery, but USB power is not. When USB power is connected, total USB current is limited to that set by USEL and system power is drawn from the battery through D5.*

## Chip Information

TRANSISTOR COUNT: 4997

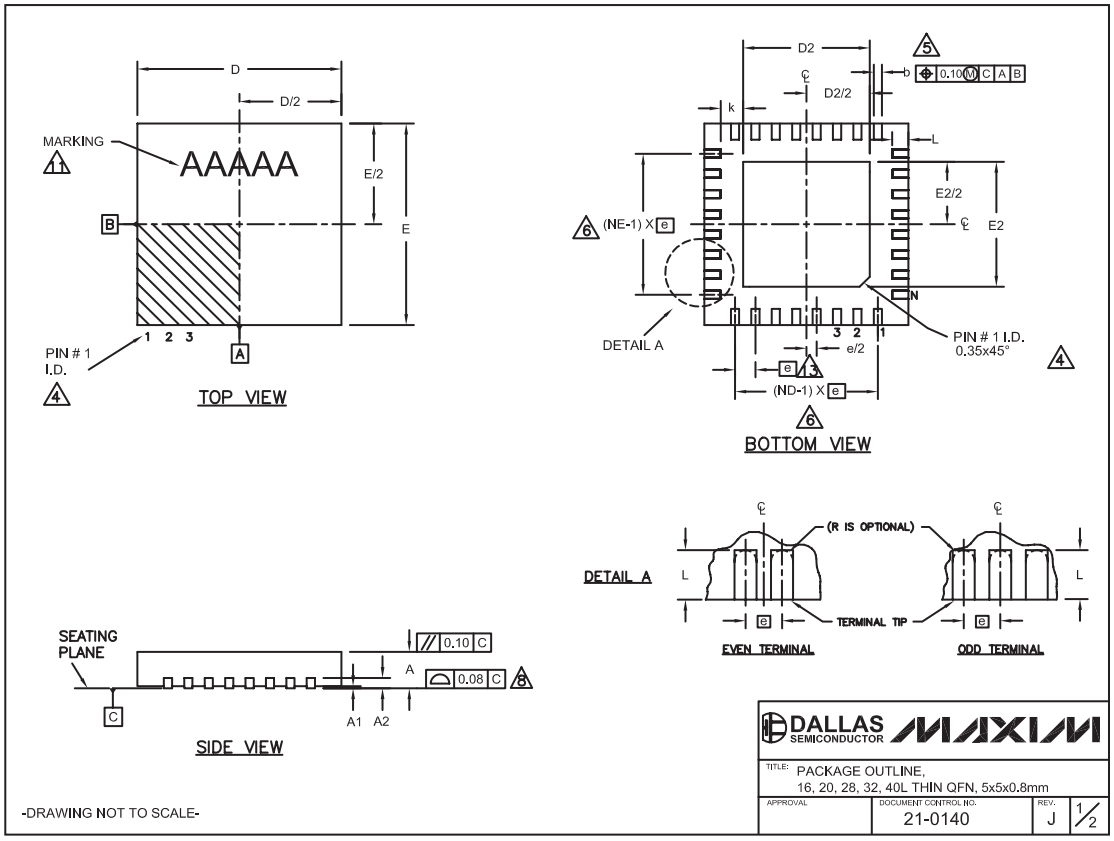
PROCESS: BICMOS

# Dual-Input, USB/AC Adapter, 1-Cell Li+ Charger with OVP and Thermal Regulation

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

| COMMON DIMENSIONS | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | | |
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 | |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 | |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | --- | | | |

| EXPOSED PAD VARIATIONS | | | | | | |
|---|---|---|---|---|---|---|
| PKG. CODES | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | J | 2/2 |

## Revision History

Pages changed at Rev 1: 1, 10, 11, 12, 14, 16