

# DS36C279

## Low Power EIA-RS-485 Transceiver with Sleep Mode

### General Description

The DS36C279 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The sleep mode feature automatically puts the device in a power saving mode when both the driver and receiver are disabled.†† The device is ideal for use in power conscious applications where the device may be disabled for extended periods of time.

The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of -7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into a high impedance state.

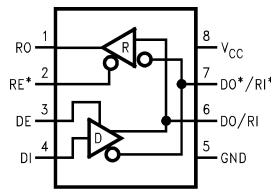
The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open.†

The DS36C279T is fully specified over the industrial temperature range (-40°C to +85°C).

### Features

- 100% RS-485 compliant
  - Guaranteed RS-485 device interoperation
- Low power CMOS design:  $I_{CC}$  500  $\mu$ A max
- Automatic sensing sleep mode
  - Reduces  $I_{CC}$  to 10  $\mu$ A maximum
- Built-in power up/down glitch-free circuitry
  - Permits live transceiver intersection/displacement
- SOIC packages
- Industrial temperature range: -40°C to +85°C
- On-board thermal shutdown circuitry
  - Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range: -7V to +12V
- Receive open input fail-safe (Note 1)
- 1/4 unit load (DS36C279):  $\geq$  128 nodes
- 1/2 unit load (DS36C279T):  $\geq$  64 nodes
- ESD (Human Body Model):  $\geq$  2 kV
- Drop-in replacement for:
  - LTC485 MAX485 DS75176 DS3695

### Connection and Logic Diagram



01205301

Order Number DS36C279M, DS36C279TM  
See NS Package Number M08A

### Truth Table

DRIVER SECTION				
RE*	DE	DI	DO/RI	DO*/RI*
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE*	DE	RI-RI*	RO	
L	L	$\geq +0.2V$	H	
L	L	$\leq -0.2V$	L	
H	L	X	Z (Note 2)	
L	L	OPEN (Note 1)	H	

**Note 1:** Non-terminated, open input only

**Note 2:** Device enters sleep mode if enable conditions are held > 600 ns

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**Absolute Maximum Ratings** (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	+12V
Input Voltage (DE, RE*, & DI)	-0.5V to ( $V_{CC} + 0.5V$ )
Common Mode ( $V_{CM}$ )	
Driver Output/Receiver Input	$\pm 15V$
Input Voltage (DO/RI, DO*/RI*)	$\pm 14V$

Receiver Output Voltage	-0.5V to ( $V_{CC} + 0.5V$ )
Maximum Package Power Dissipation @ +25°C	
M Package 1190 mW, derate	9.5 mW/°C above +25°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 4 sec)	+260°C

**Recommended Operating Conditions**

	Min	Typ	Max	Units		Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	+4.75	+5.0	+5.25	V	DS36C279T	-40	+25	+85	°C
Bus Voltage	-7		+12	V	DS36C279	0	+25	+70	°C
Operating Free Air Temperature ( $T_A$ )									

**Electrical Characteristics** (Notes 4, 5)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units	
<b>DIFFERENTIAL DRIVER CHARACTERISTICS</b>								
$V_{OD1}$	Differential Output Voltage	$I_O = 0$ mA (No Load)	(422)	1.5		5.0	V	
$V_{OD0}$	Output Voltage	$I_O = 0$ mA (Output to GND)	(485)	0		5.0	V	
$V_{OD0^*}$	Output Voltage			0		5.0	V	
$V_{OD2}$	Differential Output Voltage (Termination Load)	$R_L = 50\Omega$	(422)	Figure 1	2.0	2.8	V	
		$R_L = 27\Omega$	(485)		1.5	2.3	5.0	V
$\Delta V_{OD2}$	Balance of $V_{OD2}$ $ V_{OD2} - V_{OD2^*} $	$R_L = 27\Omega$ or $50\Omega$	(Note 6) (422, 485)	-0.2	0.1	+0.2	V	
$V_{OD3}$	Differential Output Voltage (Full Load)	$R1 = 54\Omega$ , $R2 = 375\Omega$ $V_{TEST} = -7V$ to $+12V$	Figure 2	1.5	2.0	5.0	V	
$V_{OC}$	Driver Common Mode Output Voltage	$R_L = 27\Omega$	(485)	Figure 1	0		3.0	V
		$R_L = 50\Omega$	(422)		0		3.0	V
$\Delta V_{OC}$	Balance of $V_{OC}$ $ V_{OC} - V_{OC^*} $	$R_L = 27\Omega$ or $R_L = 50\Omega$	(Note 6) (422, 485)	-0.2		+0.2	V	
$I_{OSD}$	Driver Output Short-Circuit Current	$V_O = +12V$	(485) Figure 4		200	+250	mA	
		$V_O = -7V$	(485)		-190	-250	mA	
<b>RECEIVER CHARACTERISTICS</b>								
$V_{TH}$	Differential Input High Threshold Voltage	$V_O = V_{OH}$ , $I_O = -0.4$ mA $-7V \leq V_{CM} \leq +12V$	(Note 7)		+0.035	+0.2	V	
$V_{TL}$	Differential Input Low Threshold Voltage	$V_O = V_{OL}$ , $I_O = 0.4$ mA $-7V \leq V_{CM} \leq +12V$	(422, 485)	-0.2	-0.035		V	
$V_{HST}$	Hysteresis	$V_{CM} = 0V$	(Note 8)		70		mV	
$R_{IN}$	Input Resistance	$-7V \leq V_{CM} \leq +12V$	DS36C279T		24	68	k $\Omega$	
			DS36C279		48	68	k $\Omega$	
$I_{IN}$	Line Input Current (Note 9)	Other Input = 0V, DE = $V_{IL}$ , RE* = $V_{IL}$ , $V_{CC} = 4.75$ to $5.25$ or 0V	DS36C279	$V_{IN} = +12V$	0	0.19	0.25	mA
				$V_{IN} = -7V$	0	-0.1	-0.2	mA
			DS36C279T	$V_{IN} = +12V$	0	0.19	0.5	mA
				$V_{IN} = -7V$	0	-0.1	-0.4	mA
$I_{ING}$	Line Input Current Glitch (Note 9)	Other Input = 0V, DE = $V_{IL}$ , RE* = $V_{IL}$ ,	DS36C279	$V_{IN} = +12V$	0	0.19	0.25	mA
				$V_{IN} = -7V$	0	-0.1	-0.2	mA

**Electrical Characteristics** (Notes 4, 5) (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units	
<b>RECEIVER CHARACTERISTICS</b>								
		$V_{CC} = +3.0V$ or $0V$ , $T_A = 25^\circ C$	DS36C279T	$V_{IN} = +12V$	0	0.19	0.5	mA
				$V_{IN} = -7V$	0	-0.1	-0.4	mA
$I_B$	Input Balance Test	$RS = 500\Omega$	(422) (Note 12)			$\pm 400$	mV	
$V_{OH}$	High Level Output Voltage	$I_{OH} = -4$ mA, $V_{ID} = +0.2V$	RO Figure 11	3.5	4.6		V	
$V_{OL}$	Low Level Output Voltage	$I_{OL} = +4$ mA, $V_{ID} = -0.2V$			0.3	0.5	V	
$I_{OSR}$	Short Circuit Current	$V_O = GND$	RO	7	35	85	mA	
$I_{OZR}$	TRI-STATE Leakage Current	$V_O = 0.4V$ to $2.4V$				$\pm 1$	$\mu A$	
<b>DEVICE CHARACTERISTICS</b>								
$V_{IH}$	High Level Input Voltage		DE, RE*, DI	2.0		$V_{CC}$	V	
$V_{IL}$	Low Level Input Voltage			GND		0.8	V	
$I_{IH}$	High Level Input Current	$V_{IH} = V_{CC}$				2	$\mu A$	
$I_{IL}$	Low Level Input Current	$V_{CC} = 5V$	$V_{IL} = 0V$			-2	$\mu A$	
		$V_{CC} = +3.0V$				-2	$\mu A$	
$I_{CC}$	Power Supply Current (No Load)	Driver and Receiver ON	$V_{CC}$		200	500	$\mu A$	
$I_{CCR}$		Driver OFF, Receiver ON			200	500	$\mu A$	
$I_{CCD}$		Driver ON, Receiver OFF			200	500	$\mu A$	
$I_{CCX}$		Sleep Mode			0.2	10	$\mu A$	

**Switching Characteristics** (Notes 5, 10)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
<b>DRIVER CHARACTERISTICS</b>							
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 54\Omega$ , $C_L = 100$ pF	Figures 5, 6	10	39	80	ns
$t_{PLHD}$	Differential Propagation Delay Low to High			10	40	80	ns
$t_{SKD}$	Differential Skew $ t_{PHLD} - t_{PLHD} $			0	1	10	ns
$t_r$	Rise Time			3	25	50	ns
$t_f$	Fall Time			3	25	50	ns
$t_{PHZ}$	Disable Time High to Z	$C_L = 15$ pF	Figures 7, 8		80	200	ns
$t_{PLZ}$	Disable Time Low to Z	$RE^* = L$	Figures 9, 10		80	200	ns
$t_{PZH}$	Enable Time Z to High	$C_L = 100$ pF	Figures 7, 8		50	200	ns
$t_{PZL}$	Enable Time Z to Low	$RE^* = L$	Figures 9, 10		65	200	ns
$t_{PSH}$	Driver Enable from Sleep Mode to Output High	$C_L = 100$ pF (Note 11)	Figures 7, 8	70	98	250	ns
$t_{PSL}$	Driver Enable from Sleep Mode to Output Low	$C_L = 100$ pF (Note 11)	Figures 9, 10	70	98	250	ns
<b>RECEIVER CHARACTERISTICS</b>							
$t_{PHL}$	Propagation Delay High to Low	$C_L = 15$ pF	Figures 12, 13	30	210	400	ns
$t_{PLH}$	Propagation Delay Low to High			30	190	400	ns
$t_{SK}$	Skew, $ t_{PHL} - t_{PLH} $			0	20	50	ns

## Switching Characteristics (Notes 5, 10) (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
<b>RECEIVER CHARACTERISTICS</b>							
$t_{PLZ}$	Output Disable Time	$C_L = 15 \text{ pF}$ $DE = H$	<i>Figures 14, 15, 16</i>		50	150	ns
$t_{PHZ}$					55	150	ns
$t_{PZL}$	Output Enable Time				40	150	ns
$t_{PZH}$					45	150	ns
$t_{PSH}$	Receiver Enable from Sleep Mode to Output High	$C_L = 15 \text{ pF}$ (Note 11)	<i>Figures 14, 16</i>	70	97	250	ns
$t_{PSL}$	Receiver Enable from Sleep Mode to Output Low	$C_L = 15 \text{ pF}$ (Note 11)	<i>Figures 14, 15</i>	70	95	250	ns

**Note 3:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 4:** Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD1}$  and  $V_{OD2}$ .

**Note 5:** All typicals are given for:  $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$ .

**Note 6:** Delta  $|V_{OD2}|$  and Delta  $|V_{OC}|$  are changes in magnitude of  $V_{OD2}$  and  $V_{OC}$ , respectively, that occur when input changes state.

**Note 7:** Threshold parameter limits specified as an algebraic value rather than by magnitude.

**Note 8:** Hysteresis defined as  $V_{HST} = V_{TH} - V_{TL}$ .

**Note 9:**  $I_{IN}$  includes the receiver input current and driver TRI-STATE leakage current.

**Note 10:**  $C_L$  includes probe and jig capacitance.

**Note 11:** For enable from sleep mode delays  $DE = L$  and  $RE^* = H$  for greater than 600 ns prior to test (device is in sleep mode).

**Note 12:** For complete details of test, see RS-485.

## Parameter Measurement Information

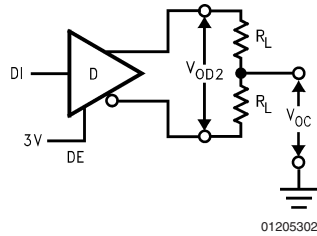


FIGURE 1. Driver  $V_{OD2}$  and  $V_{OC}$

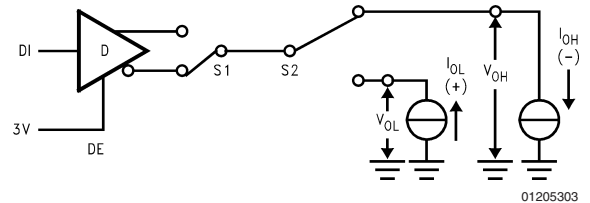


FIGURE 3. Driver  $V_{OH}$  and  $V_{OL}$

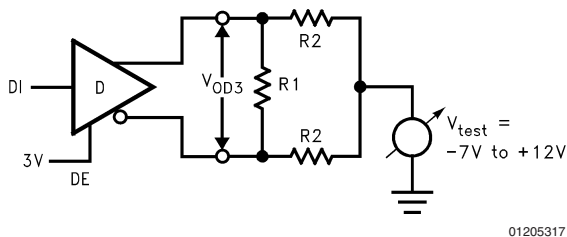


FIGURE 2. Driver  $V_{OD3}$

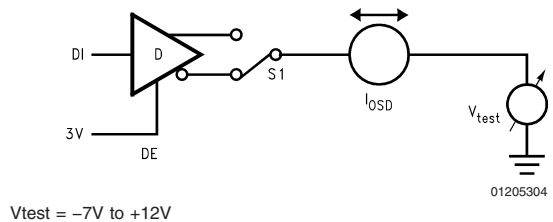
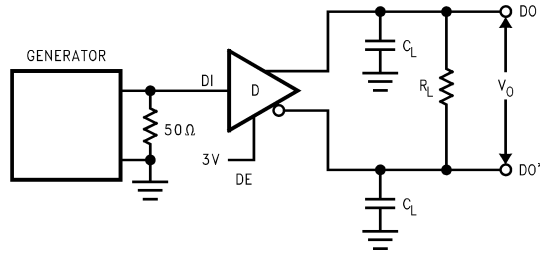


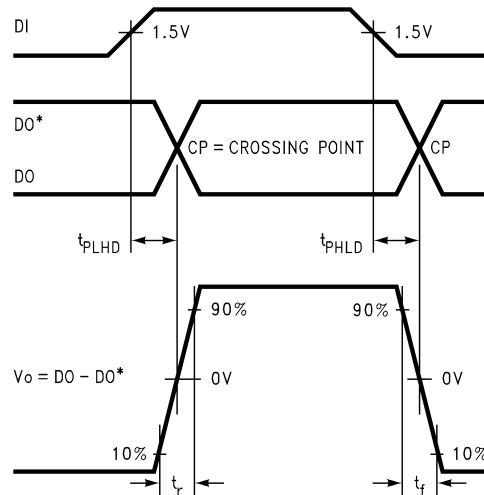
FIGURE 4. Driver  $I_{ODS}$

Parameter Measurement Information (Continued)



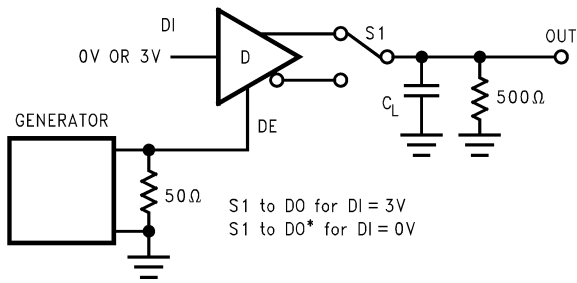
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FIGURE 5. Driver Differential Propagation Delay Test Circuit



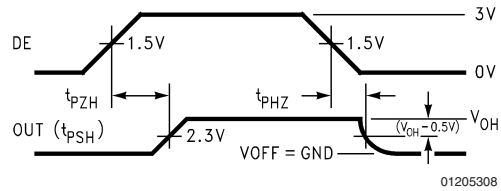
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FIGURE 6. Driver Differential Propagation Delays and Differential Rise and Fall Times



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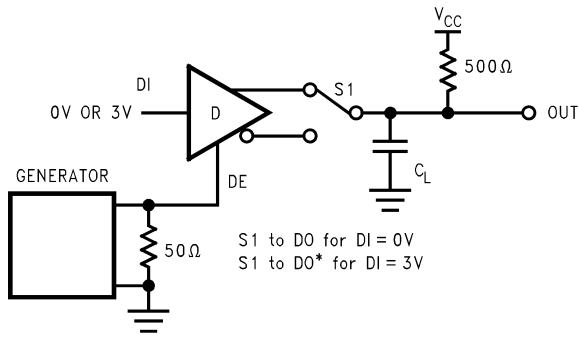
FIGURE 7. TRI-STATE and Sleep Mode Test Circuit  
( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )



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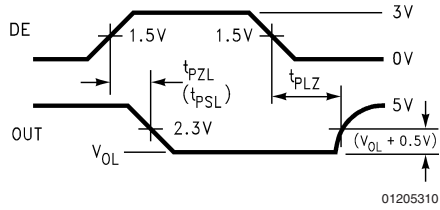
FIGURE 8. TRI-STATE and Sleep Mode Waveforms  
( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )

# Parameter Measurement Information (Continued)



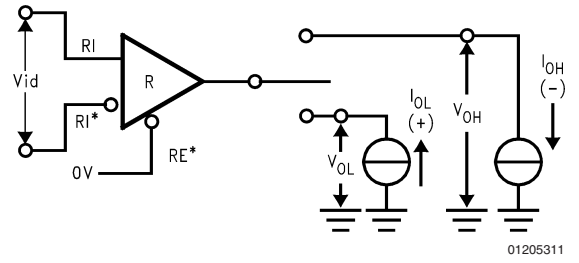
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**FIGURE 9. TRI-STATE and Sleep Mode Test Circuit**  
( $t_{PZL}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )



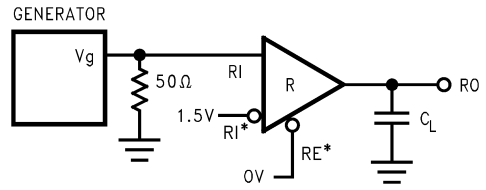
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**FIGURE 10. TRI-STATE and Sleep Mode Waveforms**  
( $t_{PZL}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )



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**FIGURE 11. Receiver  $V_{OH}$  and  $V_{OL}$**



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**FIGURE 12. Receiver Differential Propagation Delay Test Circuit**

Parameter Measurement Information (Continued)

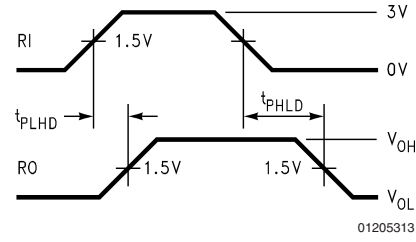


FIGURE 13. Receiver Differential Propagation Delay Waveforms

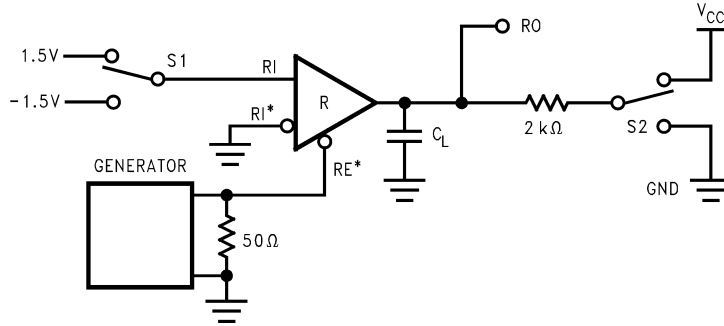


FIGURE 14. Receiver TRI-STATE and Sleep Mode Test Circuit

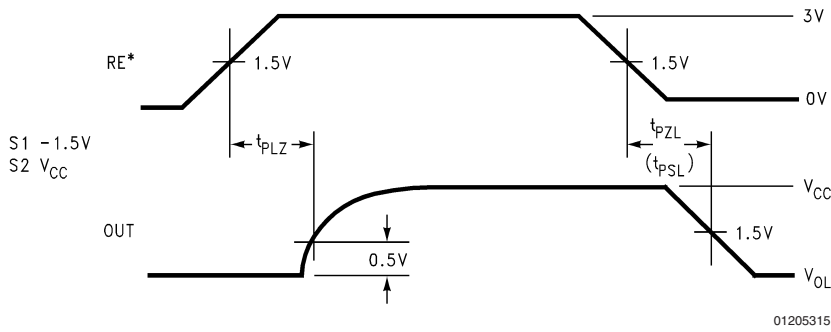


FIGURE 15. Receiver Enable and Disable Waveforms ( $t_{PLZ}$ ,  $t_{PZL}$ ,  $t_{PSL}$ )

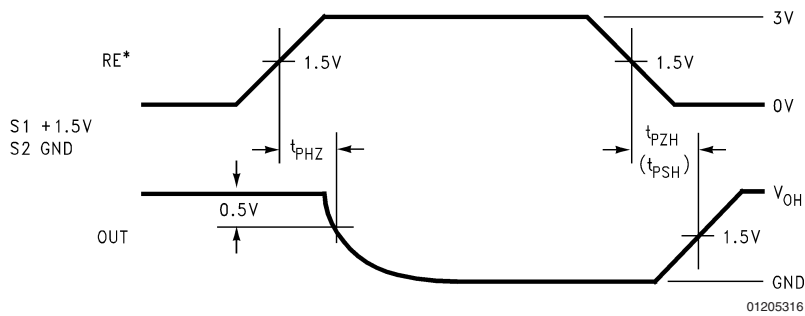


FIGURE 16. Receiver Enable and Disable Waveforms ( $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PSH}$ )

## Parameter Measurement Information (Continued)

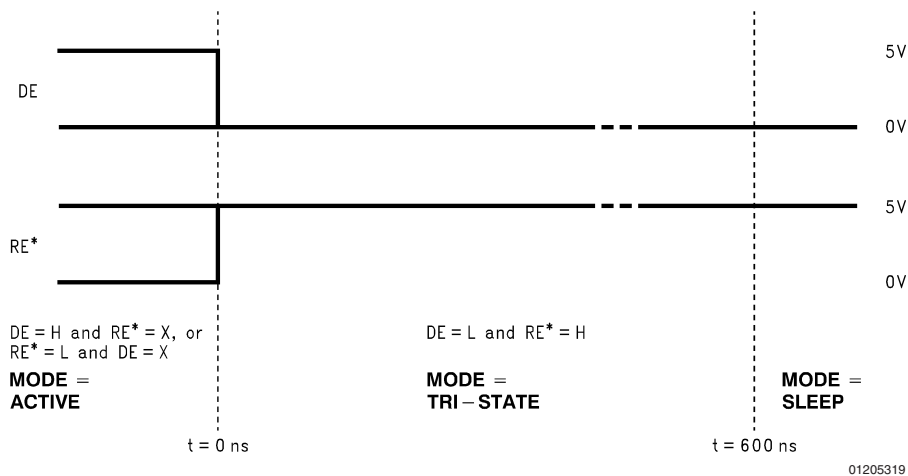


FIGURE 17. Entering Sleep Mode Conditions

## Typical Application Information

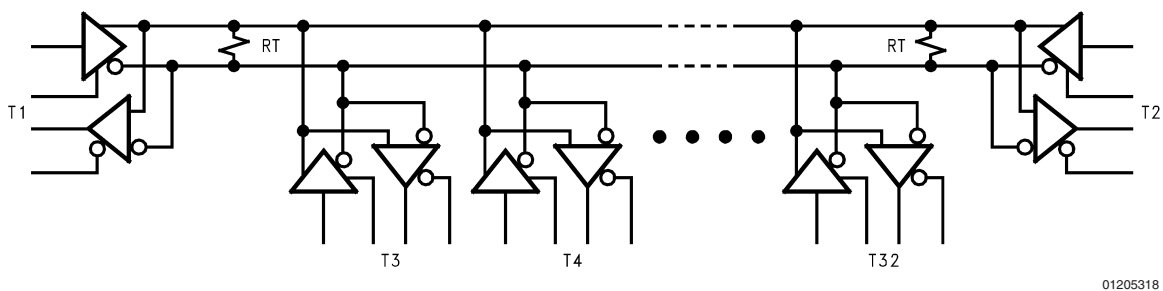


FIGURE 18. Typical RS-485 Bus Interface

TABLE 1. Device Pin Descriptions

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI $\geq$ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI $\leq$ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
2	RE*	Receiver Output Enable: When RE* is LOW the receiver output is enabled. When RE* is HIGH, the receiver output is in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection.
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V <sub>CC</sub>	Positive Power Supply Connection: Recommended operating range for V <sub>CC</sub> is +4.75V to +5.25V.



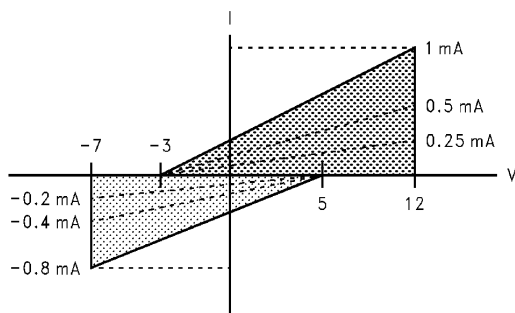
## Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from  $-7\text{V}$  to  $+12\text{V}$ . The top border extending from  $-3\text{V}$  at  $0\text{ mA}$  to  $+12\text{V}$  at  $+1\text{ mA}$  is defined as one unit load. Likewise, the bottom border extending from  $+5\text{V}$  at  $0\text{ mA}$  to  $-7\text{V}$  at  $-0.8\text{ mA}$  is also defined as one unit load (see *Figure 19*). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes. For example, an aircraft that has 32 rows with 4 seats per row would benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have  $\frac{1}{2}$  unit load and  $\frac{1}{4}$  unit load (UL) options available. These devices will allow up to 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The  $\frac{1}{2}$  UL option is available in industrial temperature and the  $\frac{1}{4}$  UL is available in commercial temperature.

First, for a  $\frac{1}{2}$  UL device the top and bottom borders shown in *Figure 19* are scaled. Both  $0\text{ mA}$  reference points at  $+5\text{V}$  and  $-3\text{V}$  stay the same. The other reference points are  $+12\text{V}$  at  $+0.5\text{ mA}$  for the top border and  $-7\text{V}$  at  $-0.4\text{ mA}$  for the bottom border (see *Figure 19*). Second, for a  $\frac{1}{4}$  UL device the top and bottom borders shown in *Figure 19* are scaled also. Again, both  $0\text{ mA}$  reference points at  $+5\text{V}$  and  $-3\text{V}$  stay the same. The other reference points are  $+12\text{V}$  at  $+0.25\text{ mA}$  for the top border and  $-7\text{V}$  at  $-0.2\text{ mA}$  for the bottom border (see *Figure 19*).

The advantage of the  $\frac{1}{2}$  UL and  $\frac{1}{4}$  UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.



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**FIGURE 19. Input Current vs Input Voltage Operating Range**

The DS36C279 and DS36C280 have an additional feature which offers more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

## Sleep Mode

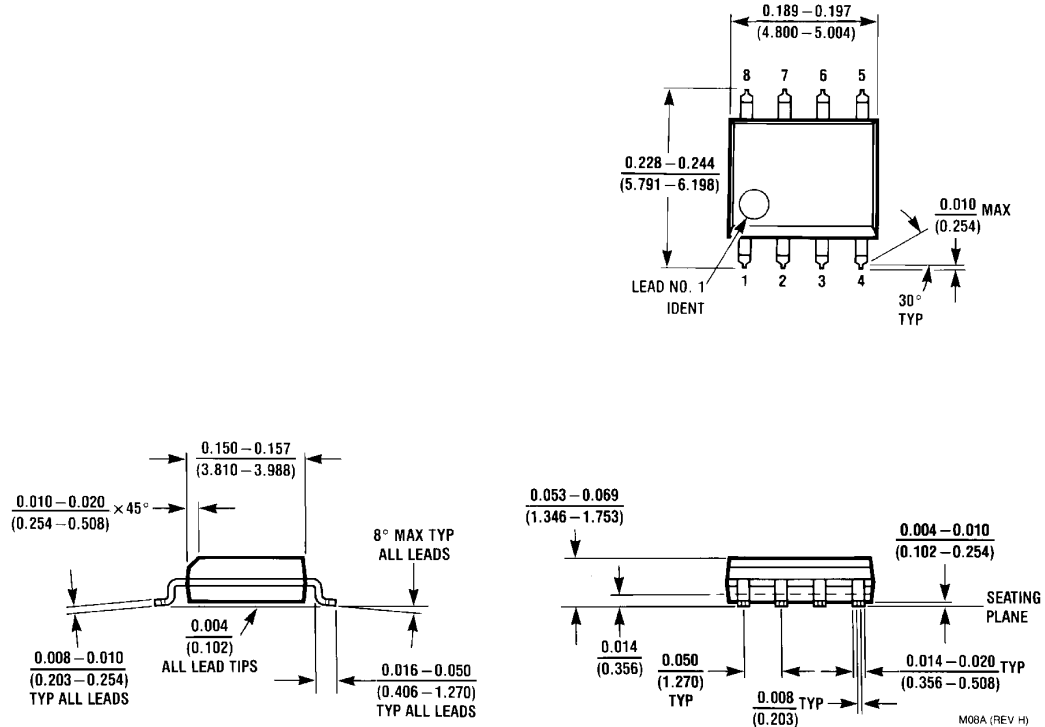
The DS36C279 features an automatic shutdown mode that allows the device to save power when not transmitting data. Since the shutdown mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the RE\* pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode typically in 50 ns. The DS36C279 is guaranteed to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the RE\* pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to datasheet specifications  $t_{PSL}$  and  $t_{PSH}$  and compare with  $t_{PZL}$  and  $t_{PZH}$  for timing differences.

The benefit of the DS36C279 is definitely its power savings. When active the device has a maximum  $I_{CC}$  of  $500\text{ }\mu\text{A}$ . When in sleep mode the device has a maximum  $I_{CC}$  of only  $10\text{ }\mu\text{A}$ , which is 50 times less power than when active. The  $I_{CC}$  when the device is active is already very low but when in sleep mode the  $I_{CC}$  is ultra low.

## Physical Dimensions inches (millimeters)

unless otherwise noted



**8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC**  
**Order Number DS36C279M or DS36C279TM**  
**NS Package Number M08A**

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