

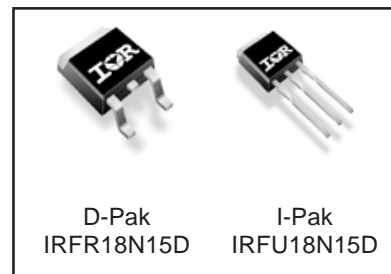
**Applications**

- | High frequency DC-DC converters

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>150V</b>	<b>0.125Ω</b>	<b>18A</b>

**Benefits**

- | Low Gate to Drain Charge to Reduce Switching Losses
- | Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- | Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	18	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	13	
I <sub>DM</sub>	Pulsed Drain Current	72	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt <i>f</i>	3.3	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Typical SMPS Topologies**

- | Telecom 48V input DC-DC Active Clamp Reset Forward Converter

Notes through † are on page 10

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# IRFR18N15D/IRFU18N15D

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Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ †
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.125	$\Omega$	$V_{GS} = 10V, I_D = 11A$ „
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	4.2	—	—	S	$V_{DS} = 50V, I_D = 11A$
$Q_g$	Total Gate Charge	—	28	43	nC	$I_D = 11A$
$Q_{gs}$	Gate-to-Source Charge	—	7.6	11		$V_{DS} = 120V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	14	21		$V_{GS} = 10V, „$
$t_{d(on)}$	Turn-On Delay Time	—	8.8	—	ns	$V_{DD} = 75V$
$t_r$	Rise Time	—	25	—		$I_D = 11A$
$t_{d(off)}$	Turn-Off Delay Time	—	15	—		$R_G = 6.8\Omega$
$t_f$	Fall Time	—	9.8	—		$V_{GS} = 10V „$
$C_{iss}$	Input Capacitance	—	900	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	190	—		$V_{DS} = 25V$
$C_{rSS}$	Reverse Transfer Capacitance	—	49	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1160	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	88	—		$V_{GS} = 0V, V_{DS} = 120V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	95	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V \dots$

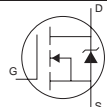
## Avalanche Characteristics

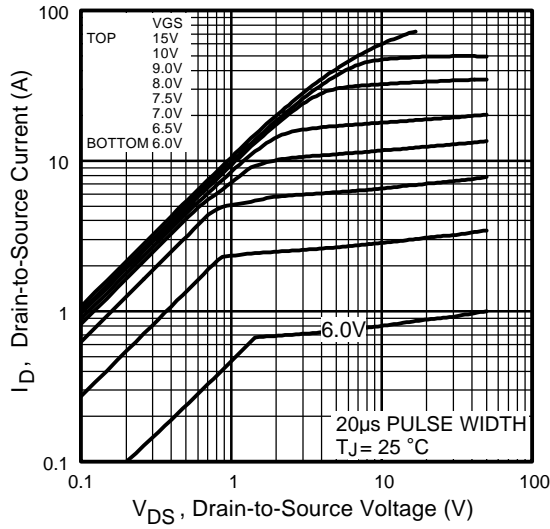
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy,	—	200	mJ
$I_{AR}$	Avalanche Current	—	11	A
$E_{AR}$	Repetitive Avalanche Energy	—	11	mJ

## Thermal Resistance

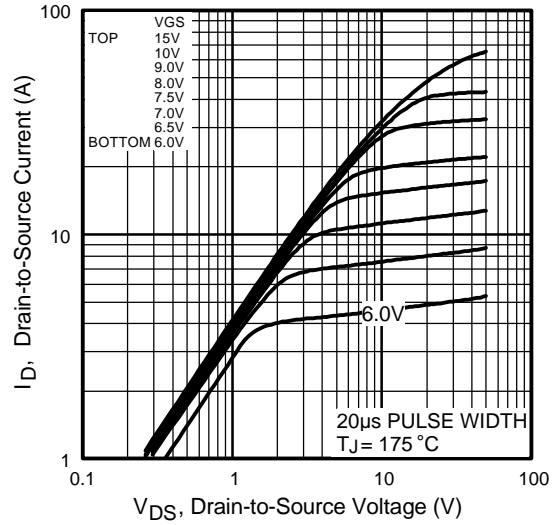
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

## Diode Characteristics

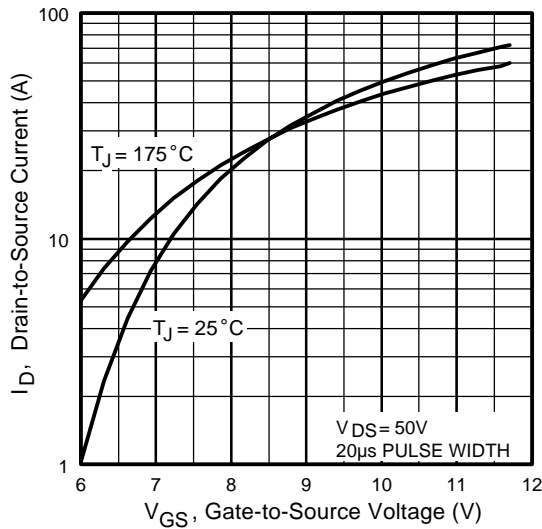
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	72		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V „$
$t_{rr}$	Reverse Recovery Time	—	130	190	ns	$T_J = 25^\circ\text{C}, I_F = 11A$
$Q_{rr}$	Reverse Recovery Charge	—	660	980	nC	$di/dt = 100A/\mu s „$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				



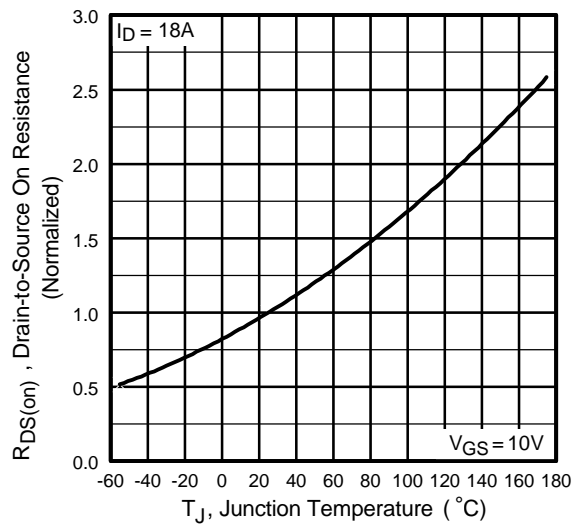
**Fig 1.** Typical Output Characteristics



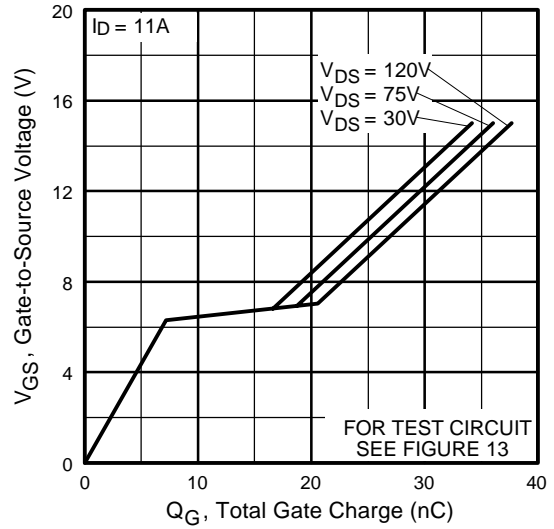
**Fig 2.** Typical Output Characteristics



**Fig 3.** Typical Transfer Characteristics

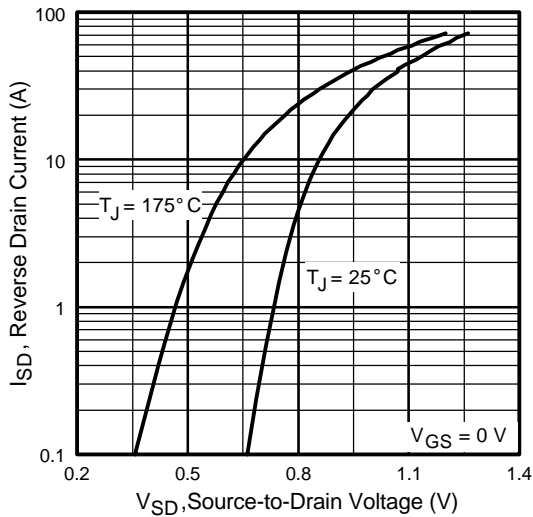


**Fig 4.** Normalized On-Resistance Vs. Temperature

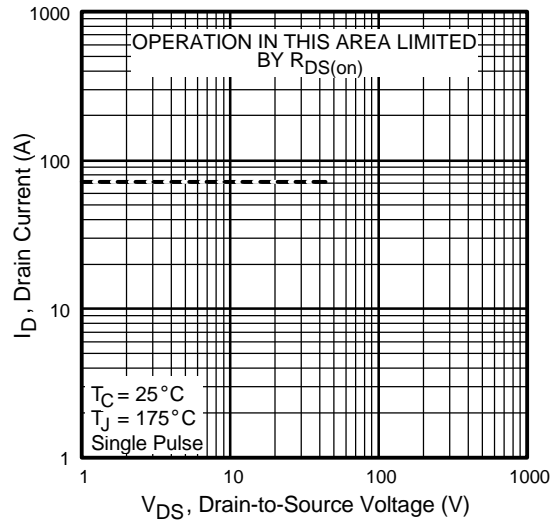


**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

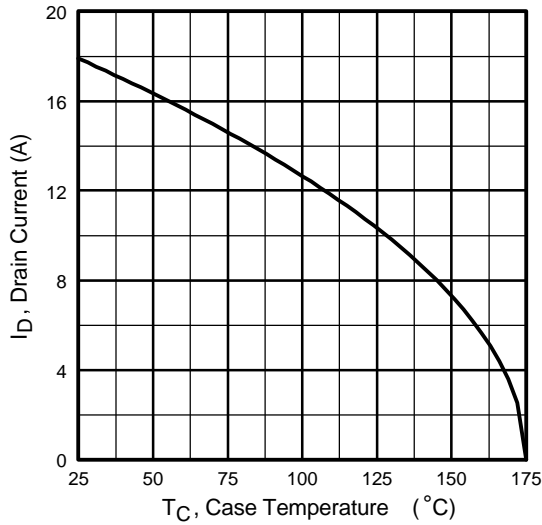
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



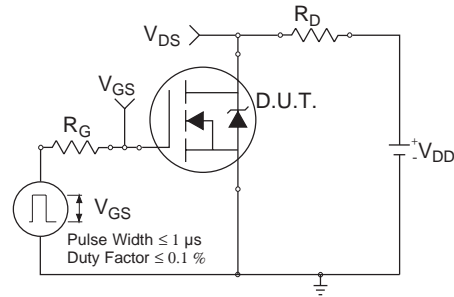
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



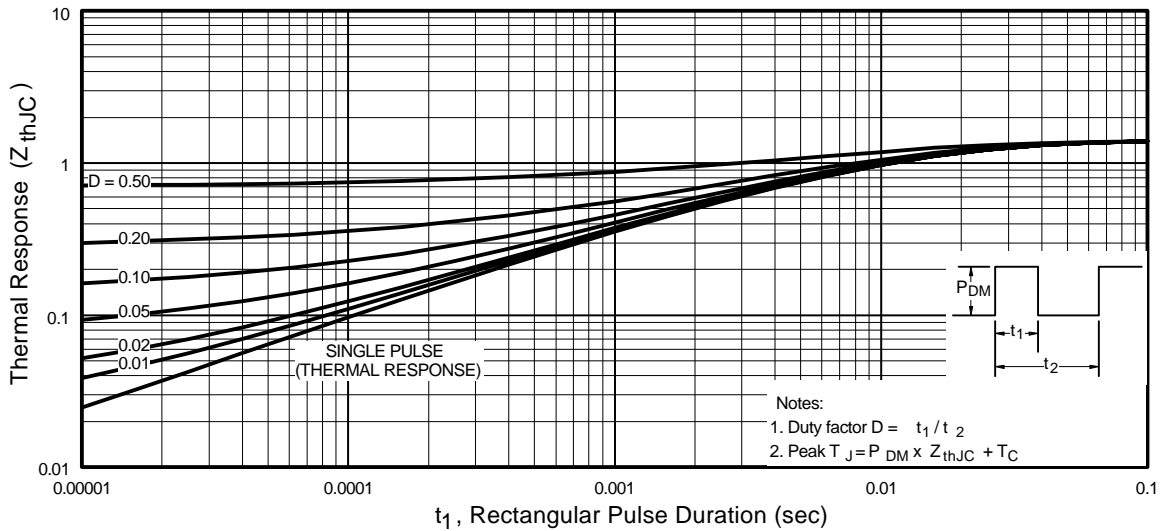
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



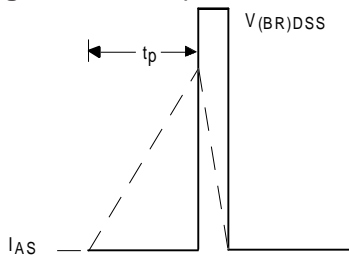
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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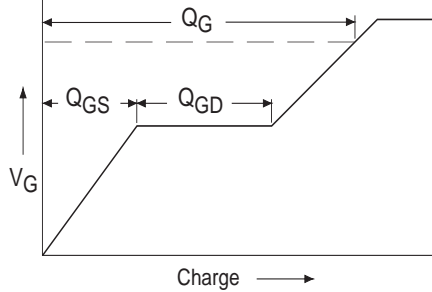
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**Fig 12a.** Unclamped Inductive Test Circuit



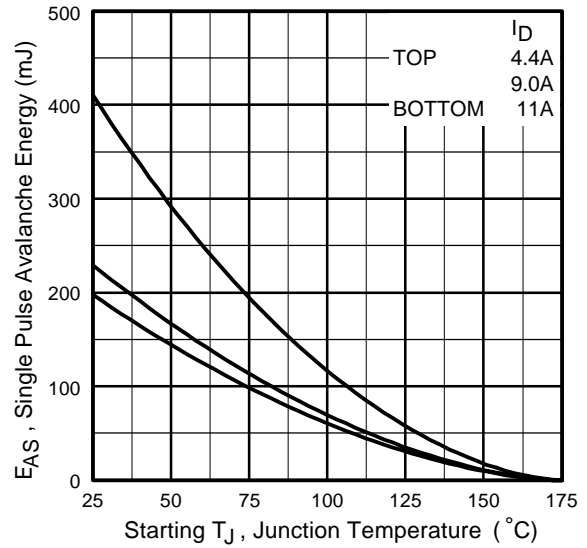
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

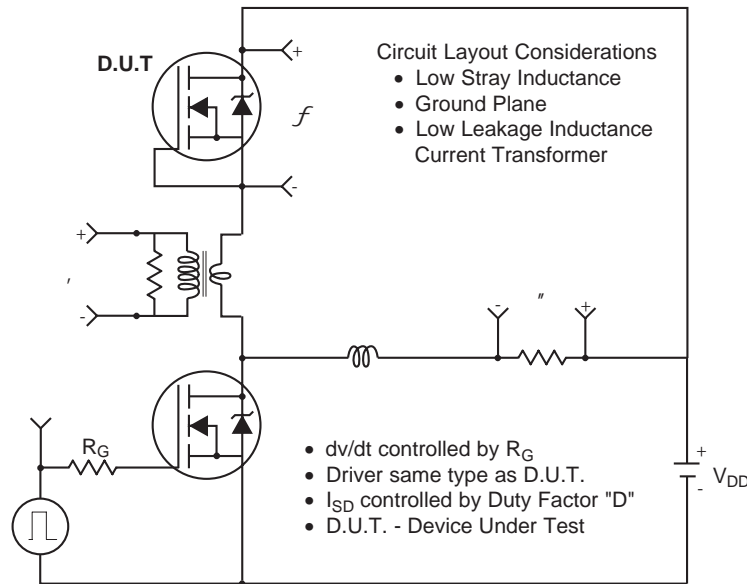


**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

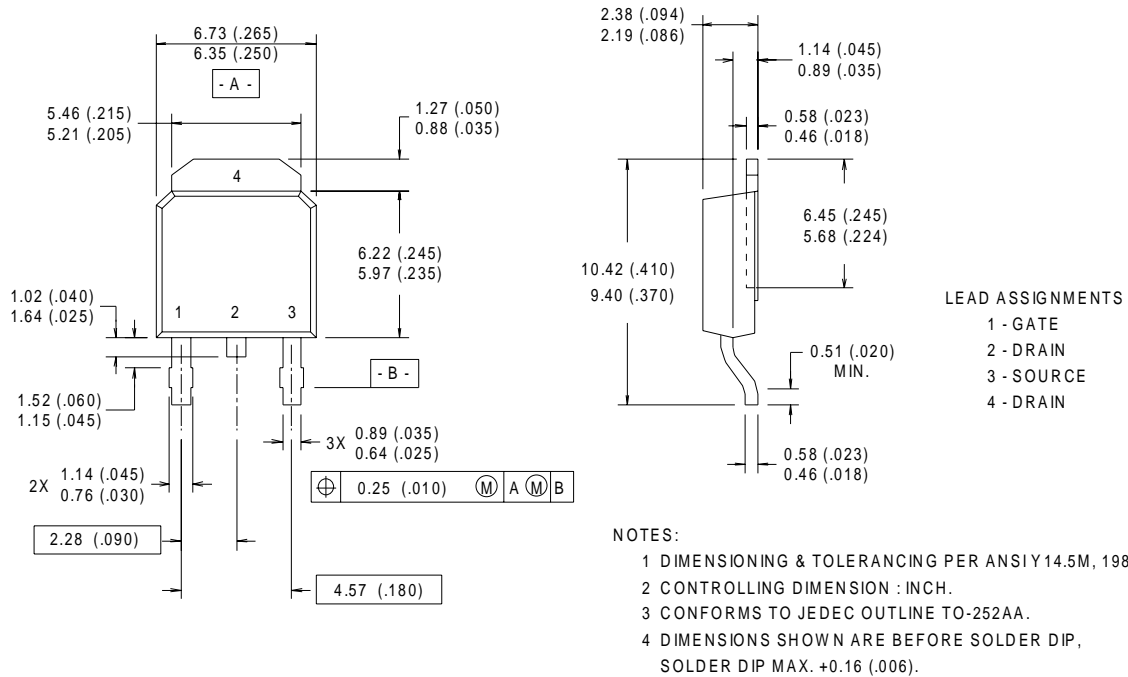
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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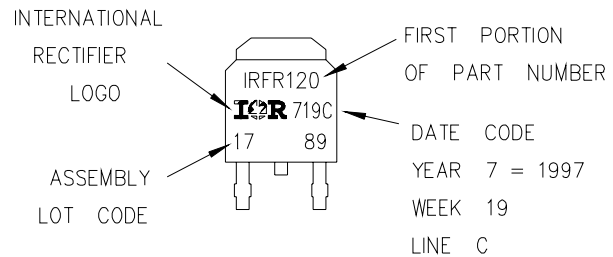
## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



## D-Pak (TO-252AA) Part Marking Information

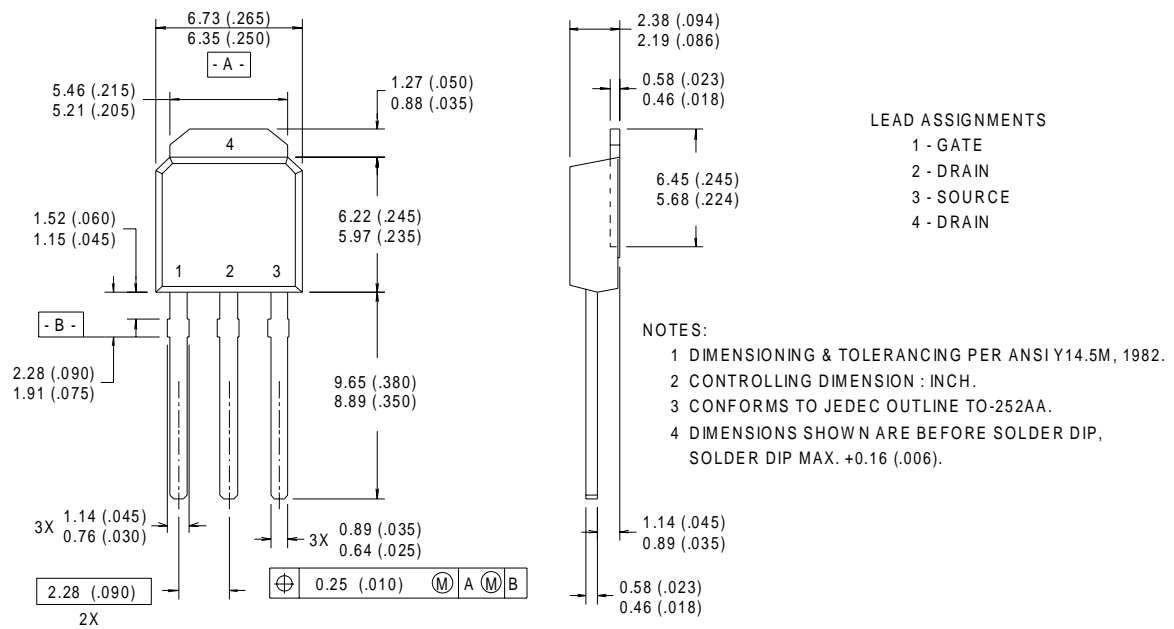
EXAMPLE: THIS IS AN IRFR120  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"





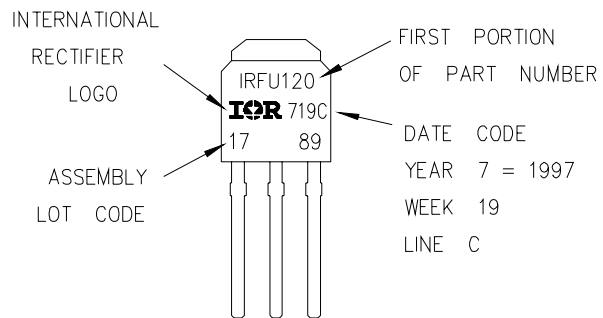
## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

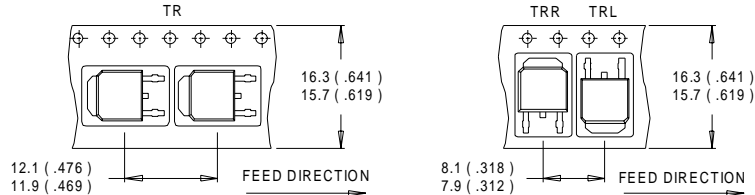


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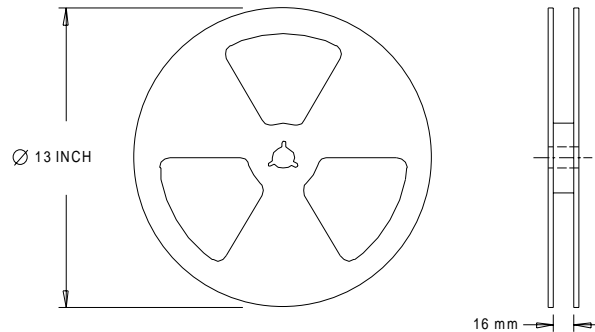
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- Repetitive rating; pulse width limited by max. junction temperature.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3.3\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 11\text{A}$ .
- $f$   $I_{SD} \leq 11\text{A}$ ,  $di/dt \leq 170\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- \* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- .. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ...  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

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**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

**IR JAPAN:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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**IR TAIWAN:** 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

*Data and specifications subject to change without notice. 2/00*