CS7401xx

# Energy Measurement SoC

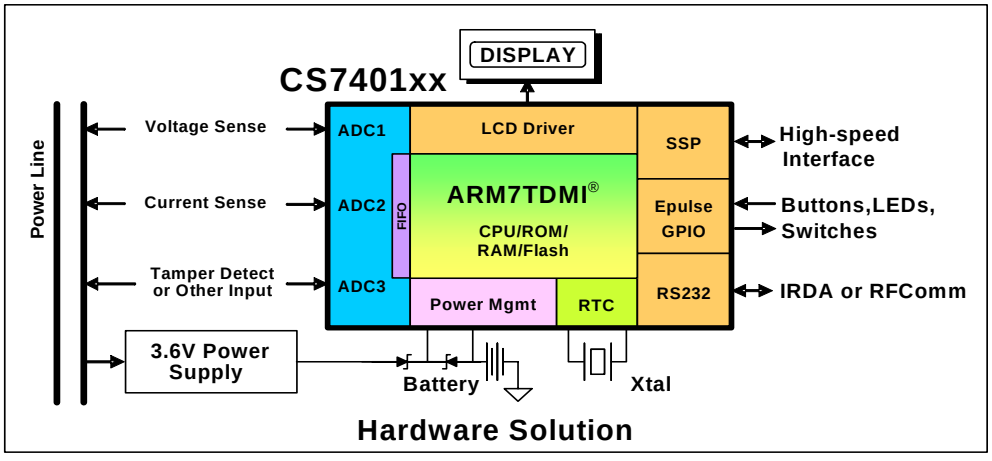
## Description

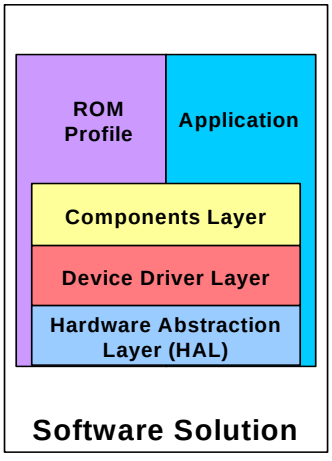
The CS7401xx energy measurement system-on-chip (SoC) device reduces the cost to implement advanced digital power meters for electrical utilities as well as enabling many other energy conservation applications. The 24-bit Delta-Sigma (ΔΣ) ADCs coupled with the on-chip metrology code enable the highest quality power measurement available. The 32-bit processor and targeted peripherals have the power to implement metrology, advanced data management standards, and communication protocols all in the same device. The extensive software library enables quick and easy program development.

## Features

- **Analog-to-Digital Converter**
  - Three Independent 24-bit Delta-Sigma ADCs
  - Selectable Sampling Rate (1 kHz-8 kHz)
  - FIFO for Buffered Data Collection
  - Voltage and Current Sampled Simultaneously
  - Third ADC can be used for Tamper Detection
  - On-chip Temperature Sensor
- **Analog Front End**
  - Single-ended or Differential Inputs
  - Programmable Gain (1x, 3x, 6x, 12x)
  - Supports 50 µΩ Shunts
  - 1.8V Reference Compensated to 10 ppm/°C
- **Measurement**
  - ANSI C12-20 / IEC 62053-22 Class 0.2% Accuracy
  - Active Power Accuracy ±0.1% Over 3000:1 Range
  - Fast Phase Calibration up to ±18° Range
  - Wide Frequency Range: 45 Hz to 70 Hz
  - Supports Total and Fundamental Measurements for Active, Reactive, and Apparent Power
- **Microcontroller Subsystem**
  - ARM7TDMI™ 16/32-bit RISC CPU
  - Dynamic Core Frequency from 4 MHz to 32 MHz
  - 32kB, 64kB, or 128kB On-chip Flash Memory
  - Flash Locking Mechanism to Protect User's Program
  - 8 kB On-chip RAM, 32kB On-chip ROM
  - Single 32 kHz Crystal with FLL to Internal Oscillator
  - Internal Oscillator: Robust Operation with EFT Events
  - On-chip Crystal Capacitors for Frequency Stability
  - JTAG Interface
- **On-chip Peripherals**
  - LCD Driver with up to 120 Segments (30 x 4)
  - RTC with Auto Calibration and 1Hz Output
  - Two UART Communications Ports
  - Configurable Sync Serial Port with SPI™ Mode
  - Programmable GPIOs, Timers, and Watchdog Timer
  - Dedicated Energy Pulse Output
- **ROM Profile**
  - Factory-ready Communications using UART0
  - Automated/Fast Calibration of Gain, Offset, and Phase
  - Power Measurement Access for Evaluation
  - Power Management for Low-power Operation
  - General-purpose Device Drivers
  - Program Loader for Flash Code Download
- **Advanced Power Management**
  - On-chip Switching Buck Converter for Internal 1.8V
  - 5 mA @ 4 MHz, 17 mA @ 32MHz
  - Low-power Mode: 25 µA @ 16kHz
  - Power Supervisor with Power On Reset (POR)
  - Programmable Battery Monitoring
  - Programmable Brown-out
- **Other**
  - Single Power Supply; VH = +2.6 to +3.6 V
  - 64-lead LQFP Package
  - Temperature Range: -40 °C to +85 °C
  - Supports ARM7™ Industry-standard Tools
  - Supports Shunts & Current Transformers (CTs)
  - Customer Development Board (CDB) Available

**ORDERING INFORMATION:**
See page 40 for details.



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# 1. HARDWARE DESCRIPTION

The CS7401xx is part of a family of energy measurement system-on-a-chip (SoC) products that provides the ability to implement Metrology, Register, and Communication (MRC) functions all in the same device. Building on our high-quality line of Delta-Sigma (ΔΣ) analog-to-digital converters (ADCs), Cirrus Logic has added a very powerful but economical 32-bit processing sub-system, along with a targeted set of peripherals to provide a very powerful yet cost-effective energy measurement solution. The CS740111/CS740121/CS740131 are identical except for the amount of flash memory, which is 32 kB/64 kB/128 kB respectively.

Basic to all energy measurement applications is the ability to acquire the voltage and current data with a high degree of precision. The CS7401xx family of products is built around three independent, high-precision ADCs that concurrently acquire both voltage and current information at a data rate high enough to measure up to the 30$^{th}$ harmonic. A third channel is available for 3-wire measurement, neutral current measurement, and for anti-tampering applications. The sampled data is processed through a pipeline of computations which results in a 24-bit quantity available at 1, 2, 4, or 8 kHz.

The power behind this advanced system is a high-performance, 32-bit embedded ARM7™-based subsystem capable of executing the most demanding standards. The large logical address space allows ease of code development. The ARM7TDMI™ core features a hardware multiplier, 31 registers, a JTAG debug port, EmbeddedICE™ module, flexible interrupt mechanism, and an optional 16-bit Thumb® instruction set. The CPU can run from Flash, ROM, or RAM. The device includes on-chip debug circuitry that provides non-intrusive, full-speed, in-circuit debugging of the device installed in the end application.

The 32-bit processing subsystem includes the ROM, RAM, on-chip flash memory, and FIFO interface to the ADC. The 32 kB of ROM contains a profile for initial code download along with many APIs (see the Firmware/API Description for more details). Application code can be downloaded to the on-chip flash memory which provides a "Flash-lock" feature that ensures code will remain secure. The ROM and flash programs are supported by 8 kB of on-chip SRAM that is intended for temporary data storage, but can also be used to execute code. A special feature of the SoC is having a FIFO interface from the ADC to the processing subsystem, reducing the interrupt overhead in acquiring data.

The CS7401xx's integrated peripherals reduce the overall system cost. The 120-segment LCD interface eliminates the need for an external LCD controller. The synchronous serial port (SSP) allows the device to interface to many different high-speed peripherals including non-volatile memory, SRAM, etc. Two UART ports allow communication to RS485, Infrared (IR), or other subsystems. The internal real time clock (RTC) eliminates the need for an external RTC chip. Other features include several timer/counters, a dedicated HW Energy Pulse output, and GPIOs to interface with buttons, switches, and control signals. Flexible control allows multiple functionality for each GPIO pin, enabling custom configuration for different applications.

Power management is key in any system's design. The device integrates a switching buck converter that efficiently provides a 1.8V internal supply from the external power supply that is very well regulated. This provides a high level of immunity to power supply noise. The device has an option for a battery mode with a battery monitor and brown-out detection which allows the software the flexibility to control the power mode.

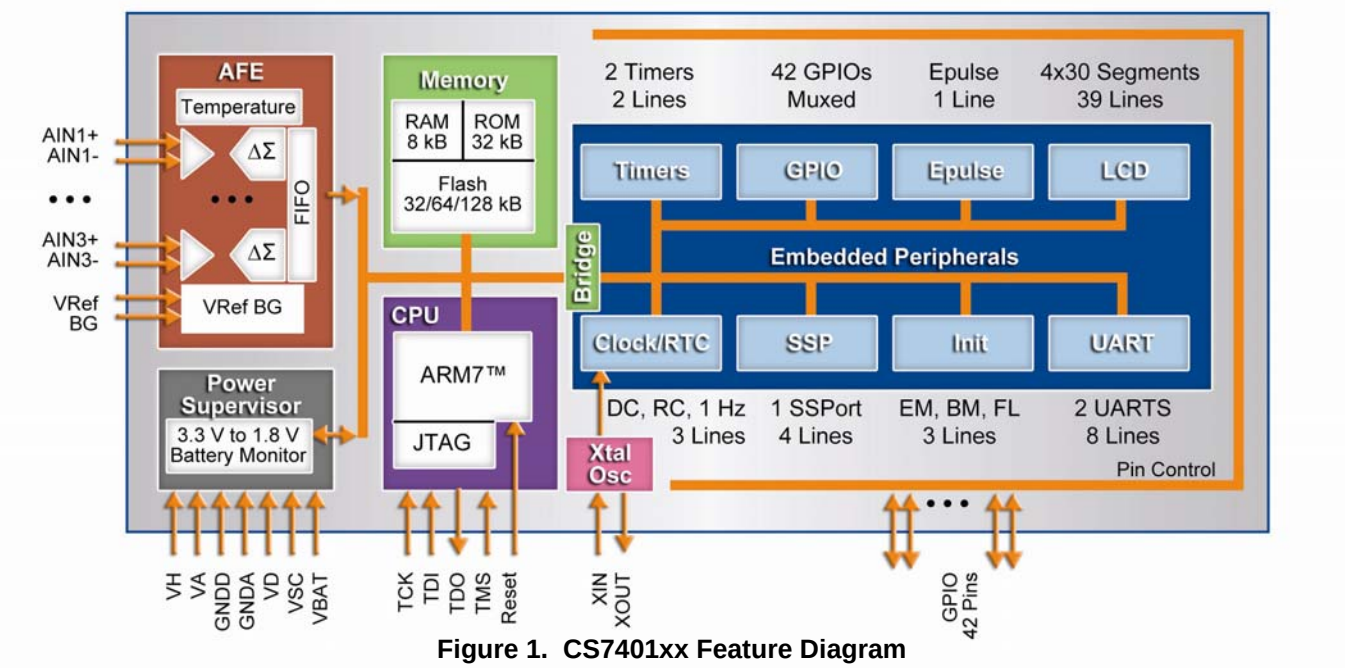



**Figure 1. CS7401xx Feature Diagram**

## 2. FIRMWARE/API DESCRIPTION

Development of user Metrology, Register, and Communications (MRC) code is accelerated with the availability of many high-level APIs in both ROM-based firmware and library function calls. The product is supported with application examples, many development notes, and library of functions which are available in the CS7401xx Software Development Kit (SDK). C-code-based development platforms for the ARM7™ can be provided by several vendors such as Keil.

One of the key firmware APIs is Cirrus Logic's wavelet-based algorithm for power calculation. This algorithm, coupled with the high-performance Delta-Sigma (ΔΣ) ADCs, produces data linearity accuracy of ±0.1% over 3000:1 dynamic range for active power measurement. In addition to active power, it also provides for measurement of reactive and apparent power for both total and fundamental power. A key feature of this algorithm is the accuracy of the fundamental reactive power measurement which measures the fundamental line frequency (45 Hz to 70 Hz), applies an extremely narrow-band filter to the voltage and current then calculates the phase angle — all with accuracy similar to that of the active power calculations. Being available in firmware, this algorithm allows for quick and accurate application development with proven metrology code.

While the Cirrus Logic power measurement algorithm is always available in ROM, it can be partially or totally customized with flash-based code. This "open" approach to metrology is one of the unique features that is enabled by having a single 32-bit RISC processing element.

In addition to the metrology, the processor has enough power to implement standards-based data management and secure communications protocols. Metrology typically requires much less than 4 MHz of processor bandwidth. The capabilities of the processing systems to dynamically change processor frequency allows the application to boost the processing power upon demand. For example, when a communication event occurs, the processor can change the system to 32 MHz operation, service the communication request, and go back to 4MHz operation, minimizing the average power consumption.

The APIs are layered into a component layer, device driver layer, and Hardware Abstraction Layer (HAL). The component layer provides support for saving/restoring system settings, rapid calibration, handling the ADCs, FIFO interface, filters, power calculations algorithms, and power management to detect brownout condition and manage low-power operation. The device driver layer contains a set of modules that implements the higher-level functionality needed for managing a hardware block including reading and writing the flash memory, the interrupt controller, UARTs, calibration/settings partition, energy partition, analog front end (AFE), core, RTC, timers, SSP, and LCD.

In addition to the APIs, the ROM code contains a full application profile allowing Evaluation, Development, and Manufacturing (EDM) capabilities over a UART port. This ROM EDM profile allows access to the firmware metrology algorithms and device calibration during initial evaluation and also supports code download to the flash during development and manufacturing. Early evaluation is available using the CDB7401xx-LV (customer demonstration board). This, coupled with a Windows®-based software tool (CapturePlus II), allows the user to calibrate and test the CS7401xx. Please refer to the CDB7401xx-LV data sheet for details on the CDB7410xx-LV and the CapturePlus II software.

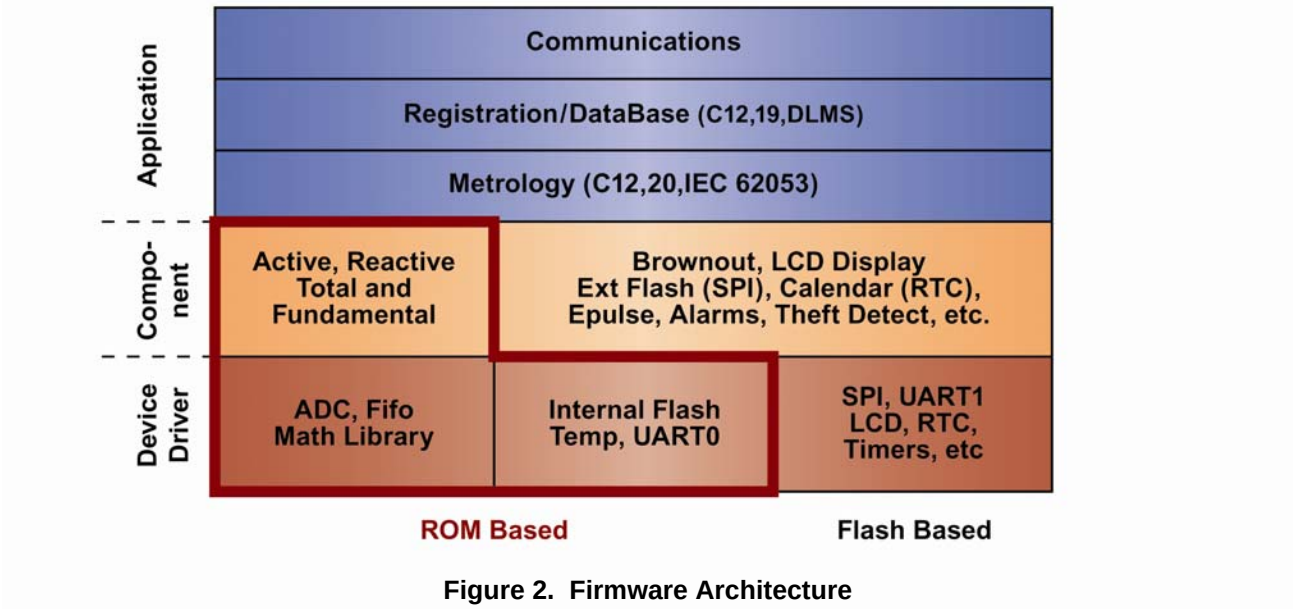



**Figure 2. Firmware Architecture**

## 3. PIN DESCRIPTION

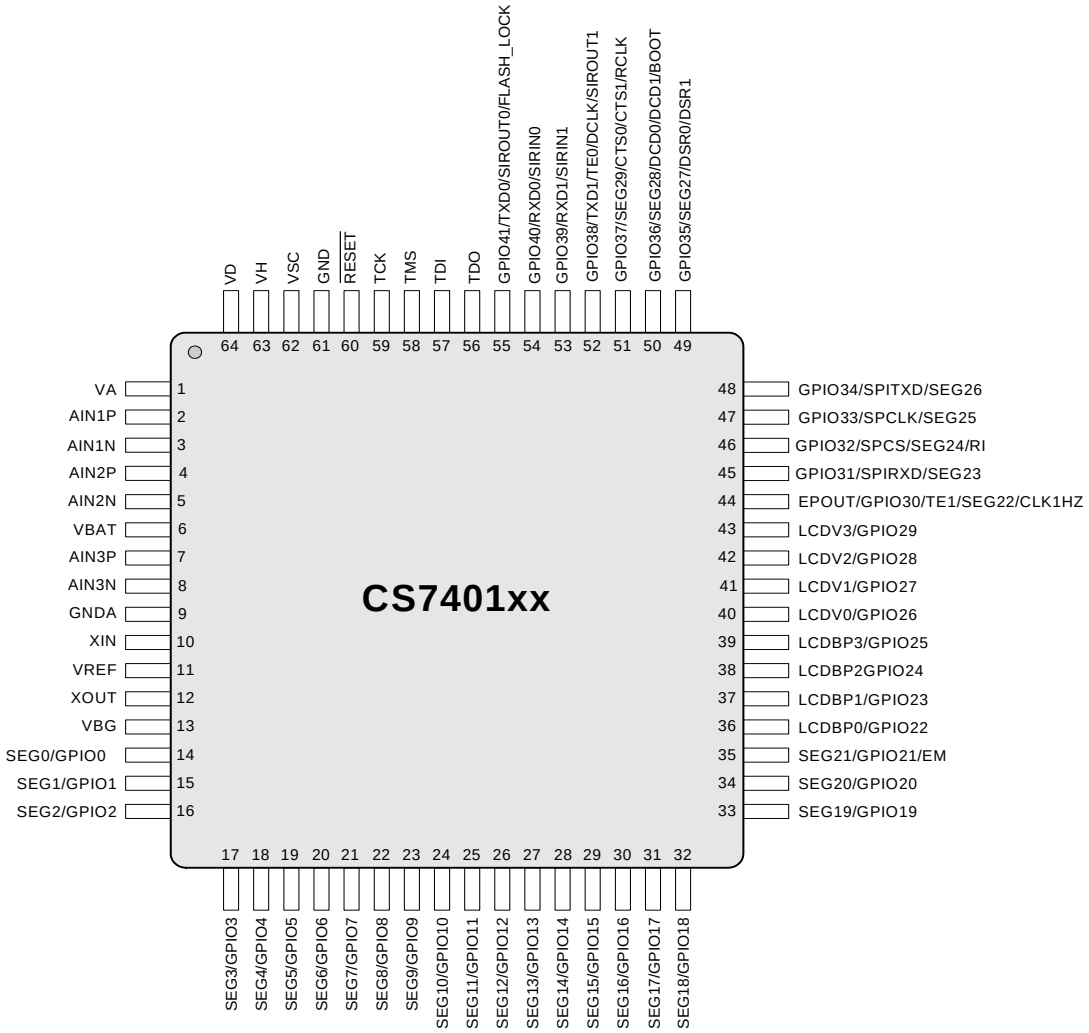



**Table 1. CS7401xx Pin Functions**

| Name | Pin # | I/O | Function |
|---|---|---|---|
| VA | 1 | | External Analog supply (1.8 V) |
| AIN1P | 2 | I | Differential analog input pin for analog channel 1 |
| AIN1N | 3 | I | Differential analog input pin for analog channel 1 |
| AIN2P | 4 | I | Differential analog input pin for analog channel 2 |
| AIN2N | 5 | I | Differential analog input pin for analog channel 2 |
| VBAT | 6 | I | Battery voltage monitor |
| AIN3P | 7 | I | Differential analog input pin (+) for analog channel 3 |
| AIN3N | 8 | I | Differential analog input pin (-) for analog channel 3 |
| GNDA | 9 | | Analog ground |
| XIN | 10 | I | Input of inverting amplifier for crystal oscillator. Connect to one side of 32.768k Hz crystal or to crystal oscillator source. When using an external 32.768 kHz clock, the input level requirements for the XIN pin are 0 to 1.8V. |

**Table 1. CS7401xx Pin Functions (Continued)**

| | | | |
|---|---|---|---|
| VREF | 11 | O | Internal reference voltage output (1.8V) |
| XOUT | 12 | O | Output of inverting amplifier for crystal oscillator. Connect to one side of 32 768k Hz crystal |
| VBG | 13 | O | Output of band-gap (1.2V) |
| SEG0/GPIO0 | 14 | I/O | LCD segment output 0 / General-purpose digital I/O 0 |
| SEG1/GPIO1 | 15 | I/O | LCD segment output 1 / General-purpose digital I/O 1 |
| SEG2/GPIO2 | 16 | I/O | LCD segment output 2 / General-purpose digital I/O 2 |
| SEG3/GPIO3 | 17 | I/O | LCD segment output 3 / General-purpose digital I/O 3 |
| SEG4/GPIO4 | 18 | I/O | LCD segment output 4 / General-purpose digital I/O 4 |
| SEG5/GPIO5 | 19 | I/O | LCD segment output 5 / General-purpose digital I/O 5 |
| SEG6/GPIO6 | 20 | I/O | LCD segment output 6 / General-purpose digital I/O 6 |
| SEG7/GPIO7 | 21 | I/O | LCD segment output 7 / General-purpose digital I/O 7 |
| SEG8/GPIO8 | 22 | I/O | LCD segment output 8 / General-purpose digital I/O 8 |
| SEG9/GPIO9 | 23 | I/O | LCD segment output 9 / General-purpose digital I/O 9 |
| SEG10/GPIO10 | 24 | I/O | LCD segment output 10 / General-purpose digital I/O 10 |
| SEG11/GPIO11 | 25 | I/O | LCD segment output 11 / General-purpose digital I/O 11 |
| SEG12/GPIO12 | 26 | I/O | LCD segment output 12 / General-purpose digital I/O 12 |
| SEG13/GPIO13 | 27 | I/O | LCD segment output 13 / General-purpose digital I/O 13 |
| SEG14/GPIO14 | 28 | I/O | LCD segment output 14 / General-purpose digital I/O 14 |
| SEG15/GPIO15 | 29 | I/O | LCD segment output 15 / General-purpose digital I/O 15 |
| SEG16/GPIO16 | 30 | I/O | LCD segment output 16 / General-purpose digital I/O 16 |
| SEG17/GPIO17 | 31 | I/O | LCD segment output 17 / General-purpose digital I/O 17 |
| SEG18/GPIO18 | 32 | I/O | LCD segment output 18 / General-purpose digital I/O 18 |
| SEG19/GPIO19 | 33 | I/O | LCD segment output 19 / General-purpose digital I/O 19 |
| SEG20/GPIO20 | 34 | I/O | LCD segment output 20 / General-purpose digital I/O 20 |
| SEG21/GPIO21 | 35 | I/O | LCD segment output 21 / General-purpose digital I/O 21 / Energy Meter (EM) mode select |
| LCDBP0/GPIO22 | 36 | I/O | LCD backplane output 0 / General-purpose digital I/O 22 |
| LCDBP1/GPIO23 | 37 | I/O | LCD backplane output 1 / General-purpose digital I/O 23 |
| LCDBP2/GPIO24 | 38 | I/O | LCD backplane output 2 / General-purpose digital I/O 24 |
| LCDBP3/GPIO25 | 39 | I/O | LCD backplane output 3 / General-purpose digital I/O 25 |
| LCDLV0/GPIO26 | 40 | I/O | Analog LCD voltage Level 0 (lowest) / General-purpose digital I/O 26 |
| LCDLV1/GPIO27 | 41 | I/O | Analog LCD voltage level 1/ General-purpose digital I/O 27 |
| LCDLV2/GPIO28 | 42 | I/O | Analog LCD voltage level 2/ General-purpose digital I/O 28 |
| LCDLV3/GPIO29 | 43 | I/O | Analog LCD voltage level 3 (highest)/ General-purpose digital I/O 29 |
| EPOUT/GPIO30/TE1/ SEG22 | 44 | I/O | Energy Pulse output/General-purpose digital I/O 30 / Timer Enable 1 / LCD segment output 22/RTC generated reference clock (CLK1HZ) / Sleep Recovery |
| GPIO31/SPIRXD/SEG23 | 45 | I/O | General-purpose digital I/O 31/ SPI Receive Data / LCD segment output 23 |
| GPIO32/SPICS/SEG24 | 46 | I/O | General-purpose digital I/O 32/ SPI Chip Select / LCD segment output 24/RI |
| GPIO33/SPICLK/SEG25 | 47 | I/O | General-purpose digital I/O 33 / SPI Clock / LCD segment output 25 |
| GPIO34/SPITXD/SEG26 | 48 | I/O | General-purpose digital I/O 34 / SPI Transmit Data LCD segment output 26 |

**Table 1. CS7401xx Pin Functions (Continued)**

| | | | |
|---|---|---|---|
| GPIO35/SEG27/DSR0/ DSR1 | 49 | I/O | General-purpose digital I/O 35 / LCD segment output 27 / DSR 0 / DSR 1 |
| GPIO36/SEG28/DCD0/ DCD1/BOOT | 50 | I/O | General-purpose digital I/O 36 / LCD segment output 28 / DCD 0 / DCD 1 / Boot mode select (from FLASH or ROM). Should be pulled high for energy meter applications. |
| GPIO37/SEG29/CTS0/ CTS1/RCLK | 51 | I/O | General-purpose digital I/O 37 / LCD segment output 29 / CTS 0 / CTS 1/RCLK (XTAL Calibration clock) |
| GPIO38/TXD1/TE0/ DCLK/SIROUT1 | 52 | I/O | General-purpose digital I/O 38 / TXD 1 /Timer Enable 0 / DCLK Output / SIROUT1 |
| GPIO39/RXD1/SIRIN1 | 53 | I/O | General-purpose digital I/O 39 / RXD 1 / SIRIN1 |
| GPIO40/RXD0/SIRIN0 | 54 | I/O | General-purpose digital I/O 40 / RXD 0 / SIRIN0 |
| GPIO41/TXD0/SIROUT0 | 55 | I/O | General-purpose digital I/O 41 / TXD 0 / SIROUT0/ FLASH_LOCK |
| TD0 | 56 | O | Test data output of Test/Debug (JTAG) Port |
| TDI | 57 | I | Test data input of Test/Debug (JTAG) Port |
| TMS | 58 | I | Test mode signal input of Test/Debug (JTAG) Port |
| TCK | 59 | I | Test clock input of Test/Debug (JTAG) Port |
| $\overline{\text{RESET}}$ | 60 | I | Active-low reset |
| GND | 61 | | Ground |
| VSC | 62 | | Internal Voltage regulator output. |
| VH | 63 | | External 3.3 V supply |
| VD | 64 | | External Digital supply (1.8 V) |

See Section *5.4.6 GPIOs* on page 34 for details on special functionality of some GPIO pins.

## 3.1 GPIO Pin Multiplexing

The GPIO pins can be multiplexed with various other functions such as SSP port, serial ports, timer input, energy pulse output, clock I/Os, and various pull-ups and pull-downs that control initialization. The following provide a reference for the pin multiplexing options.

**Table 2. GPIO Pin Multiplexing**

| Pin # | LCD Function | GPIO Pins | SSP Port | Serial Port | Timers | EPulse | Clock | Init. PU/PD |
|---|---|---|---|---|---|---|---|---|
| 14-34 | LCD Seg 0-20 | GP I/O 0-20 | | | | | | |
| 35 | LCD Seg 21 | GP I/O 21 | | | | | | Pull Up (Energy Meter) |
| 36-39 | LCD BP 0-3 | GP I/O 22-25 | | | | | | |
| 40-43 | LCD voltage 0-3 | GP I/O 26-29 | | | | | | |
| 44 | LCD Seg 22 | GP I/O 30 | | | T4 Enable | Epulse | 1Hz Out | |
| 45 | LCD Seg 23 | GP I/O 31 | SPI Receive | | | | | |
| 46 | LCD Seg 24 | GP I/O 32 | SPI CS | | | | | |
| 47 | LCD Seg 25 | GP I/O 33 | SPI Clock | | | | | |
| 48 | LCD Seg 26 | GP I/O 34 | SPI Transmit | RTS 0 | | | | |
| 49 | LCD Seg 27 | GP I/O 35 | | DSR 0 | | | | |
| 50 | LCD Seg 28 | GP I/O 36 | | DCD 0 | | | | Pull Up (Boot Mode) |
| 51 | LCD Seg 29 | GP I/O 37 | | CTS 0 | | | RCLK In | |
| 52 | | GP I/O 38 | | TXD1 | T3 Enable | | DCLK Out | Pull Down (Test) |
| 53 | | GP I/O 39 | | RXD1 | | | | |
| 54 | | GP I/O 40 | | RXD0 | | | | |
| 55 | | GP I/O 41 | | TXD0 | | | | Pull Down (Flash Lock) |

# 4. CHARACTERISTICS & SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Positive Supply Voltage (Note 1)<br>Active Mode<br>Power Saving Modes | VH | <br>2.6<br>2.4 | <br>3.3<br>2.7 | <br>3.6<br>3.6 | <br>V<br>V |
| Internal Supply Voltage | VSC | - | 1.8 | - | V |
| Digital Supply Voltage (Note 2) | VD | 1.7 | 1.8 | 1.9 | V |
| Analog Supply Voltage (Note 2) | VA | 1.7 | 1.8 | 1.9 | V |
| Internal Voltage Reference | VREF | - | 1.8 | - | V |
| Internal or External Bandgap Reference | VBG | - | 1.27 | - | V |
| System Clock | DCLK | 1.953 | 4096 | 32768 | kHz |
| Real Time Clock Crystal Frequency | RTCLK | - | 32.768 | - | kHz |
| Operating Temperature Range | $T_A$ | -40 | - | +85 | °C |

Notes: 1. See diagram below for typical power supply connection. See section 5.1.5 for the definition of power modes.
2. Supplied by VSC.

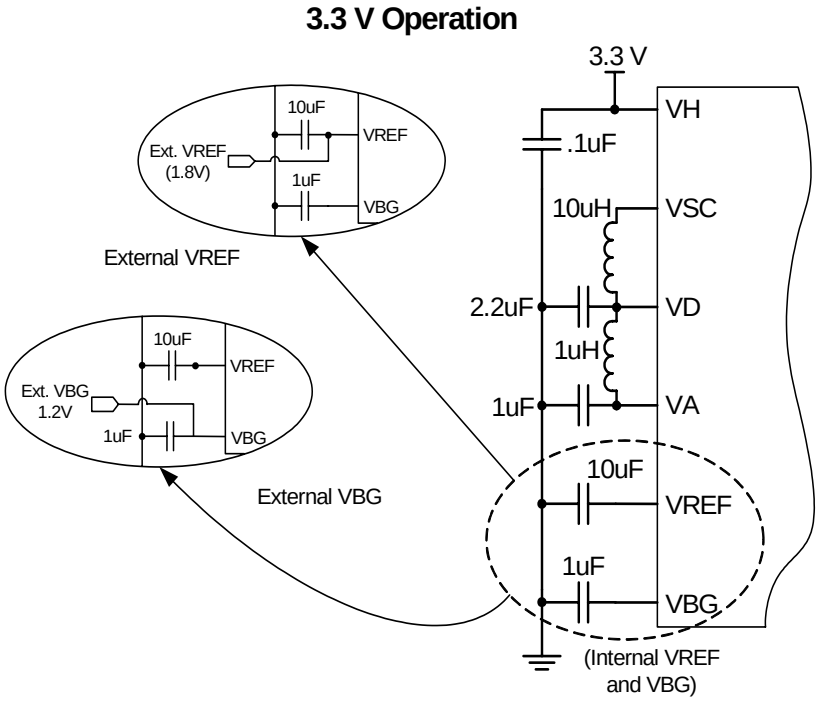



**Figure 3. DC Supply and Reference Connections**

## ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VH = 3.3 V ±5%; GNDA = GND = 0 V; VREF = +1.8 V. All voltages with respect to 0 V.
- MCLK (modulator clock) = 256 kHz; DCLK (CPU Clock) = 4.096MHz.
- Accuracy measurements are based upon using ROM-based metrology code provided by Cirrus Logic.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Accuracy*** | | | | | | |
| Active Power Accuracy | (Note 3) | P | | | | |
| | Input Range 0.03% - 100% | | - | ±0.1 | - | % |
| Reactive Power Accuracy | (Note 3) | Q | | | | |
| | Input Range 0.2% - 100% | | - | ±0.1 | - | % |
| | Input Range 0.1% - 0.2% | | - | ±0.5 | - | |
| Voltage & Current RMS Accuracy | (Note 3) | RMS | | | | |
| | Input Range 0.2% - 100% | | - | ±0.1 | - | % |
| | Input Range 0.1% - 0.2% | | - | ±0.5 | - | |
| Apparent Power Accuracy | (Note 3) | S | | | | |
| | Input Range 0.2% - 100% | | - | ±0.1 | - | % |
| | Input Range 0.1% - 0.2% | | - | ±0.5 | - | |
| Power Factor Accuracy | (Note 3) | PF | | | | |
| | Input Range 0.2% - 100% | | - | ±0.1 | - | % |
| | Input Range 0.1% - 0.2% | | - | ±0.5 | - | |
| ***Analog Inputs*** | | | | | | |
| Differential Input Range | 1.34x | IIN | - | - | ±400 | mV |
| | 3x | | - | - | ±200 | |
| | 6x | | - | - | ±100 | |
| | 12x | | - | - | ±50 | |
| Single Ended Input Range | 1.34X | IIN | - | - | ±200 | mV |
| | 3X | | - | - | ±100 | |
| | 6X | | - | - | ±50 | |
| | 12X | | - | - | ±25 | |
| Input Capacitance | | IC | - | 35 | - | pF |
| Effective Input Impedance | | EII | 400 | - | - | kΩ |
| Channel to Channel Crosstalk (50, 60 Hz) | (Note 4) | | - | -120 | - | dB |
| Common Mode Rejection | (50, 60 Hz) | CMRR | - | -60 | - | dB |
| Gain Error | | GE | - | 0.3 | - | % |
| Gain Drift | | GD | - | 20 | - | ppm/°C |

Notes: 3. Applies when the HPF option is enabled, input frequency 50 Hz ±5% and fundamental+harmonics measurement.
4. Full-scale input to the “driven” channel and “measured” channel input grounded.

## ANALOG CHARACTERISTICS (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Temperature Channel*** | | | | | |
| Temperature Accuracy (Note 5) | T | - | ±5 | - | °C |
| ***Power Supplies*** | | | | | |
| **Supply Current, Active Mode** VH = 3.3 V(Note 6, Note 7, Note 8) | | | | | |
| MCLK = 256 kHz, DCLK = 4.096 MHz | PC | - | 5 | - | mA |
| MCLK = 512 kHz, DCLK = 4.096 MHz | | - | 6 | - | |
| MCLK = 256 kHz, DCLK = 32.768 MHz | | - | 16 | - | |
| MCLK = 512 kHz, DCLK = 32.768 MHz | | - | 17 | - | |
| **Supply Current, Standby Mode** VH = 2.7 V(Note 6, Note 7, Note 8) | | | | | |
| Internal OSC =OFF, DCLK = 2.048 kHz | PC | - | 24 | - | µA |
| Internal OSC = OFF, DCLK = 32 kHz | | - | 27 | - | |
| **Supply Current, Sleep Mode** VH = 2.7 V(Note 6, Note 7, Note 8) | | | | | |
| Internal OSC = OFF, DCLK = Off, Crystal OSC = ON | PC | - | 23 | - | µA |
| **Supply Current, OFF Mode** VH = 2.7 V(Note 7, Note 7, Note 8) | | | | | |
| Internal OSC = OFF, Crystal OSC = OFF | PC | - | 16 | - | µA |
| | | | | | |
| **Power Supply Rejection Ratio** (50 Hz, 60 Hz) (Note 9) | PSRR | - | -85 | - | dB |

Notes:
5. After temperature sensor calibration.
6. MCLK is sourced by the on-chip oscillator, DCLK is the CPU clock
7. See section 5.1.5 for a description of “Active”, “Standby”, “Sleep”, and “OFF” modes.
8. All outputs unloaded. All inputs CMOS level. All gains = 1.34x.
9. Definition for PSRR: VH = 3.3 V, a 150 mV (peak-to-peak) (60 Hz) sinewave is imposed onto the +3.3 V DC supply voltage at VH pins. The “+” and “-” input pins of both input channels are shorted to AGND. Then the CS7401xx is commanded to continuous conversion acquisition mode, and digital sampled data is collected for the channel under test. The zero-to-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-to-peak value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel’s inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

## VOLTAGE REFERENCE

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Internal Reference*** | | | | | |
| Voltage | VREF | +1.7 | +1.8 | +1.9 | V |
| VREF Temperature Coefficient (Note 10)<br>Uncalibrated<br>Factory Calibrated | $TC_{VREF}$ | <br>-<br>- | <br>±60<br>±20 | <br>-<br>- | <br>ppm/°C<br>ppm/°C |
| ***External Reference Input*** | | | | | |
| Input Voltage Range | VREF | - | +1.8 | - | V |
| Input Capacitance | | - | 4 | - | pF |
| Input CVF Current | | - | 33 | - | µA |
| ***External Bandgap Reference Input*** | | | | | |
| Input Voltage Range | VBG | - | +1.27 | - | V |
| Input Capacitance | | - | 4 | - | pF |
| Input Current | | - | - | 2 | µA |

Notes: 10. The voltage at VREF is measured across the temperature range. Device Flash has not been written. From these measurements the following formula is used to calculate the VREF Temperature Coefficient:

$$TC_{VREF} = \left(\frac{(VREF_{MAX} - VREF_{MIN})}{VREF_{AVG}}\right)\left(\frac{1}{T_{MAX} - T_{MIN}}\right)(1.0 \times 10^{6})$$

11. Specified at maximum recommended output of 1 µA, source or sink.

## DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VH = 3.3 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 256 kHz; DCLK = 4.096MHz.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Clock Characteristics*** | | | | | |
| XIN Frequency (watch crystal or external source), (Note 12) | XIN | - | 32.768 | - | kHz |
| XIN Frequency Tolerance @ $T_A$ = 25°C | | - | ±20 | - | ppm |
| Digital Clock Frequency (Note 13) | DCLK | 1.953 | 4096 | 32768 | kHz |
| Modulator Clock Frequency (Note 13) | MCLK | 256 | 256 | 512 | kHz |
| ***XIN Crystal Characteristics*** (Note 14) | | | | | |
| Frequency Temperature Coefficient | $f_{TC}$ | - | -0.034 | | ppm/°C |
| Motional Series Resistance @ $T_A$ = 25°C | $R_M$ | - | - | 70 | kΩ |
| Drive Level@ $T_A$ = 25°C | $D_L$ | - | - | 1 | µW |
| Shunt Capacitance | $C_0$ | - | 1 | - | pF |
| Load Capacitance | $C_L$ | - | 12.5 | - | pF |
| Quality Factor | Q | - | 53000 | - | |
| ***EM Characteristics (Using ROM-based energy monitor metrology code)*** | | | | | |
| Phase Compensation Range | | -9 | - | +9 | ° |
| Output Word Rate | OWR | 1 | - | 8 | kHz |
| High-pass Filter Corner Frequency -3 dB | | - | 0.5 | - | Hz |
| ***Input/Output Characteristics*** | | | | | |
| High-level Input Voltage (VH=3.3V) | $V_{IH}$ | VH - 0.5 | - | - | V |
| Low-level Input Voltage (VH = 3.3 V) | $V_{IL}$ | - | - | 0.5 | V |
| High-level Output Voltage (VH=3.3V) $I_{out}$ = +2 mA | $V_{OH}$ | VH - 1.0 | - | - | V |
| Low-level Output Voltage (VH=3.3V) $I_{out}$ = -2 mA | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current | $I_{in}$ | - | ±1 | ±10 | µA |
| 3-state Leakage Current | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Output Pin Capacitance | $C_{out}$ | - | 5 | - | pF |

Notes: 12. When using an external 32.768 kHz clock, the input level requirements for the XIN pin are 0 to 1.8V.
13. MCLK is sourced by the on-chip oscillator, DCLK is the CPU clock.
14. Citizen CM415 or equivalent crystal.

## SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA = 1.8 V ±.1 V, VD = 1.8 V ± 0.1 V; GNDA = GND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rise Times<br>(Note 15) | <br>Any Digital Output | $t_{rise}$ | -<br>- | -<br>50 | 1.0<br>- | µs<br>ns |
| Fall Times<br>(Note 15) | <br>Any Digital Output | $t_{fall}$ | -<br>- | -<br>50 | 1.0<br>- | µs<br>ns |
| ***Start-up*** | | | | | | |
| RTCLK Start-up Time | XTAL = 32.768 kHz (Note 16) | $t_{rtcos}$ | - | 0.3 | - | s |
| MCLK and DCLK Start-up Time | See Figure 6 | $t_{sysos}$ | - | 1 | - | s |
| ***Serial Port (SSP) Timing*** | | | | | | |
| Serial Clock Frequency | | SPICLK0 | - | - | 2 | MHz |
| Serial Clock Pulse Widths | Pulse Width High<br>Pulse Width Low | $t_1$<br>$t_2$ | 200<br>200 | -<br>- | -<br>- | ns<br>ns |
| ***SPIRXD Timing*** | | | | | | |
| $\overline{\text{SPICS0}}$ Falling to SPICLK0 Rising | | $t_3$ | 50 | - | - | ns |
| Data Set-up Time Prior to SPICLK0 Rising | | $t_4$ | 50 | - | - | ns |
| Data Hold Time After SPICLK0 Rising | | $t_5$ | 100 | - | - | ns |
| ***SPITXD Timing*** | | | | | | |
| $\overline{\text{SPICS0}}$ Falling to SPITXD Driving | | $t_6$ | - | 20 | 50 | ns |
| SPICLK0 Falling to New Data Bit (hold time) | | $t_7$ | - | 20 | 50 | ns |
| $\overline{\text{SPICS0}}$ Rising to SPITXD Hi-Z | | $t_8$ | - | 20 | 50 | ns |
| ***External E$^2$PROM Mode Timing*** | | | | | | |
| Serial Clock (SPICLK0) | Pulse Width Low<br>Pulse Width High | $t_9$<br>$t_{10}$ | -<br>- | 8<br>8 | -<br>- | ns |
| MODE setup time to $\overline{\text{RESET}}$ Rising | | $t_{11}$ | 50 | - | - | ns |
| $\overline{\text{RESET}}$ rising to $\overline{\text{CS}}$ falling | | $t_{12}$ | 48 | - | - | ns |
| $\overline{\text{SPICS0}}$ falling to SPICLK0 rising | | $t_{13}$ | 100 | 8 | - | ns |
| SPICLK0 falling to $\overline{\text{SPICS0}}$ rising | | $t_{14}$ | - | 16 | - | ns |
| $\overline{\text{SPICS0}}$ rising to driving MODE low | | $t_{15}$ | 50 | - | - | ns |
| SPITXD setup time to SPICLK0 rising | | $t_{16}$ | 100 | - | - | ns |

Notes: 15. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

16. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

## SWITCHING CHARACTERISTICS (Continued)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***EPOUT Timing*** (Note 17, 17and 19) | | | | | |
| Period | $t_{period}$ | 0.5 | - | $2^{30}$ - 1 | µs |
| Pulse Width | $t_{pw}$ | 0.25 | - | $2^{30}$ - 2 | µs |
| Rising Time | $t_{on}$ | - | 20 | - | ns |
| Falling Time | $t_{off}$ | - | 20 | - | ns |
| ***CLK1HZ Timing*** | | | | | |
| Period | $t_{period}$ | - | 1 | - | s |
| Pulse Width | $t_{pw}$ | - | 0.5 | - | ms |
| Rising Time | $t_{on}$ | - | 20 | - | ns |
| Falling Time | $t_{off}$ | - | 20 | - | ns |

Notes: 17. Pulse output timing is specified at DCLK = 4.096 MHz. Both period and pulse width are user programmable.
18. Output pin has the driving load of 30 pF.
19. Timing is proportional to the frequency of DCLK

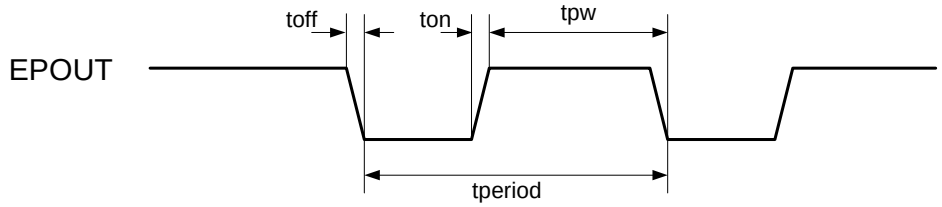



**Figure 4. EPOUT Timing**

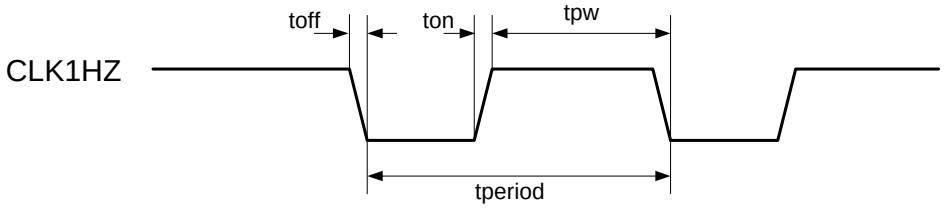



**Figure 5. CLK1HZ Timing**

## ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Power Supplies | (Notes 20 and 21) | VH | -0.3 | - | 3.63 | V |
| | Digital | VD | -0.3 | - | 1.98 | V |
| | Analog | VA | -0.3 | - | 1.98 | V |
| Input Current, Any Pin Except Supplies | (Notes 22, 23, 24) | $I_{IN}$ | - | - | ±10 | mA |
| Output Current | | $I_{OUT}$ | - | - | 100 | mA |
| Output Current Sourced or Sunk by Any I/O Pin | | | - | | 5 | mA |
| Analog Input Voltage | All Analog Pins | $V_{INA}$ | -0.3 | - | (VA) + 0.3 | V |
| Digital Input Voltage | All Digital Pins | $V_{IND}$ | -0.3 | - | (VD) + 0.3 | V |
| Ambient Operating Temperature | | $T_A$ | -40 | - | 85 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | - | 150 | °C |

Notes:
20. VA and GNDA must satisfy [(VA) - (AGND)] ≤ + 1.98 V.
21. VD and GNDA must satisfy [(VD) - (AGND)] ≤ + 1.98 V.
22. Applies to all pins including continuous over-voltage conditions at the analog input pins.
23. Transient current of up to 100 mA will not cause SCR latch-up.
24. Maximum DC input current for a power supply pin is ±50 mA.

## MEMORY

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***RAM*** | | | | | |
| Read/Write Time (No Wait State) | | 30 | - | - | ns |
| ***FLASH*** | | | | | |
| Program Time per Word | | 20 | - | 40 | µs |
| Read Time (No Wait State) | | 30 | - | - | ns |
| Page Erase (2 kB) | | 20 | - | 40 | ms |
| Mass Erase | | 20 | - | 40 | ms |
| Maximum number of Write Cycles | | - | 20 | - | k |

Notes: 25. Minimum supply voltage when the data in the RAM remain unchanged. No program execution should take place.

## POWER ON RESET (POR) AND BROWNOUT DETECTION TIMING

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VH=Vt1 to $\overline{\text{RESET}}$ pin high | $t_0$ | 2 | - | - | ms |
| VH=Vt1 to $\overline{\text{POR\_3.3V}}$ rising | $t_1$ | - | 50 | - | µs |
| $\overline{\text{POR\_3.3V}}$ rising to Bandgap_on rising | $t_2$ | - | 2 | - | ns |
| Bandgap_on rising to Bandgap_rdy rising | $t_3$ | - | 50 | - | µs |
| Bandgap_rdy rising to 65.536 MHz OSC_on rising | $t_4$ | - | 20 | - | ns |
| 65.536 MHz OSC_on rising to Regulator_on rising | $t_5$ | - | 1 | - | µs |
| Buck Regulator_on to $\overline{\text{ARM\_Reset}}$ rising | $t_6$ | - | 4 | - | µs |
| VH=vt2 to $\overline{\text{PSUP\_INT[1]}}$ high | $t_7$ | - | 60 | - | µs |

26. POR timing parameters and timing are shown in Figure 6 on page 18

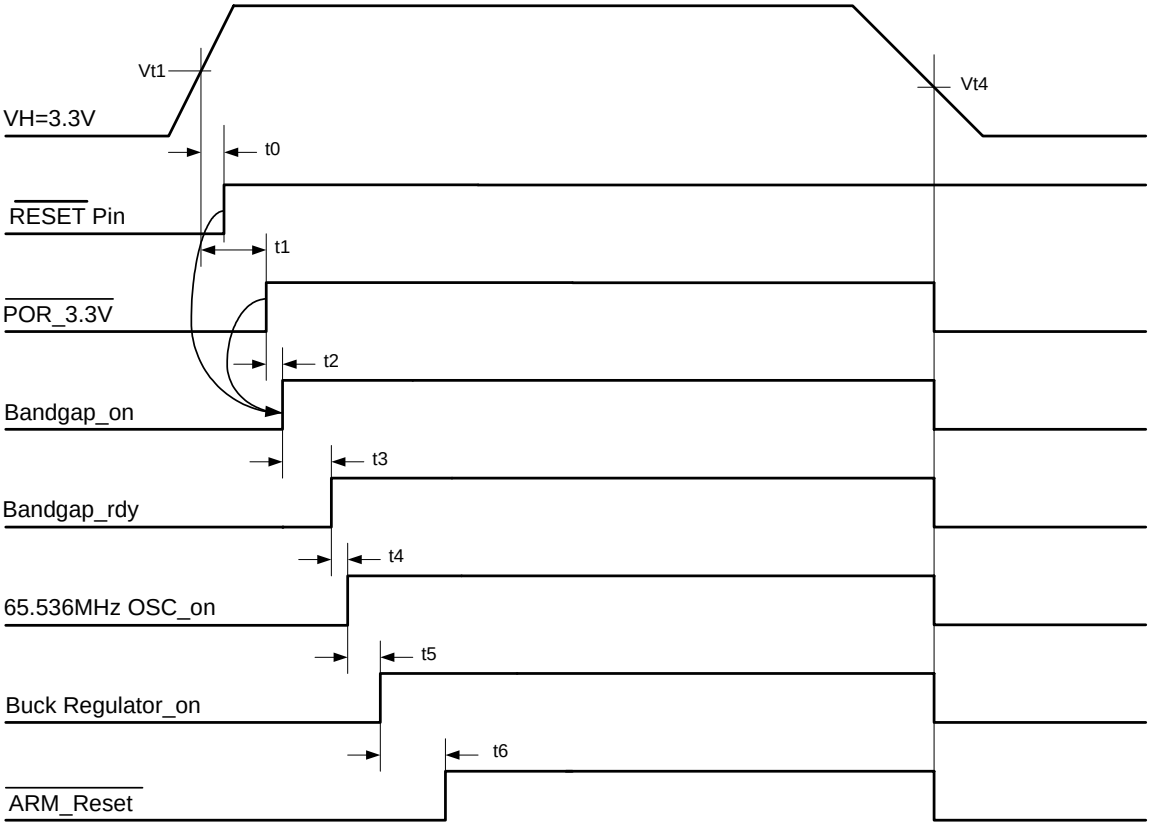



**Figure 6. POR and Reset Timing**

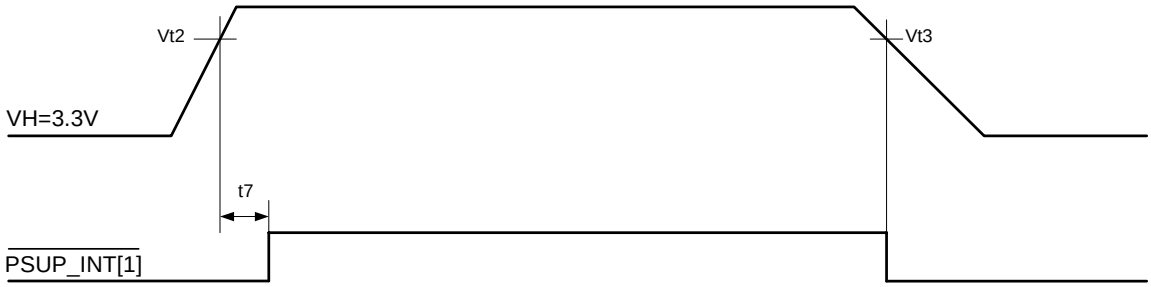



**Figure 7. Brownout Timing**

**Table 3. Typical Brownout and POR Threshold Voltages**

| Voltage Threshold | VH |
|---|---|
| Voltage Threshold $V_{t1}$ | 1.95 V |
| Voltage Threshold $V_{t2}$ | 2.66 V |
| Voltage Threshold $V_{t3}$ | 2.6 V |
| Voltage Threshold $V_{t4}$ | 1.7 V |

# 5. FUNCTIONAL DESCRIPTION

## 5.1 Analog Front End

The CS7401xx Analog Front End (AFE) incorporates three fully differential analog input channels. Inputs AINx± are designed for voltage and/or current channel inputs.

Each channel has a highly integrated, 24-bit ADC, designed using multi-bit delta-sigma techniques. The ADCs operate at an over-sample rate of programmable 32, 64, 128, or 256 times the system output word rate (OWR). The different clock rates maximize power savings while maintaining high performance. The multiple-ADC structure samples the voltage and current inputs simultaneously. The ADC operates in one of two clock rates: 256 kHz and 512 kHz. The output word rates supported can be from 1 kHz to 8 kHz. For power meter applications, the typical output word rate is 4 kHz. The AFE is tightly integrated within the SoC with configuration registers, status registers, and ADC data interface mapped into the CPU I/O memory.

### *5.1.1 Analog Channels*

To accommodate different sensing elements each channel incorporates a Programmable Gain Amplifier (PGA) with four programmable input gains. Table3 illustrates the ADC channels' four gain selections and corresponding maximum input-signal level. The maximum level of single-ended signal is half of that of fully differential signal.

**Table 4. Channel PGA Configuration**

| Input Connection Type | Maximum Input Range | RMS | Gain |
|---|---|---|---|
| Fully Differential | ±400 $mV_p$ | 282.8 $mV_{RMS}$ | 1.34x |
| | ±200 $mV_p$ | 141.4 $mV_{RMS}$ | 3x |
| | ±100 $mV_p$ | 70.7 $mV_{RMS}$ | 6x |
| | ±50 $mV_p$ | 35.4 $mV_{RMS}$ | 12x |
| Single Ended | ±200 mV | 141.4 $mV_{RMS}$ | 1.34x |
| | ±100 mV | 70.7 $mV_{RMS}$ | 3x |
| | ±50 mV | 35.4 $mV_{RMS}$ | 6x |
| | ±25mV | 17.7 $mV_{RMS}$ | 12x |

For example, the channel's PGA gain is set to 1.34x. If the input signal is fully differential and pure sinusoid, the maximum signal level will be 400 mVp or 282.8 mVrms which generates full-scale ADC data output. If the input signal is single-ended, the maximum signal level will be 200 mVp or 141.4 mVrms which generates half the full-scale ADC data output. To achieve the maximum input impedance, the ADCs should be configured as single-ended or differential mode according to the actual signal input connection.

Figure 9 shows a typical fully differential connection for the current channel with a current transformer (CT). In this diagram, Ri± (470 ohms) and Ci± (33nF) act as the simple RC anti-alias filter that has about 30 dB attenuation at the sampling rate MCLK = 256KHz.

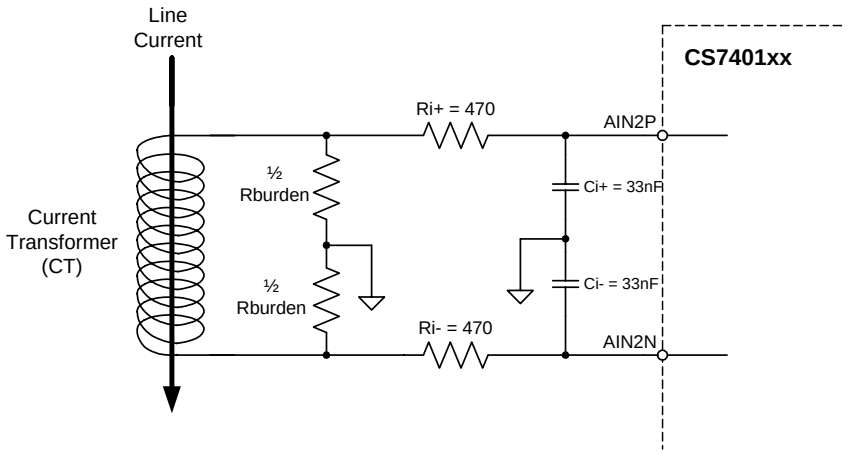



**Figure 8. Typical Fully Differential Connection for Current Channel**

### 5.1.2 ADC Measurements

The CS7401xx AFE incorporates three oversampling, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The high-fidelity 24-bit ADCs are identical. The ADCs operate with analog supply voltage VA of 1.8V and provide an output word rate of up to 8k samples per second. The AFE ADCs can be powered down individually to save power consumption.

A 3rd-order, feed-forward, multi-bit delta-sigma modulator is the core of the AFE A/D converters. The multi-bit modulator architecture facilitates ultra-low-power operation. The decimation ratio (DR) of the ADCs is 32/64/128/256 programmable. The ADCs perform instantaneous measurements at an output word rate (OWR) of

$$OWR = \frac{MCLK}{DR}$$

Therefore, with MCLK = 256KHz and DR = 64, the maximum OWR is 4k samples per second and the ADC frequency bandwidth is 2 kHz.

At each instantaneous measurement, the 24-bit sample is stored in the AFE FIFO. When the data in the FIFO reaches a user determined level, an interrupt is generated to the CPU. Handling this AFE interrupt is the main responsibility of the meter pre-process component in Energy Monitor firmware. The meter pre-process component offers a variety of filters and other services to manipulate the samples acquired by the AFE.

After the meter pre-process, the power utilities component in the Energy Monitor firmware provides functions to calculate both basic and advanced power parameters such as RMS voltage/current, active power, apparent power, reactive power, power factor, etc.

### 5.1.3 Voltage Reference

A high-precision, low-drift 1.8 V bandgap reference is provided on-chip. The internal reference also appears on the VREF pin. When using the internal reference, a 10 µF capacitor must be connected from the VREF pin to AGND to filter the output-stage noise and ensure stability during conversions. Also a 1µF capacitor must be connected from VBG pin to AGND to filter the bandgap noise. The reference can be used as a reference for other circuits in the system. However, an external buffer would be required because of the low drive capability of the VREF output. The VREF pin also provides a means of connecting an external reference.

### 5.1.4 Temperature Sensor

The CS7401xx contains an on-chip temperature sensor which is designed to assist in characterizing the measurement elements over a desired temperature range. Once a temperature characterization is performed, the temperature sensor can then be utilized to assist in compensating for temperature drift.

By setting the appropriate bits in temperature sensor configuration register (CONFIG_TS), the temperature sensor can be powered up and routed to an ADC channel (ADC channel 2 or 3). The ADC output can then be calculated to the real temperature value by the firmware. The calibration component in ROM also provides temperature calibrations. After the calibrations, the on-chip temperature sensor can reach to an accuracy of ±5 °C.

## 5.2 Power Supervisor and Power Modes

The CS7401xx power supervisor circuitry provides battery-mode detection, power on reset, and programmable brown-out detection and low-battery detection. The supervisory circuit guarantee the RESET assertion to protect the SoC during power up and power down. The battery-mode detection, brown-out detection and low-battery detection generate interrupts which can be used by software to initiate specific power down sequence to put the SoC into different power modes for power saving and proper operation.

Typically, power modes for the CS7401xx include “Active”, “Standby”, “Sleep”, and “Off”. Each mode is defined in Table 5.

.

**Table 5. Power Modes**

| Power Mode | Description |
|---|---|
| Active | All circuitry is operational. The Buck regulator is enabled. |
| Standby | The linear regulator is enabled. The internal oscillator, bandgap, ADCs and temperature sensor are powered down. The digital sections including the ARM7 are running using a slow clock from RTC oscillator. The speed of the digital clock is dependent upon the settings of the Clock Divider Control and Enable register. |
| Sleep | The linear regulator is enabled. All circuits are shut down or disabled except the RTC. This mode can only be exited by applying a low-to-high transition on GPIO30 (pin 44) or by a chip reset. |
| Off | RAM retention only. The linear regulator is enabled. All circuits are shut down or disabled including internal oscillator and RTC oscillator. This mode can only be exited by a chip reset. |

### *5.2.1 On-chip Voltage Regulators*

The CS7401xx has two voltage regulators internally to step down the single power supply (VH) to1.8V for the analog and the digital circuitry. Refer to figure 2 on page 8 for recommended power supply connections.

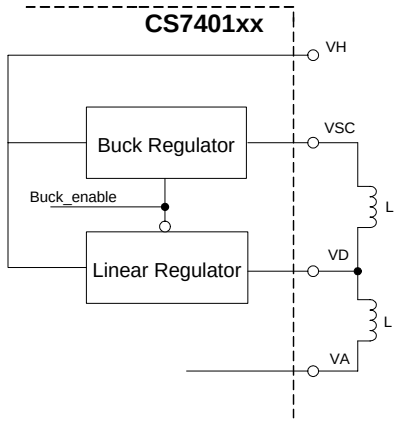



**Figure 9. On-chip Voltage Regulators**

The buck regulator can supply the maximum load current of 80mA and is used in active power mode. The operation of the buck regulator needs the internal 65.536 MHz oscillator and bandgap to be ready. The linear regulator can supply a load current up to 2 mA and be used in power saving modes. If the linear regulator is enabled, the Flash operation (read or write) must be avoided and software code should be running from either ROM or RAM. The internal Buck_enable signal controls which regulator is enabled.

### 5.2.2 Power On Reset and Brown-out Detection

Proper operation of the POR system requires that the external reset pin be connected to a RC with a time constant greater than 2 ms. This reset input pin is AND-ed with an internal signal indicating that the voltage is above 1.95 V to start the power-on sequence within the device. This signal will then enable the band gap, internal 65.536MHz oscillator, buck regulator, and finally release the reset to the ARM processor. This comparator has hysteresis such that when the voltage drops back below 1.7 V, the part will be held in reset. Refer to *Power On Reset (POR) and Brownout Detection Timing* on page 17 and Figure 6 on page 18 for detail on timing.

There are two conditions that can generate an interrupt to the ARM processor as an indication of a potential brown-out condition. The first is a comparator between VH and the battery. If VH falls below the battery voltage, the internal PSUP_INT[0] interrupt will trigger, if enabled. The second is a comparator between VH and an internal, programmable comparator. This comparator can be programmed from 2.75 V to 3.05 V in 0.1 V steps. If VH falls below the programmed threshold, the internal PSUP_INT[1] interrupt will trigger, if enabled.

At the point the interrupts occur, it is the responsibility of the software to manage the power state. See the power manager software development note for more details on the software operation during this condition.

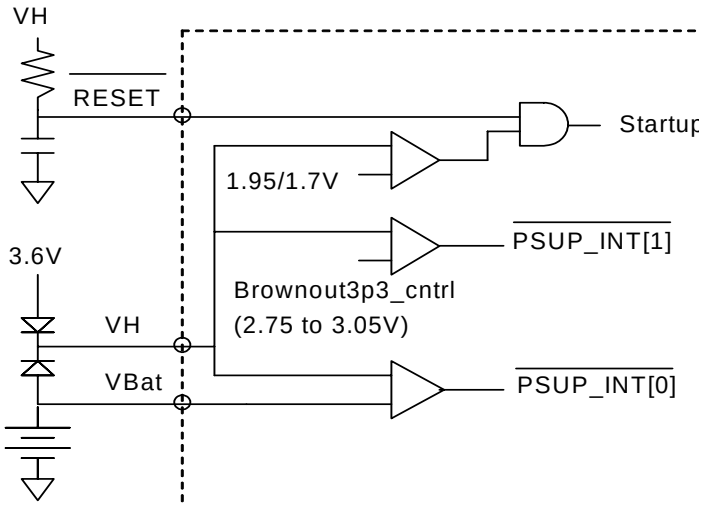



**Figure 10. POR and Brownout Functional Diagram**

### 5.2.3 Low-battery Detection

The CS7401xx contains a voltage comparator for low-battery detection. When the comparator is enabled and the battery voltage is lower than the pre-programmed threshold, the Vbat_low bit in the power supervisory register will be set. Because battery voltage may differ considerably with or without a load, an internal 8 Kohms resistive load can be enabled on VBAT pin to implement more practical low-battery detection.

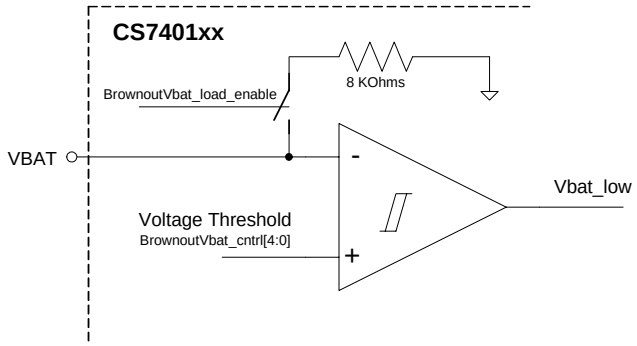



**Figure 11. Low Battery Detection**

## 5.3 Central Processor Unit (CPU)

The CPU offers a high-performance processor utilizing the high-speed 16/32-bit ARM7TDMI™ core, resulting in a high instruction throughput while maintaining high code efficiency. The processor core views ROM, SRAM, Flash, and memory-mapped registers (MMRs) as a single, linear array. ICE debugging is supported via the JTAG interface.

### *5.3.1 ARM7TDMI™ CORE*

The ARM7TDM™ core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8, 16, or 32 bits and the length of the instruction word is 32 bits. The ARM7TDMI™ is an ARM7™ core with 4 additional features:

- **T**humb® 16-bit compressed instruction set
- JTAG **D**ebug support on-chip, enabling the processor to halt in response to a debug request
- **M**ultiplier enhanced with higher performance, yielding a full 64-bit result
- Embedded**I**CE™ included within the core hardware to support embedded system debugging.

#### *5.3.1.1 Thumb® Mode*

An ARM® instruction is 32-bits long. The ARM7TDMI™ processor supports a second instruction set that has been compressed into 16-bits, the Thumb® instruction set. Greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications. However, the Thumb mode has two limitations:

- Thumb code usually uses more instructions for the same job, so ARM code is usually best for maximizing the performance of any time-critical code.
- The Thumb instruction set does not include some instructions that are needed for exception handling, so the core will automatically switch to ARM code for exception handling.

Since the CS7401xx program memory (Flash) is on-chip, up to 30% code density can be achieved by utilizing Thumb instructions. Thumb and ARM instructions both reside in 32-bit Flash memory. Therefore, one fetch will retrieve two Thumb instructions from the 32-bit memory.

#### *5.3.1.2 Long Multiply*

The Energy Monitor (EM) requires efficient digital signal processing (DSP) routines to calculate power/energy measurements. The ARM7TDMI instruction set includes four extra instructions which perform 32-bit by 32-bit multiplication with 64-bit product, and 32-bit by 32-bit multiplication-accumulation (MAC) with 64-bit result. These calculations are achieved in a reduced number of cycles compared to a standard ARM7 core.

#### *5.3.1.3 EmbeddedICE™ Module*

The EmbeddedICE™ module provides integrated on-chip support for the core. The EmbeddedICE module contains the break-point and watchpoint registers which allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port. When a breakpoint or watchpoint is encountered, the processor halts and enters the debug state. Once in the debug state, the processor registers may be inspected as well as the embedded Flash, SRAM, and MMRs.

#### *5.3.1.4 Exceptions*

ARM supports five types of exceptions, and a privileged processing mode for each type. The five type of exceptions are:

- normal interrupt or IRQ provided to service general-purpose interrupt handling of internal and external events
- fast interrupt or FIQ provided to service data transfer or communication with low latency. FIQ has priority over IRQ.
- memory abort
- attempted execution of an undefined instruction
- software interrupt (SWI) instruction which can be used to make a call to an operating system

Typically the programmer will define interrupts as IRQ, but for a higher-priority interrupt, the programmer can define the interrupt as FIQ for faster response time.

#### 5.3.1.5 ARM Registers

The ARM7TDMI™ processor has a total of 37 registers, of which 31 are general-purpose registers and six are status registers. Each operating mode has dedicated, banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (r0 to r14), the program counter (r15), and the current program status register (CPSR) are usable. The remaining registers are used only for system-level programming and for exception handling.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (r13) and the link register (r14), as represented in Figure 12. The fast interrupt mode has more registers (8 to 12) for fast interrupt processing, so that the interrupt processing can begin without the need to save or restore these registers and thus save critical time in the interrupt handling process.

### 5.3.2 Memory System

The CS7401xx SoC is constructed so that the complete memory system is on-chip. On-chip memory can support zero-wait-state access speeds and provides better power efficiency and reduced electromagnetic interference. The CS7401xx on-chip SRAM is preferred to cache memory for a number of reasons: it is simpler, cheaper, uses less power, and has a more deterministic behavior. The memory controller and Flash interface enable the ARM7 to access RAM, Flash, and ROM via the AHB (Advanced High-speed Bus).

The CPU is configured with the types of memory shown in Table 6: Memory Types and Sizes.

| Memory Type | Size | Address |
|---|---|---|
| ROM | 32 kB | 0x0800_0000 |
| SRAM | 8 kB | 0x0400_0000 |
| FLASH | 32 kB, 64 kB, or 128 kB | 0x0000_0000 |

**Table 6. Memory Types and Sizes**

Bank size and cycle times are fixed for the ROM and SRAM, but can be configured for Flash. The memory types are described later.

#### 5.3.2.1 Memory Remap

The CS7401xx is a small embedded implementation with memory constraints. However, a hardware solution is provided which allows a portion of ROM that overlays Flash to be remapped. As on all ARM-based processors, the boot strap loader (BSL) image starts execution at address 0x0000_0000. The first instruction executed loads the program counter with the reset vector address stored at an initial offset (of usually 0x0000_0020). Execution then continues at the reset vector address. The memory map has two states:

- *Normal*, selected when BOOT pin (pin 50) is low at reset.
- Remapped, selected when the BOOT pin (pin 50) is high at reset.

For energy meter applications, pin 50 (BOOT) should be pulled high.

#### 5.3.2.2 I/O peripherals overview

The CPU utilizes a standard memory-mapped I/O approach to perform I/O functions. The base address of all I/O memory mapped registers (MMRs) is factory defined, starting at address 0x1800_0000. The SoC architecture supports embedded peripherals in two areas:

- Advanced Peripheral Bus (APB)
- Advanced High-speed Bus (AHB)

The AHB peripherals implement a Clock Generator and System Controller which are connected to the AMBA AHB. Other embedded peripherals such as interrupt controller, timers/counters, LCD driver, RTC, UART, SSP and GPIOs are connected to the APB.

### 5.3.2.3 Memory Map

The CS7401xx has its memory arranged as a linear set of logical addresses. The ARM7 core sees memory as a linear array of $2^{32}$ byte locations. The different blocks of memory are mapped as outlined in Figure 12. The memory organization is configured in *little endian* format – the least-significant byte is located in the lowest byte address and the most-significant byte in the highest-byte address. Register addresses are all word-aligned. The exception vectors are all mapped at the bottom of the memory array from address 0x0000_0000 to 0x0000_0020.

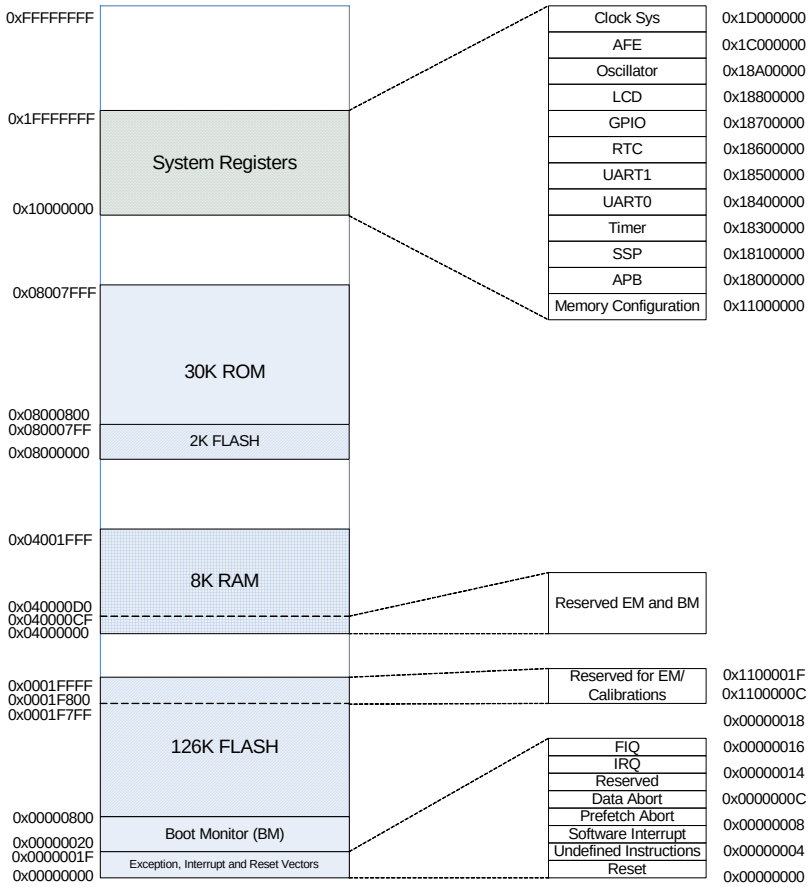



**Figure 12. CS7401xx Memory Map**

C language programs expect to have access to a fixed area of program memory (where the application image resides) and to support two data areas that grow dynamically and where the compiler often cannot work out an optimum size. These dynamic areas are:

- The stack. Whenever a (non-trivial) function is called, a new activation frame is created. When a function returns, its stack space is automatically recovered and will be reused for the next function call.
- The heap. The heap is an area of memory used to satisfy program request for more memory for new data structures. A program which continues to request memory over a long period of time should be careful to free up all sections that are no longer needed, otherwise the heap will grow until memory is full.

Due to the limitations of the SRAM in a small embedded system such as the CS7401xx, minimal stand-alone run-time libraries should be ported to the target environment, which allows basic C programs to run. This library therefore reflects the minimal requirements of a C program.

### 5.3.2.4 ROM

ROM provides single-cycle, read-only memory and is factory programmed with a Boot Monitor and the Energy Monitor firmware image. At power up and with the BOOT pin high, the SoC is in remapped state (See Figure 12), ROM aliases Flash at 0x0000_0000 and Boot Monitor initiates the SoC boot sequence. See *5.3.4 Boot Monitor* on page 28 for detailed boot sequence.

#### 5.3.2.5 SRAM

Synchronous SRAM is used to provide single-cycle, read-write memory. The SRAM region is organized as 2k x 32-bits and is chosen to represent temporary data memory. SRAM is used for temporary power calculation storage and for the dynamic stack/heap areas. The memory controller provides the interface between SRAM and the AHB (Advanced High-speed Bus). The SRAM is located at address 0x0400_0000. SRAM locations from 0x0400_0000 to 0x0400_00CF are reserved for Boot Monitor and Energy Monitor firmware. Free SRAM for custom applications starts from 0x0400_00D0.

#### 5.3.2.6 FLASH and FLASH Interface

The Flash memory is organized into pages of 2 kB. The total Flash size is up to 128 kB and is connected to the ARM7 core via the Memory Controller and Flash Interface and the AHB. Address, data along with clock and control signals are passed to the Flash from the AHB. Programming and erase function are configured and controlled via the internal Memory Controller and Flash Interface registers. The Flash locations from 0x0001F800 to 0x0001FFF are reserved for calibration functions of Energy Monitor. All other locations can be used to store user's application code and data.

To protect the customer's application code, the Flash memory can be locked either by hardware (pin55 - Flash Lock) or by software. Once the flash is locked, the Flash memory can not be read through JTAG. Only a mass erase can clear the Flash lock state.

Refer to the MEMORY table on page 17 for the timing specifications for the Flash memory.

### 5.3.3 Interrupt Controller

The interrupt controller provides a simple software interface to the interrupt system. The interrupt controller is compliant with the ARM Reference Peripheral Specification (RPS). The mapping of the interrupt controller registers conforms to the RPS with a base address of 0x1890_0000. In the CS7401xx system, two levels of interrupts are available:

- FIQ (Fast Interrupt Request) for fast, low-latency interrupt handling
- IRQ (Interrupt Request) for more-general interrupts

Separate interrupt controllers are used for FIQ and IRQ. The difference is that only a single bit position is defined for FIQ, which is intended for use by a single interrupt source, while 32 bits are available in the IRQ controller. A number of methods may be used to extend the IRQ interrupt controller if more than 32 interrupt sources are required.

The CPU utilizes a single-source FIQ, which is driven by the AFE circuit. This provides a true low-latency interrupt, because a single source ensures that the interrupt service routine may be executed directly without the need to determine the source of the interrupt. It also reduces the interrupt latency because the extra banked registers that are available for FIQ interrupts may be used to maximum efficiency by preventing the need for a context save.

The IRQ interrupt controller uses a bit position for each interrupt source. Bit positions are defined for software-programmed interrupts, communication channels, timers/counters, real time clock, and analog front end. Bit 0 is unassigned in the IRQ controller so that it may share the same interrupt source as the FIQ controller. All IRQ interrupt source inputs are active high and level sensitive. A programmed interrupt register is provided to generate an interrupt under software control.

#### 5.3.3.1 Interrupt Latency

The worst-case latency for an FIQ consists of the longest time the request can take to pass through the synchronizer, plus the time for the longest instruction to complete (the longest instruction is an LDM) which loads all the registers including the program counter (PC), plus the time for the data abort entry, plus the time for FIQ entry. At the end of this time, the ARM7TDMI will be executing the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just over 1.5 µSec in a system using a continuous 32 MHz processor clock. The maximum IRQ latency calculation is similar, but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used, some compilers have an option to compile without using this command. Another option is to run that part of the code in Thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is five cycles, which consists of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

*Note: The ARM7TDMI will always be run in ARM (32-bit) mode when in privileged modes, i.e. when executing interrupt service routines.*

### 5.3.4 Boot Monitor

The **Boot Monitor** is part of the factory-embedded firmware in ROM. After the SoC comes out of reset with BOOT pin high, the Boot Monitor starts to run and guide the boot sequence as follows.

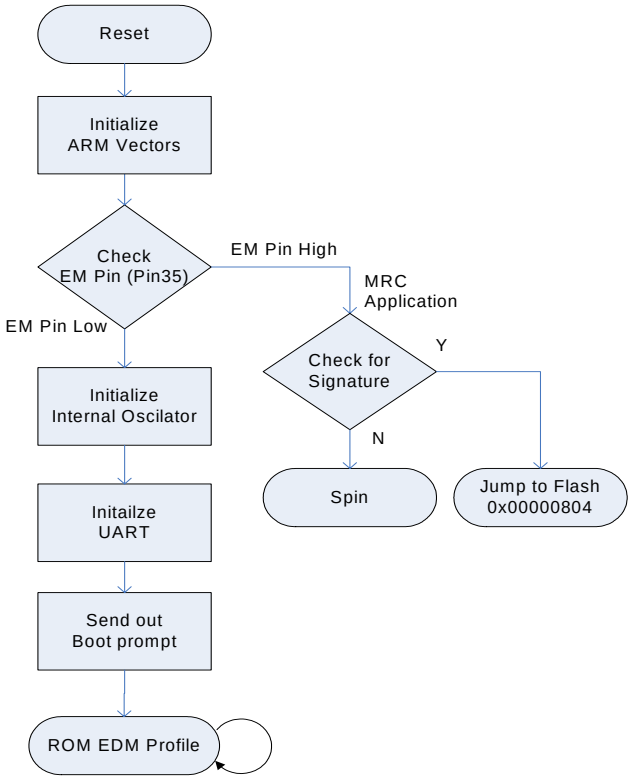



**Figure 13. CS7401xx Boot Sequence**

1) Initialize ARM Vectors - All exception vectors except for reset jump to RAM. This step initializes the exception vector table by initializing the code in RAM to the “b.” instruction.
2) Check EM Pin - Check Pin 35 which is EM pin (pin 35). The latched state of the EM pin is in bit 2 of the MEM_PROT register. If the pin is high, the process branches to the Flash-based MRC user application. If the pin is low, then branches to the embedded ROM EDM profile.
3) Check for Signature - This step checks if the custom application code loaded at Flash address 0x00000800 contains a valid data signature of “CRUS”. If the signature exists, then the process steps to the next address location (0x00000804) and executes the loaded application code. If the signature does not exist, then the process remains a loop.
4) Initialize Internal Oscillator - This step initializes the internal 65.536 MHz oscillator. This step must occur before using the UART. Failure to perform this step causes the CS7401xx UART baud rate to deviate more than 5% from acceptable levels. As a result, the CS7401xx will be unable to communicate with other devices through the UART.
5) Initial UART - Initialize the UART0 to 9600 baud, 8 bits, no parity, and no stop bit.
6) Send Out Prompt - Sends out a ‘>’ prompt so that a host computer can initiate ROM EDM profile commands through RS232 port.
7) ROM EDM Profile - This step branches to the main routine in ROM EDM Profile.

### 5.3.5 JTAG Debug Interface

The ARM7TDMI™ processor debug interface is based on IEEE std. 1149.1 - 1990, *Standard Test Access Port and Boundary-scan Architecture*. Refer to this standard for an explanation of the terms and for a description of the Test Access Port (TAP) controller states. The CPU contains hardware extensions for advanced debugging features. These make it easier to develop application software, monitors/BSL, and the hardware itself.

The EmbeddedICE™ module provides integrated, on-chip support for the core. A JTAG debug probe (e.g. Multi-ICE) and EmbeddedICE are a JTAG-based debugging system for the CS7401xx SoC providing the interface between a debugger and the ARM7 core embedded within the ASSP.

This system provides:

- real-time, address-dependent, and data-dependent breakpoints
- watchpoint registers
- single stepping
- full access to, and control of the ARM core
- full access to the SOC
- full memory access (read and write). Once the Flash is locked, access to Flash is prohibited.
- full I/O system access (read and write)
- enable the embedded microprocessor to access services of the host system

## 5.4 Embedded Peripherals

The CS7401xx SoC incorporates a collection of intelligent peripherals that are required in applications specific to energy metering. All embedded peripherals are fully compliant with the widely used SoC bus protocol, the Advanced Microcontroller Bus Architecture (AMBA®) protocol from ARM. The embedded peripherals utilize the AMBA Advanced Peripheral Bus (APB), which is optimized for minimal power consumption and reduced interface complexity to support peripheral functions. APB is used in conjunction with the standard AMBA AHB version of the on-chip system bus for high system performance.

### *5.4.1 Clock Generation & Real Time Clock (RTC)*

All clocks on the CS7401xx are generated from a single, low-cost 32.768 kHz crystal. To further reduce cost, the 22 pF capacitors typically needed for crystal operation, are integrated into the device. This oscillator circuit drives the fast clock generation, RTC subsystem and can drive the ARM process for ultra-low-power operation.

The real time clock (RTC) subsystem is driven from the 32 kHz oscillator. This clock is then divided down to a 1 Hz clock to operate a digital counter that can be used to generate time and date information. In many cases, the low-cost, 32.768 kHz crystal oscillator may not meet the accuracy requirements of the application. In this case, an external 16.77721 MHz clock can be used to calibrate the RTC to produce a highly accurate 1 Hz clock. Once calibrated, the RTC block will always generate an accurate clock with the crystal. Other than counting on the 1 Hz clock, the RTC can also generate an interrupt. The real time clock portion of the circuit operates whenever power is applied and the 32 kHz input clock is running.

On on-chip relaxation oscillator is used to generate a 65.536 MHz internal high-speed clock. This clock feeds both the analog front end (AFE) subsystem and the digital core. The AFE subsystem has its own clock divider needed to set the sampling rate of the ADC. The digital core is clocked by the output of a clock divider which can provide 4 MHz, 8 MHz, 16 MHz or 32 MHz operational speed. The default DCLK is 4.096 MHz.

During brownout conditions, the system clock can be switched to 32 kHz operation. This is a low-power standby mode where the RTC, RAM, and CPU are still operational. The AFE is not powered during standby mode. In standby mode, Flash is operational only in read mode. Interrupts can be used to bring the system out of standby mode or the power management can detect that power has been restored and software will bring the device out of standby mode.

DCLK is also used to drive the timing for the SPP and UART peripherals. Care must be taken to ensure these clock dividers are changed when the DCLK speed is changed.

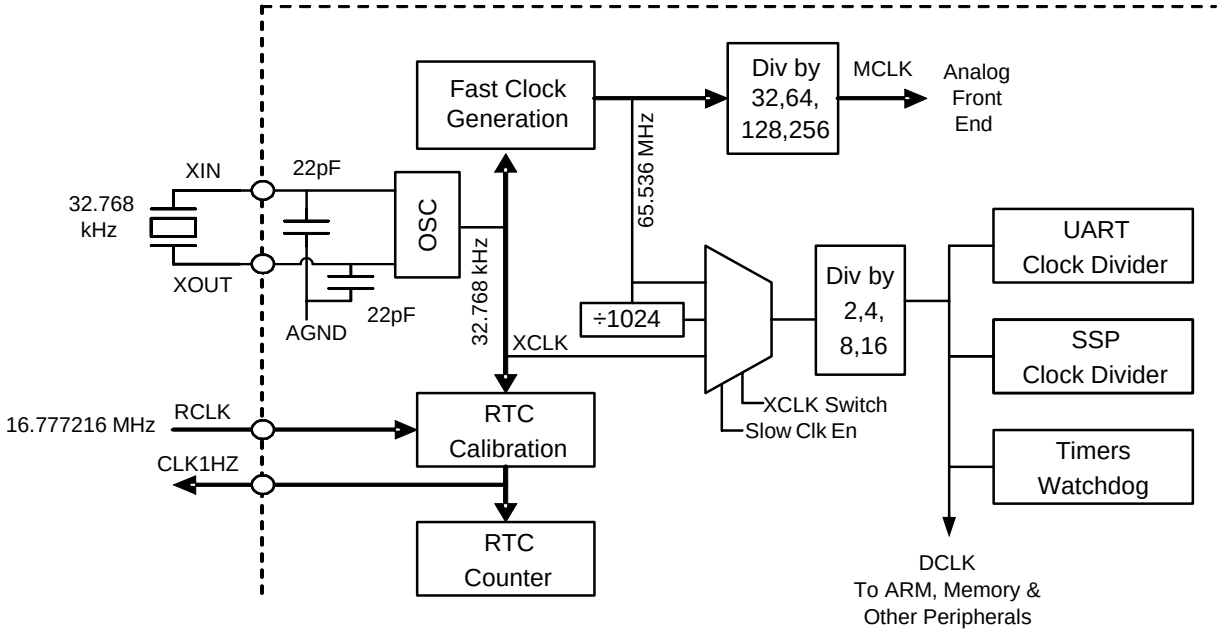



**Figure 14. Clock Generation Diagram**

### 5.4.2 UART/IRDAs

Each of the two UARTs is a serial communication controller with full infrared support which is also compatible to industry-standard 16C550 UART devices. These intelligent peripherals support the RS-232 and Infrared Data Association (IrDA®) SIR physical layer standards. Modem control signals CTS, DCD, DSR and RI are supported. DTR and RTS signals are not supported and could be implemented using GPIOs.

The controllers have a 16-byte FIFO which frees the CPU of excessive software overhead. Interrupt support for all operations has been included in this architecture. The controllers offer programmable registers for routing interrupts and handshake signals.

The UARTs incorporate an IrDA SIR ENDEC (encoder/decoder). The IrDA physical layer specification is intended to define a half-duplex, infrared communication link for exchanging data over a distance of up to 1 meter. The full standard includes data rates up to 115 kbps.

UART0 is the dedicated communication interface to a host PC when the CS7401xx is running in ROM EDM Profile.

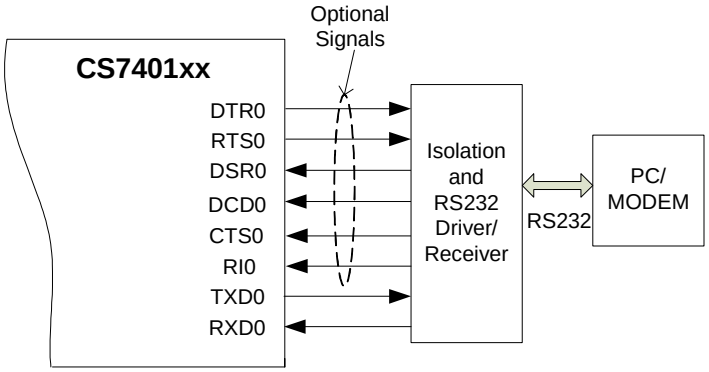



**Figure 15. Typical UART Connections**

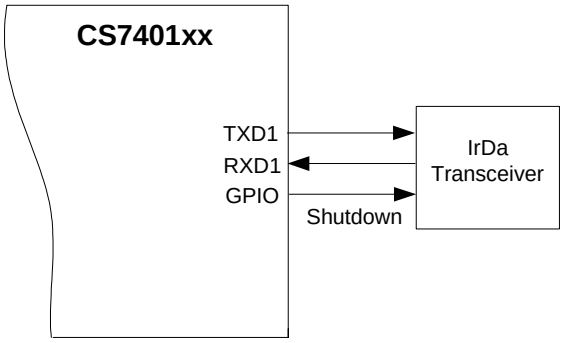



**Figure 16. Typical IrDA Connections**

### 5.4.3 Synchronous Serial Communication Port

The synchronous serial communication port (SSP) provides a convenient method of serial interaction for high-speed communication between similar shift-register-type devices. The SSP is a programmable serial port that is an AMBA® APB intelligent peripheral. The SSP port supports Motorola® SPI™ format, TI® synchronous serial format, and National Semiconductor® Microwire™ format.

The SSP is a high-speed, synchronous serial, input/output port that allows a serial bit stream of programmed length (4 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SSP is normally used for communication between the CPU and external peripherals or another microcontroller. Typical applications include interface to external I/O or peripheral expansion via devices such as nonvolatile memory, display drivers, and digital-to-analog converters.

The SSP is equipped with four communication interface signals. The pins SPICLK0, SPIRXD, and SPITXD are used in all SSP pin modes. The pin SPCS0 is optional and may be used if the pin is configured.

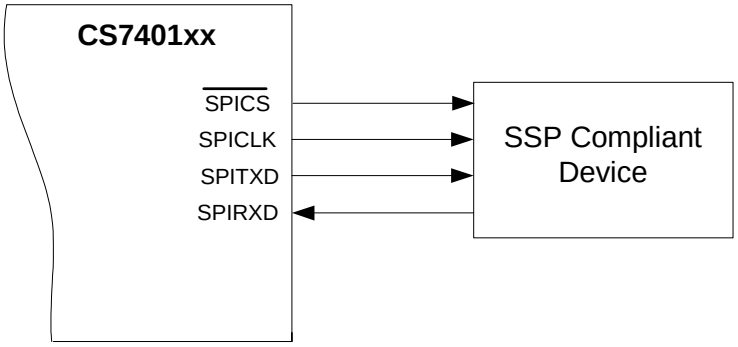



**Figure 17. CS7401xx SSP Port Connections in Master Mode**

### 5.4.4 LCD Controller/Driver

The LCD controller generates the timing signals that drive a static or multiplexed LCD panel, with support for up to 30 segments multiplexed with up to four common signals. The LCD controller consists of a control register, 3 display memory registers and 3 buffer registers. The control register defines the mux mode, number of segments, LCD frequency and blinking control, etc. Display memory registers defines the pixels display on or off. Display memory registers are written through buffer registers. To drive a LCD panel, the corresponding segment and common pins have to be configured as LCD driver enabled.

LCD controller features include:

- display buffer
- blink capability
- configurable frame frequency and blink frequency
- number of segments programmable
- support for four types of LCDs: static, 2-mux, 3-mux, and 4-mux

#### 5.4.4.1 Operation

The number of pixels that an LCD can drive is given by the mux mode times the number of segment pins. The voltage applied across a particular pixel is the voltage on the COM pin minus the voltage on the SEG pin. If the resulting voltage is above the $V_{on}$ threshold voltage, the pixel is visible. If the voltage is below the $V_{off}$ threshold voltage, the pixel will not be visible. In multiplexed LCD applications, the segment data for the second, third, and fourth column of the display memory are time-multiplexed with COM1, COM2, and COM3 respectively.

#### 5.4.4.2 LCD Operating Frequencies Example

- When DCLK = 4.096MHz, $f_{LCD}$ is programmable among 1 kHz, 512 Hz, 256 Hz, 128 Hz, 64Hz, 32Hz and 16Hz
- $f_{LCD} = 2 * Muxmode * f_{frame}$
- When DCLK= 4.096MHz, the blink frequency is programmable among 0.03Hz, 0.06Hz, 0.12Hz, 0.25 Hz, 0.5 Hz, 1 Hz, and 2 Hz.

**Table 7. Modes of Operation**

| Mode | Voltage Across On Pixel | Voltage Across Off Pixel |
|---|---|---|
| Static | Vdd, -Vdd | 0 |
| 2-mux | Vdd, -Vdd | Vdd/2, -Vdd/2 |
| 3-mux | 2Vdd/3, -2Vdd/3 | Vdd/3, -Vdd/3 |
| 4-mux | 2Vdd/3, -2Vdd/3 | Vdd/3, -Vdd/3 |

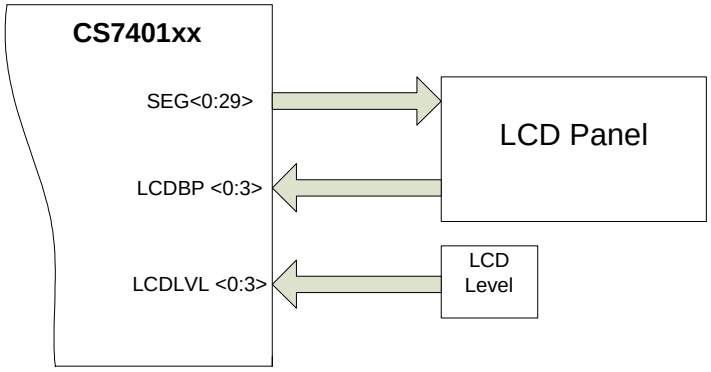



**Figure 18. CS7401xx LCD Connections**

### 5.4.5 Timers and Counters

In CS7401xx, two 32-bit and two 16-bit timers/counters are available and can be used for a wide range of functions:

- frequency measurement
- event counting
- interval measurement
- pulse generation
- delay timing
- Watchdog timer
- etc.

The timers are driven by a system clock and can be initialized by writing a count value through the APB. Each timer is a down counter with selectable pre-scale. The pre-scaler allows either the system clock to be used directly, or the clock (frequency) divided by 16 or 256 may be used. This functionality is provided by 0, 4, or 8 stages of pre-scale. Each timer may be configured as either a free running or a periodic timer. The timer is loaded by writing to the load register and then, if enabled, the timer will begin counting down. After reaching a zero count, an interrupt will be generated. The interrupt is cleared by writing to the clear register. If the timer is operating in free-running mode, it continues to count down from its maximum value after reaching a zero count. If the timer is operating in periodic mode, then the timer will reload from the load register after reaching a zero count and continue to count down. In this mode the timer will effectively generate a periodic interrupt. The timer mode is selected by a bit in the control register. In addition to the enable bit in the control register, the two 32-bit timers can also be enabled/disabled by pin inputs TE0 and TE1. One of the 32-bit timers can be used as a watchdog timer.

### 5.4.6 GPIOs

Pin14 to pin 55 of CS7401xx are functionality-multiplexed input/output pins. They can be configured individually as the input/output interfaces for the embedded peripherals such as LCD driver, SSP port, and UARTs, etc., or as general purpose digital input/outputs (GPIOs). When configured as input GPIOs, these pins also have interrupt generation capability. The interrupt properties of each GPIO pin are individually configurable.

**Because some of the I/O pins have special functionality after reset and by default, the following concerns must be taken carefully when using CS7401xx**.

1) After reset and by default, pin 14 through pin 34, and pin 36 through pin 43 are configured as LCD functionality.
2) After reset and by default, pin 35, and pin 44 through pin 55 are input GPIOs that need to be pulled to a high/low CMOS level externally.
3) Pin 52 (TXD1) has special factory-test functionality and has to be pulled down at reset.
4) Pin 55 (TXD0) acts as a Flash lock request at reset if it is high, so normally this pin should be pulled down at reset. Flash lock can be done by software.
5) Pin 50 is the BOOT pin and normally pulled high at reset in order to boot from ROM.
6) Pin 35 is the EM pin and normally pulled up at reset in order to run the application code after the booting from ROM. A pull-down option (through a button/switch) should also be provided to be able to run the ROM EDM Profile after reset.

# 6. USING A CS7401xx-BASED POWER METER

## 6.1 Calibration

### *6.1.1 AC/DC-Offset and Gain Calibration*

To ensure power measurement accuracy, a CS7401xx based power meter requires calibration prior to field use. When calibration completes, the calibration results are saved to Flash memory for subsequent use. Factory-embedded Energy Monitor firmware provides all the power measurement calibration functions through calibration components. This section discusses the technical details and steps for calibrating a CS7401xx power meter.

The CS7401xx provides DC-offset and gain calibration that are applied to the voltage and current measurement, and AC-offset calibration, which is applied to the voltage and current RMS calculations. Since all ADC channels have independent offset and gain calibration values, users can perform offset and gain calibration on any path independently. In power meter applications with high-pass filters enabled, DC offset is optional. For most applications, AC offset calibration is not required.

Figure 19 demonstrates the algorithms within the calibration data flow. The value in the APR (Accumulation Period Register), which is passed during component initialization, determines the number (N) of samples averaged during calibration. DC-offset and gain calibrations take N + $T_{SETTLE}$ samples. As N is increased, the accuracy of calibration results also increases. Cirrus Logic recommends setting N and $T_{SETTLE}$ to at least 4000 samples.

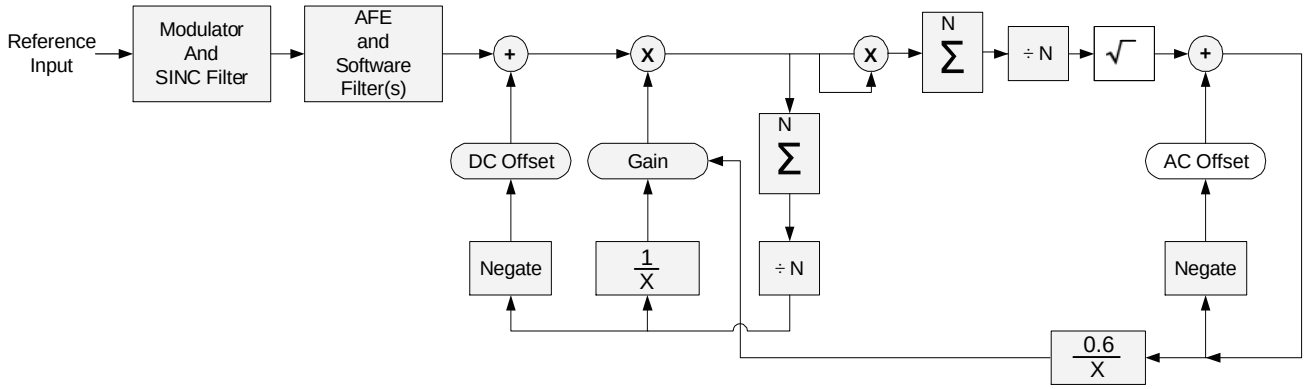



**Figure 19. DC/AC-Offset and Gain Data Flow**

#### *6.1.1.1 Offset Calibration*

During offset calibrations, no line voltage or current should be applied to the power meter.

#### *DC-Offset Calibration*

The DC-offset calibration function measures and averages DC values on the specified ADC channel with zero input and returns the inverse result. This result is passed to the AFE device driver during initialization and added to instantaneous measurements in subsequent conversions, removing the DC offset. Prior to performing DC offset calibration, the gain of the channel should be set to 1.0.

#### *AC-Offset Calibration*

The AC offset calibration function measures the residual RMS value on the specified ADC channel with zero input and returns the inverse result. This result is passed to the power utilities component during initialization and added to RMS measurements in subsequent conversions, removing the AC offset.

#### *6.1.1.2 Gain Calibration*

During gain calibration, reference voltage and current must be applied to the power meter, or optionally, apply scaled low-level signals to the AIN1± and AIN2± pins of the CS7401xx. Either AC or DC low-level reference signals can be used on the AIN1±

and AIN2± pins for AC gain calibration. If a DC signal is used, the associated high-pass filter (HPF) must be disabled. Using a reference that is too large or too small can cause an out-of-range condition and should be avoided. Refer to the *5.1.1 Analog Channels* on page 19 for the maximum input voltages on AIN1± and AIN2± pins.

#### *AC Gain Calibration*

Normally the maximum current (Imax) and reference voltage (Un) are used for AC gain calibration and Irms/Vrms will be calibrated to 60% of the full-scale register value.

During AC gain calibration, the RMS level of the applied reference is measured with the preset gain, then divided into 0.6 and the quotient is returned as the gain calibration value.

#### *DC Gain Calibration*

With a DC reference applied, the DC gain calibration function measures and averages DC values on the specified voltage or current paths and returns the reciprocal result as the gain calibration value. For power/energy measurement applications, DC gain calibration is not applicable.

#### *6.1.1.3 Calibration Order*

1. DC Offset (if needed)
2. AC Gain
3. AC Offset (if needed)

If both AC gain and offset calibrations were performed, it is possible to repeat both to obtain additional accuracy as AC gain and offset may interact.

### *6.1.2 Temperature Sensor Calibration*

By setting the appropriate bits in the CONFIG_TS register, the internal temperature sensor can be routed to ADC channel 2 or channel 3. Temperature calculation and calibration functions are provided through the components in Energy Monitor firmware. Temperature sensor calibration involves the adjustment of two internal parameters: Temperature Gain and Temperature Offset. These parameters are applied to measured temperature in the following way:

TemperatureReported = [TemperatureRead * TemperatureGain] + TemperatureOffset

By default, Temperature Gain is 1 and Temperature Offset is 0. The temperature calibration process involves the software reporting a temperature and then the user manually calculating the Gain and Offset using the external temperature reference.

#### *6.1.2.1 Temperature Gain Calibration*

To calibrate temperature gain, use two temperature points far enough apart to give reasonable accuracy, for example 25°C and 85°C. Divide the actual temperature difference by the software measured difference for the two temperatures, resulting in a gain correction factor. Save this value as the Temperature Gain and it will be multiplied as shown above.

#### *6.1.2.2 Temperature Offset Calibration*

Even though users can perform offset calibration at any temperature, Cirrus Logic recommends a temperature of mid-scale if any gain error exists. Subtract the software measured temperature from the actual temperature to determine the offset error. Save this value as the Temperature Offset and it will be added as shown above.

### *6.1.3 RTC Calibration*

RTC calibration requires a very stable and accurate 16.777216 MHz clock source connected to the CS7401xx RCLK pin (51). The RTC device driver in Energy Monitor firmware provides RTC calibration software functions. Both hardware and software controls the RTC calibration process. The calibration duration is 1, 2, or 4 seconds configurable. After calibration completes, software stores the calibrated value in the RTCINCR register.

### 6.1.4 Power Offset Calibration

Power offset calibration compensates for erroneous power sources resident in the metering system not originating from the power line. Residual power offsets occur due to crosstalk between current and voltage channels (ADC channels 1, 2, and 3), or due to ripple within the power meter or the CS7401xx SoC power supply. Positive or negative offsets indicate crosstalk coupling either in phase or out of phase with the applied voltage input. Power offset calibration is performed without a load connected (current channel). Power offset calibration is one of the calibration components provided by the Energy Monitor firmware.

### 6.1.5 Phase Compensation Calibration

Phase compensation calibration is implemented by setting the different time delays on both voltage and current ADC paths. CS7401xx ADC hardware provides up to 63 samples delay (1 hardware sample delay = 1/MCLK) on voltage channel. Energy Monitor can provides a software delay of up to 3 samples (1 software sample delay = 1/OWR) on both voltage and current channel.

The phase calibration component calculates the phase shift between the voltage channel and the current channel using wavelet technology and translates the phase shift into the number of samples of delay needed on the voltage and current ADC paths. The actual compensated phase shift in degrees is also depended on the line frequency. Table 7 lists the phase ranges and step sizes that the phase calibration component can calibrate precisely based on different MCLK/OWR and line frequencies.

For the phase shift beyond the ranges in Table 7, the application code needs to calculate phase shift and set the delay by itself to make the phase compensation. The maximum phase shift ranges that could be compensated are listed in table 8.

Energy Monitor requires the OWR to be 4KHz with BR-filter disabled or 8KHz with BR-filter enabled.

**Table 8. Phase Compensation Calibration Range**

| | 50 Hz | | 60 Hz | |
|---|---|---|---|---|
| **MCLK/OWR** | Range | Step Size | Range | Step Size |
| **256 kHz / 4KHz** | -6.75° ~ 8.96° | 0.0703° | -8.10° ~ 10.76° | 0.0844° |
| **512 kHz / 8KHz** | -6.703° ~ 8.854° | 0.0352° | -8.019° ~ 10.567° | 0.0422° |

**Table 9. Maximum Phase Compensation Range**

| | 50 Hz | 60 Hz |
|---|---|---|
| **MCLK/OWR** | Range | Range |
| **256 kHz / 4KHz** | -13.5° ~ 17.93° | -16.2° ~ 21.516° |
| **512 kHz / 8KHz** | -6.703° ~ 8.854° | -8.019° ~ 10.567° |

## 6.2 Energy Pulse and 1 Hz RTC Output

To support accuracy verification of energy measurement and RTC, the CS7401xx I/O pin 44 can be configured to provide the EPOUT or CLK1Hz signal.

When configured as EPOUT, pin 44 generates pulses of variable frequency that directly corresponds to the power values measured by the power utilities component in Energy Monitor firmware. EPOUT can output active, reactive, or apparent energy pulses. The energy type, polarity, the maximum pulse rate and pulse width are configurable through the power utilities component in the Energy Monitor.

When configured as CLK1Hz, pin 44 generates a fixed RTC 1 Hz reference clock. This 1Hz clock can used to measure or verify the accuracy of the CS7401xx RTC.

## 6.3 Typical Application Circuit

Figure 20 below show a typical CS7401xx based single phase power meter application circuit with the AIN3 channel used for tampering detection.

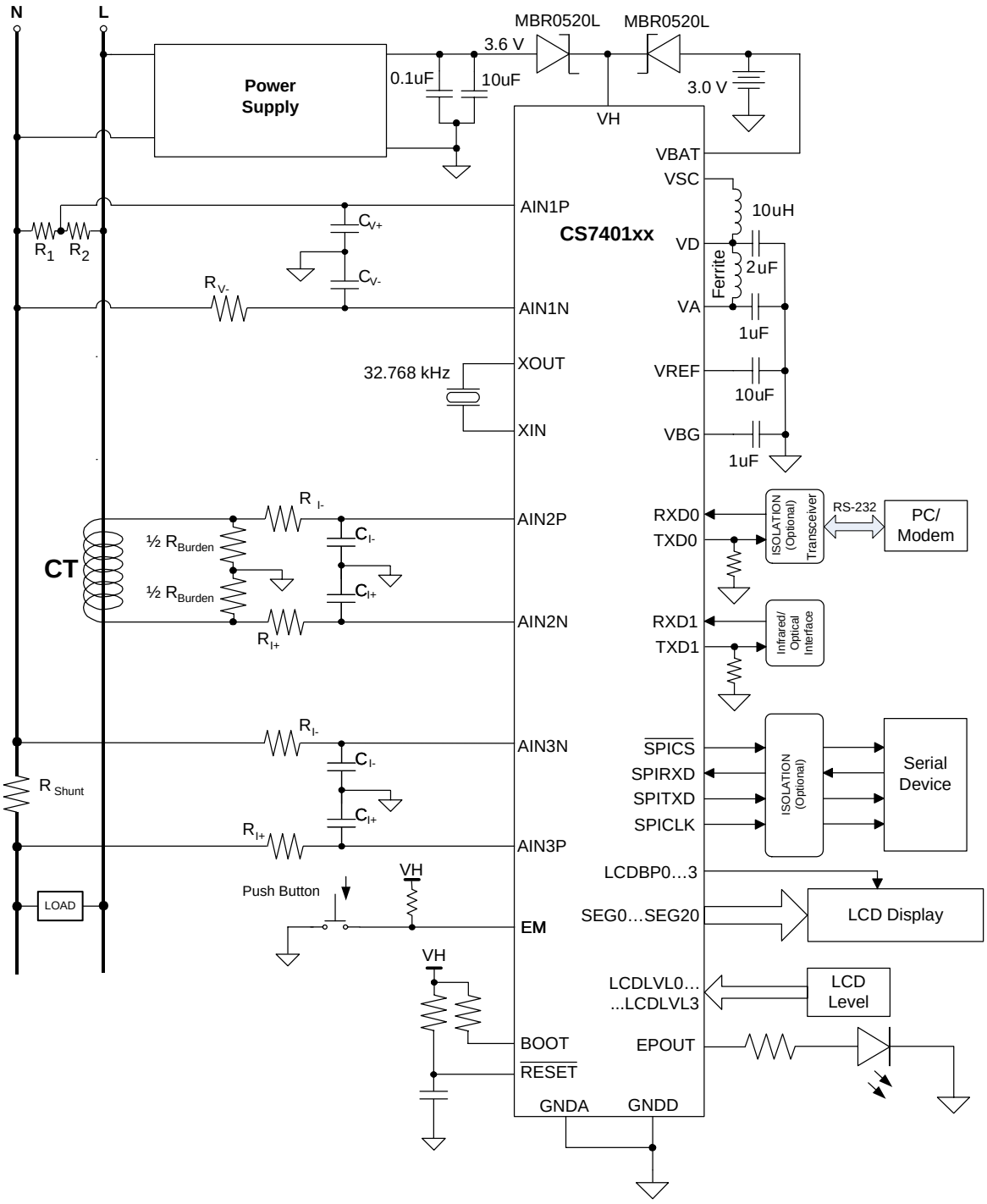
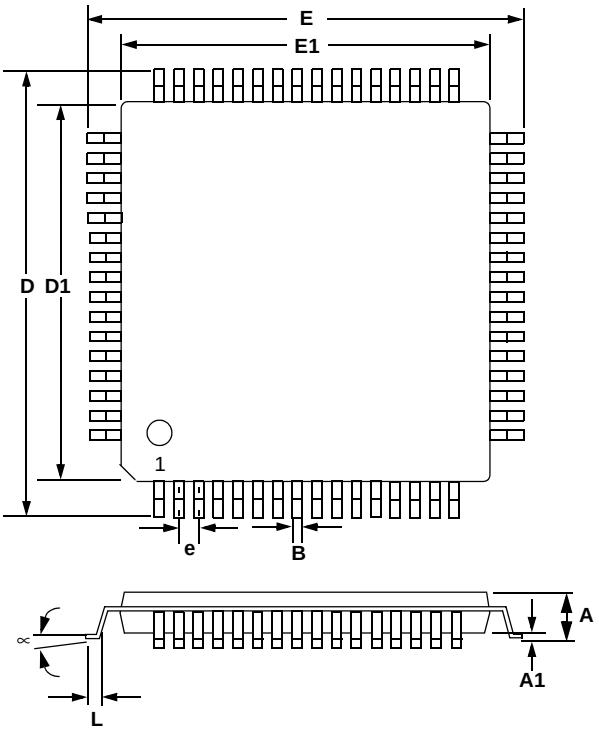



**Figure 20. Typical Connection Diagram *(Single-phase, 2-wire, direct connection power meter)***

## 7. PACKAGE INFORMATION

### 64L LQFP PACKAGE DRAWING




| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | 0.55 | 0.063 | --- | 1.40 | 1.60 |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| B | 0.007 | 0.008 | 0.011 | 0.17 | 0.20 | 0.27 |
| D | 0.461 | 0.472 BSC | 0.484 | 11.70 | 12.0 BSC | 12.30 |
| D1 | 0.390 | 0.393 BSC | 0.398 | 9.90 | 10.0 BSC | 10.10 |
| E | 0.461 | 0.472 BSC | 0.484 | 11.70 | 12.0 BSC | 12.30 |
| E1 | 0.390 | 0.393 BSC | 0.398 | 9.90 | 10.0 BSC | 10.10 |
| e* | 0.016 | 0.020 BSC | 0.024 | 0.40 | 0.50 BSC | 0.60 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| ∝ | 0.000° | 4° | 7.000° | 0.00° | 4° | 7.00° |

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

## 8. ORDERING INFORMATION

| Model | Package | Temperature |
|---|---|---|
| CS740111-IQZ (32 kB Flash) | 64-pin LQFP | -40 to +85 °C |
| CS740121-IQZ (64 kB Flash) | | |
| CS740131-IQZ (128 kB Flash) | | |

## 9. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

| Model Number | Peak Reflow Temp | MSL Rating* | Max Floor Life |
|---|---|---|---|
| CS740111-IQZ | 250 °C | 3 | 7 Days |
| CS740121-IQZ | | | |
| CS740131-IQZ | | | |

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

## REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| A1 | October 2007 | Advance Release |
| PP1 | April 2008 | Initial Preliminary Release |
| PP2 | April 2008 | Preliminary Release |
| PP3 | August 2008 | Initial Public Release |
| F1 | August 2008 | Final Release |

## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to **www.cirrus.com**

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