Low Cost Quad Voltage Controlled Amplifier

SSM2164

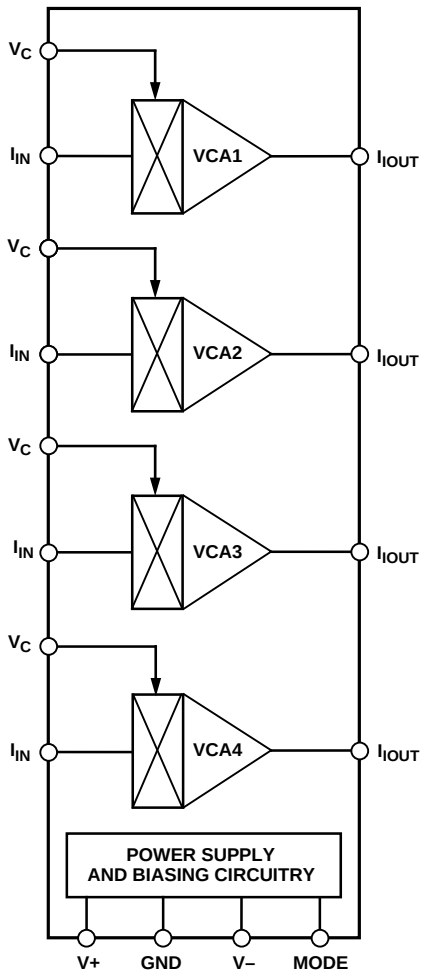
FEATURES

Four High Performance VCAs in a Single Package
0.02% THD
No External Trimming
120 dB Gain Range
0.07 dB Gain Matching (Unity Gain)
Class A or AB Operation

APPLICATIONS

Remote, Automatic, or Computer Volume Controls
Automotive Volume/Balance/Faders
Audio Mixers
Compressor/Limiters/Compandors
Noise Reduction Systems
Automatic Gain Controls
Voltage Controlled Filters
Spatial Sound Processors
Effects Processors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2164 contains four independent voltage controlled amplifiers (VCAs) in a single package. High performance (100 dB dynamic range, 0.02% THD) is provided at a very low cost-per-VCA, resulting in excellent value for cost sensitive gain control applications. Each VCA offers current input and output for maximum design flexibility, and a ground referenced –33 mV/dB control port.

All channels are closely matched to within 0.07 dB at unity gain, and 0.24 dB at 40 dB of attenuation. A 120 dB gain range is possible.

A single resistor tailors operation between full Class A and AB modes. The pinout allows upgrading of SSM2024 designs with minimal additional circuitry.

The SSM2164 will operate over a wide supply voltage range of ±4 V to ±18 V. Available in 16-pin P-DIP and SOIC packages, the device is guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

REV. 0

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SSM2164–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (V_S = ±15 V, A_V = 0 dB, 0 dBu = 0.775 V rms, V_{IN} = 0 dBu, R_{IN} = R_{OUT} = 30 kΩ, f = 1 kHz, –40°C < T_A < +85°C using Typical Application Circuit (Class AB), unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	SSM2164 Min	Typ	Max	Units
AUDIO SIGNAL PATH					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–94		dBu
Headroom	Clip Point = 1% THD+N		22		dBu
Total Harmonic Distortion	2nd and 3rd Harmonics Only				
	A_V = 0 dB, Class A		0.02	.1	%
	A_V = ±20 dB, Class A[1]		0.15		%
	A_V = 0 dB, Class AB		0.16		%
	A_V = ±20 dB, Class AB[1]		0.3		%
Channel Separation			–110		dB
Unity Gain Bandwidth	C_F = 10 pF		500		kHz
Slew Rate	C_F = 10 pF		0.7		mA/µs
Input Bias Current			±10		nA
Output Offset Current	V_{IN} = 0		±50		nA
Output Compliance			±0.1		V
CONTROL PORT					
Input Impedance			5		kΩ
Gain Constant	(Note 2)		–33		mV/dB
Gain Constant Temperature Coefficient			–3300		ppm/°C
Control Feedthrough	0 dB to –40 dB Gain Range[3]		1.5	8.5	mV
Gain Matching, Channel-to-Channel	A_V = 0 dB		0.07		dB
	A_V = –40 dB		0.24		dB
Maximum Attenuation			–100		dB
Maximum Gain			+20		dB
POWER SUPPLIES					
Supply Voltage Range		±4		±18	V
Supply Current	Class AB		6	8	mA
Power Supply Rejection Ratio	60 Hz		90		dB

NOTES
[1]–10 dBu input @ 20 dB gain; +10 dBu input @ –20 dB gain.
[2]After 60 seconds operation.
[3]+25°C to +85°C.
Specifications subject to change without notice.

TYPICAL APPLICATION AND TEST CIRCUIT

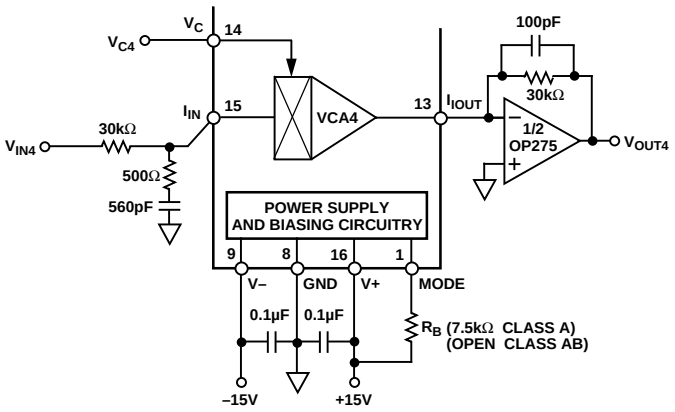


Figure 1. R_{IN} = R_{OUT} = 30 kΩ, C_F = 100 pF. Optional R_B = 7.5 kΩ, Biases Gain Core to Class A Operation. For Class AB, Omit R_B.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Input, Output, Control Voltages . . . . . V– to V+
Output Short Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
16-Pin Plastic DIP (P Suffix)	76	33	°C/W
16-Pin SOIC (S Suffix)	92	27	°C/W

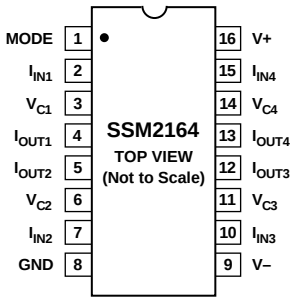
*θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for P-DIP packages, θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
SSM2164P	–40°C to +85°C	Plastic DIP	N-16
SSM2164S	–40°C to +85°C	Narrow SOIC	R-16A

PIN CONFIGURATION

16-Lead Epoxy DIP and SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2164 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics

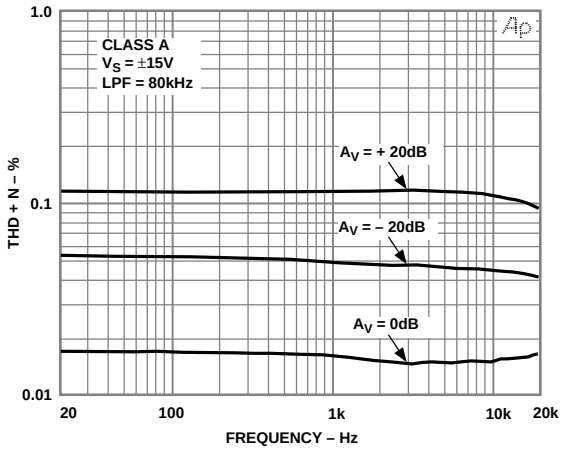


Figure 2. THD+N vs. Frequency, Class A

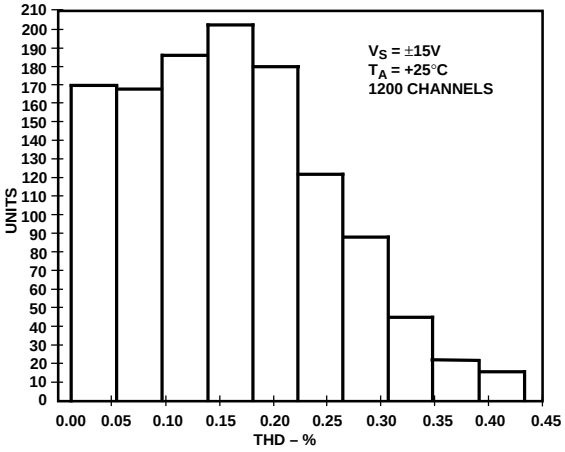


Figure 5. THD Distribution, Class AB

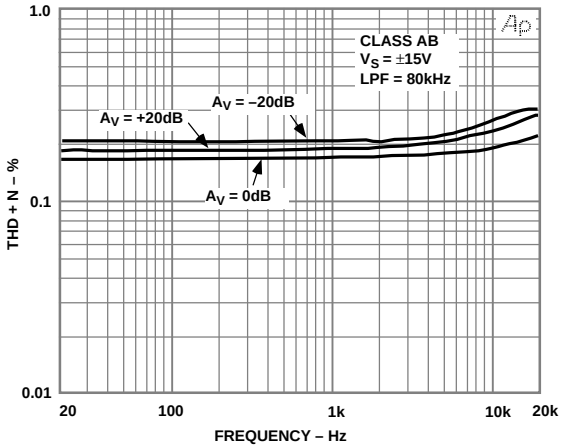


Figure 3. THD+N vs. Frequency Class, AB

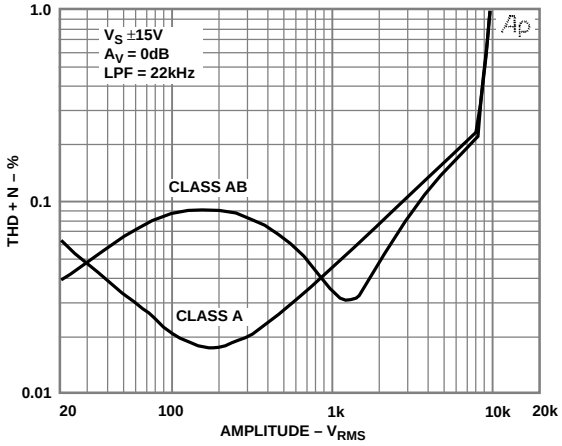


Figure 6. THD+N vs. Amplitude

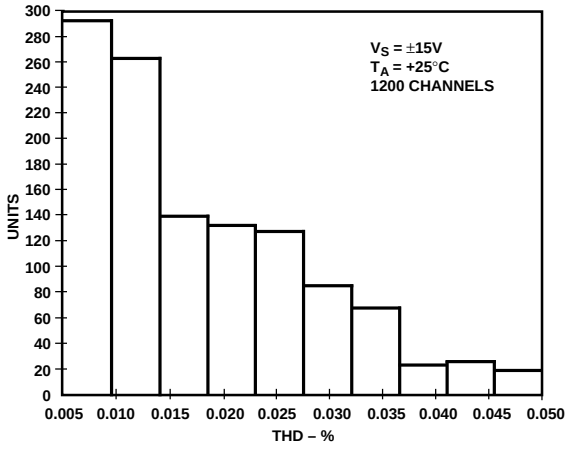


Figure 4. THD Distribution, Class A

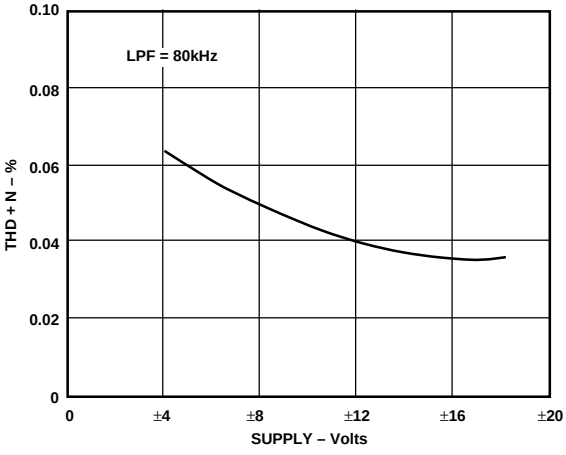


Figure 7. THD+N vs. Supply Voltage, Class A

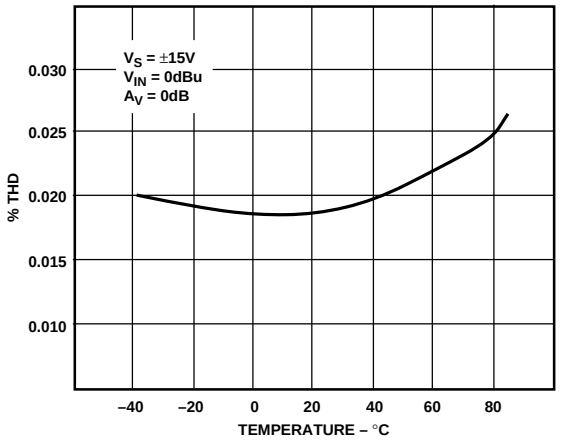


Figure 8. THD vs. Temperature, Class A

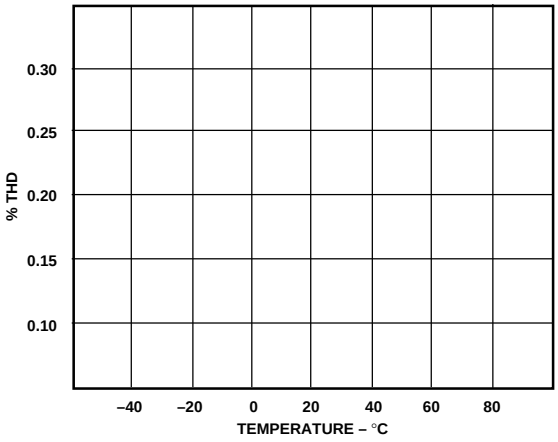


Figure 9. THD vs. Temperature, Class AB

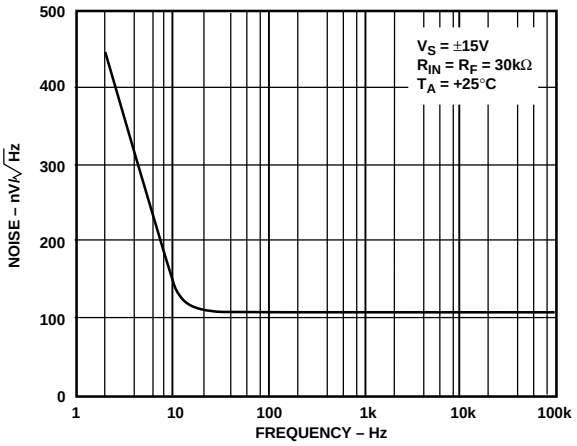


Figure 10. Voltage Noise Density vs. Frequency, Class AB

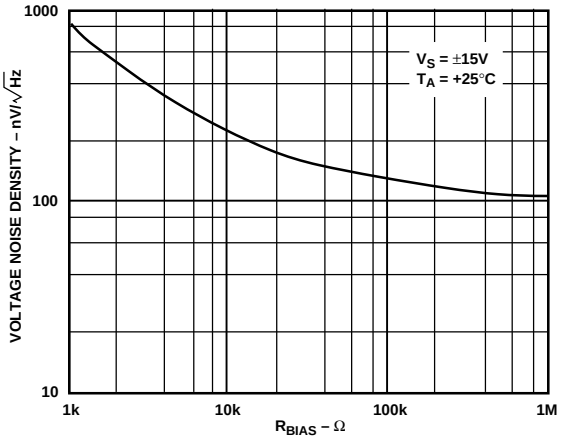


Figure 11. Voltage Noise Density vs. R_{BIAS}

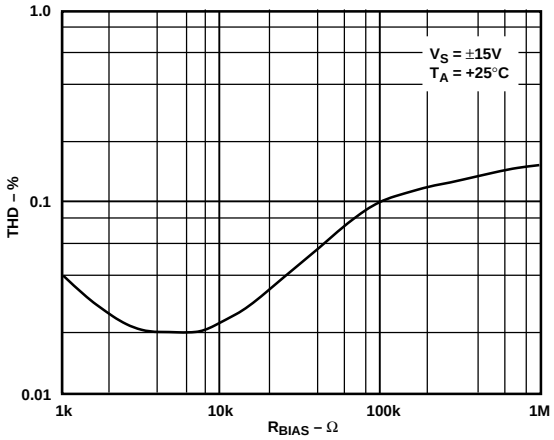


Figure 12. THD vs. R_{BIAS}

Figure 13. Control Feedthrough vs. R_{BIAS}

Typical Performance Characteristics

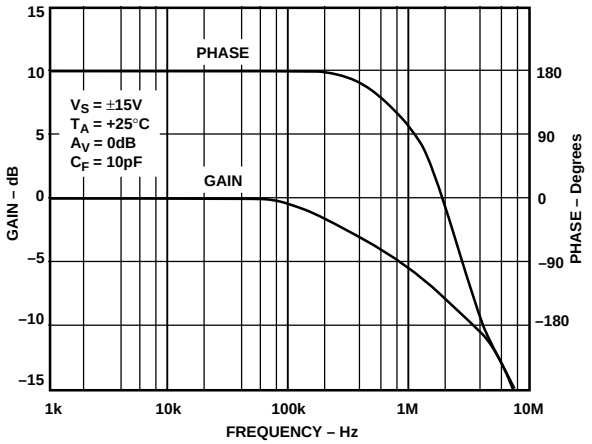


Figure 14. Gain/Phase vs. Frequency

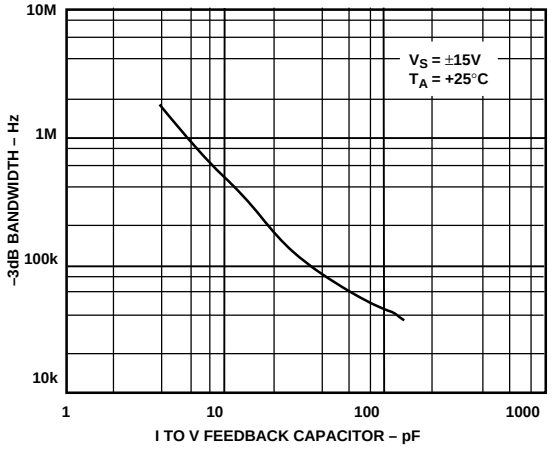


Figure 17. –3 dB Bandwidth vs. I-to-V Feedback Capacitor

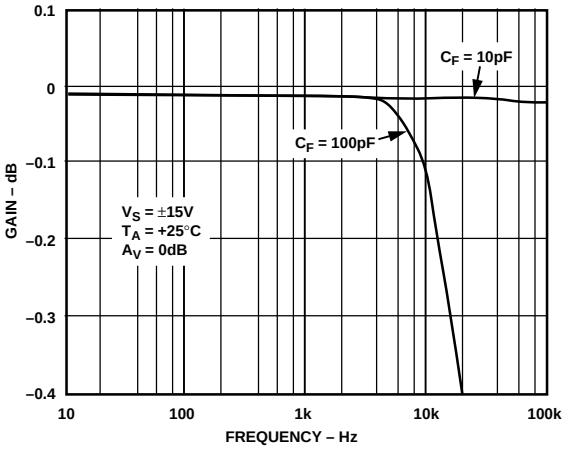


Figure 15. Gain Flatness vs. Frequency

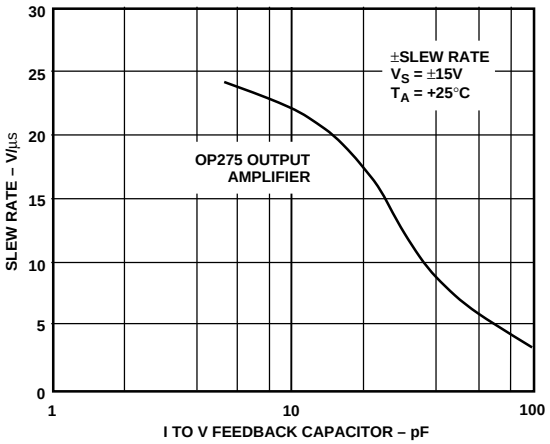


Figure 18. Slew Rate vs. I-to-V Feedback Capacitor

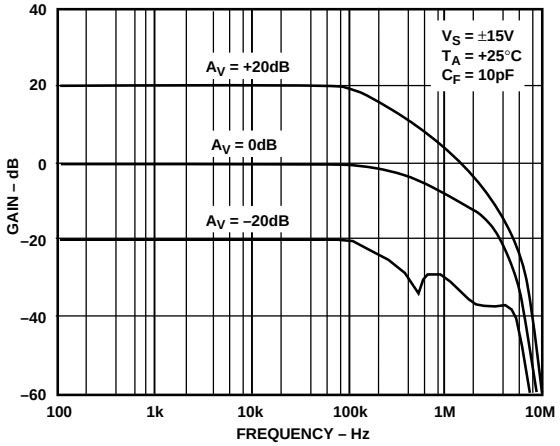


Figure 16. Bandwidth vs. Gain

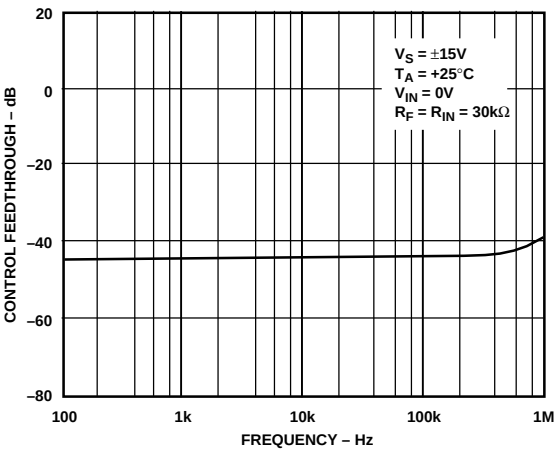


Figure 19. Control Feedthrough vs. Frequency

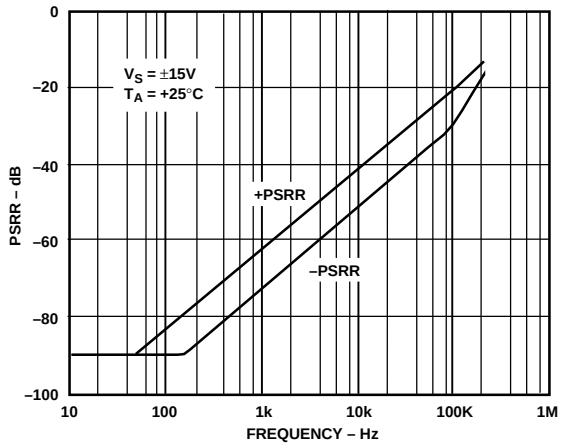


Figure 20. PSRR vs. Frequency

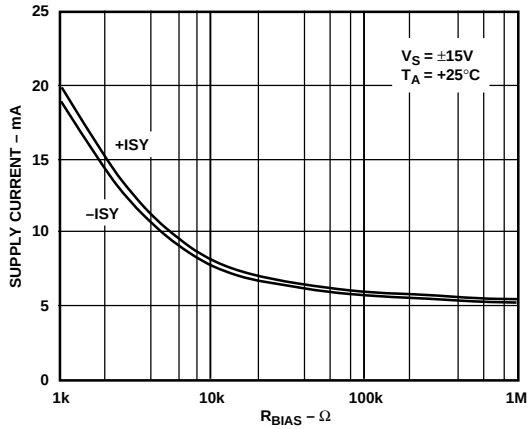


Figure 21. Supply Current vs. R_{BIAS}

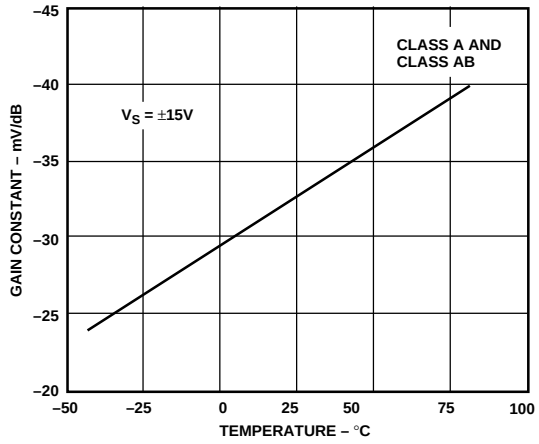


Figure 22. Gain Constant vs. Temperature

APPLICATIONS INFORMATION

Circuit Description

The SSM2164 is a quad Voltage Controlled Amplifier (VCA) with 120 dB of gain control range. Each VCA is a current-in, current-out device with a separate –33 mV/dB voltage input control port. The class of operation (either Class A or Class AB) is set by a single external resistor allowing optimization of the distortion versus noise tradeoff for a particular application. The four independent VCAs in a single 16-pin package make the SSM2164 ideal for applications where multiple volume control elements are needed.

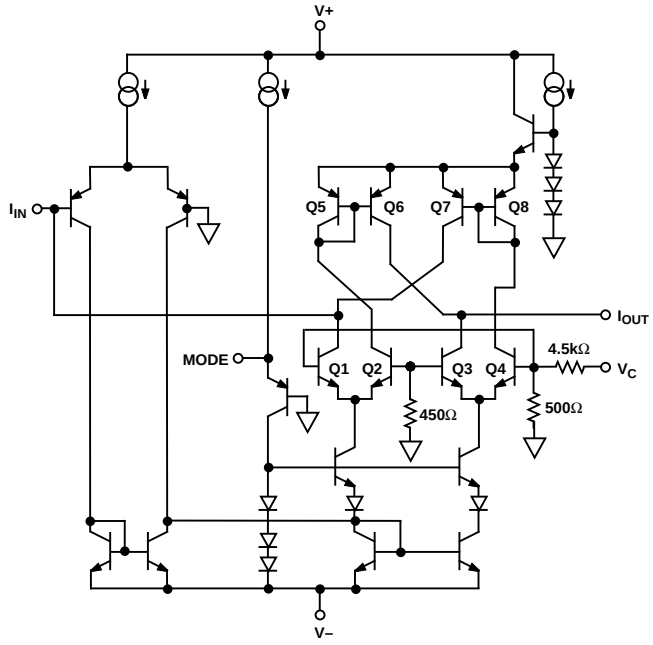


Figure 23. Simplified Schematic (One Channel)

The simplified schematic in Figure 23 shows the basic structure of one of the four VCAs in the device. The gain core is comprised of the matched differential pairs Q1-Q4 and the current mirrors of Q5, Q6 and Q7, Q8. The current input pin, I_{IN}, is connected to the collectors of Q1 and Q7, and the difference in current between these two transistors is equivalent to I_{IN}. For example, if 100 µA is flowing into the input, Q1's collector current will be 100 µA higher than Q7's collector current.

Varying the control voltage V_C, steers the signal current from one side of each differential pair to the other, resulting in either gain or attenuation. For example, a positive voltage on V_C steers more current through Q1 and Q4 and decreases the current in Q2 and Q3. The current output pin, I_{OUT}, is connected to the collector of Q3 and the current mirror (Q6) from Q2. With less current flowing through these two transistors, less current is available at the output. Thus, a positive V_C attenuates the input and a negative V_C amplifies the input. The VCA has unity gain for a control voltage of 0.0 V where the signal current is divided equally between the gain core differential pairs.

The MODE pin allows the setting of the quiescent current in the gain core of the VCA to trade off the SSM2164's THD and noise performance to an optimal level for a particular application. Higher current through the core results in lower distortion

but higher noise, and the opposite is true for less current. The increased noise is due to higher current noise in the gain core transistors as their operating current is increased. THD has the opposite relationship to collector current. The lower distortion is due to the decrease in the gain core transistors' emitter impedance as their operating current increases.

This classical tradeoff between THD and noise in VCAs is usually expressed as the choice of using a VCA in either Class A or Class AB mode. Class AB operation refers to running a VCA with less current in the gain core, resulting in lower noise but higher distortion. More current in the core corresponds to Class A performance with its lower THD but higher noise. Figures 11 and 12 show the THD and noise performance of the SSM2164 as the bias current is adjusted. Notice the two characteristics have an inverse characteristic.

The quiescent current in the core is set by adding a single resistor from the positive supply to the MODE pin. As the simplified schematic shows, the potential at the MODE pin is one diode drop above the ground pin. Thus, the formula for the MODE current is:

$$I_{MODE} = \frac{(V+) - 0.6\,V}{R_B}$$

With ±15 V supplies, an R_B of 7.5k gives Class A biasing with a current of 1.9 mA. Leaving the MODE pin open sets the SSM2164 in Class AB with 30 µA of current in the gain core.

Basic VCA Configuration

Figure 24 shows the basic application circuit for the SSM2164. Each of the four channels is configured identically. A 30 kΩ resistor converts the input voltage to an input current for the VCA. Additionally, a 500 Ω resistor in series with a 560 pF capacitor must be added from each input to ground to ensure stable operation. The output current pin should be maintained at a virtual ground using an external amplifier. In this case the OP482 quad JFET input amplifier is used. Its high slew rate, wide bandwidth, and low power make it an excellent choice for the current-to-voltage converter stage. A 30 kΩ feedback resistor is chosen to match the input resistor, giving unity gain for a 0.0 V control voltage. The 100 pF capacitors ensure stability and reduce high frequency noise. They can be increased to reduce the low pass cutoff frequency for further noise reduction.

For this example, the control voltage is developed using a 100 kΩ potentiometer connected between +5 V and ground. This configuration results in attenuation only. To produce both gain and attenuation, the potentiometer should be connected between a positive and negative voltage. The control input has an impedance of 5 kΩ. Because of this, any resistance in series with V_C will attenuate the control signal. If precise control of the gain and attenuation is required, a buffered control voltage should be used.

Notice that a capacitor is connected from the control input to ground. Because the control port is connected directly to the gain core transistors, any noise on the V_C pin will increase the output noise of the VCA. Filtering the control voltage ensures that a minimal amount of noise is introduced into the VCA, allowing its full performance to be realized. In general, the largest possible capacitor value should be used to set the filter at a low cutoff frequency. The main exception to this is in dynamic processing applications, where faster attack or decay times may be needed.

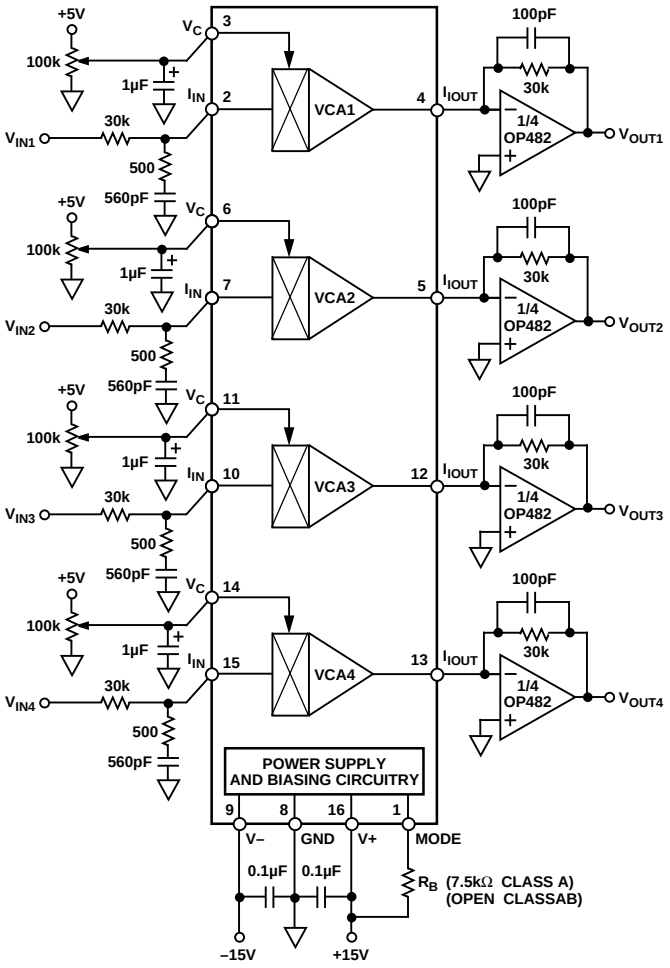


Figure 24. Basic Quad VCA Configuration

Low Cost, Four-Channel Mixer

The four VCAs in a single package can be configured to create a simple four-channel mixer as shown in Figure 25. The inputs and control ports are configured the same as for the basic VCA, but the outputs are summed into a single output amplifier. The OP176 is an excellent amplifier for audio applications because of its low noise and distortion and high output current drive. The amount of signal from each input to the common output can be independently controlled using up to 20 dB of gain or as much as 100 dB of attenuation. Additional SSM2164s could be added to increase the number of mixer channels by simply summing their outputs into the same output amplifier. Another possible configuration is to use a dual amplifier such as the OP275 to create a stereo, two channel mixer with a single SSM2164.

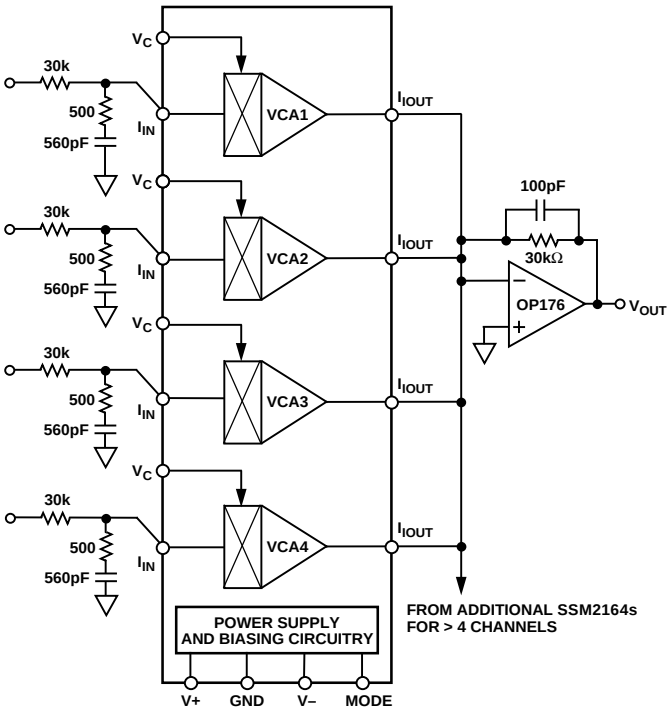


Figure 25. Four-Channel Mixer (4 to 1)

If additional SSM2164s are added, the 100 pF capacitor may need to be increased to ensure stability of the output amplifier. Most op amps are sensitive to capacitance on their inverting inputs. The capacitance forms a pole with the feedback resistor, which reduces the high frequency phase margin. As more SSM2164's are added to the mixer circuit, their output capacitance and the parasitic trace capacitance add, increasing the overall input capacitance. Increasing the feedback capacitor will maintain the stability of the output amplifier.

Digital Control of the SSM2164

One option for controlling the gain and attenuation of the SSM2164 is to use a voltage output digital-to-analog converter such as the DAC8426 (Figure 26), whose 0 V to +10 V output controls the SSM2164's attenuation from 0 dB to –100 dB. Its simple 8-bit parallel interface can easily be connected to a microcontroller or microprocessor in any digitally controlled system. The voltage output configuration of the DAC8426 provides a low impedance drive to the SSM2164 so the attenuation can be controlled accurately. The 8-bit resolution of the DAC and its full-scale voltage of +10 V gives an output of 3.9 mV/bit. Since the SSM2164 has a –33 mV/dB gain constant, the overall control law is 0.12 dB/bit or approximately 8 bits/dB. The input and output configuration for the SSM2164 is the same as for the basic VCA circuit shown earlier. The 4-to-1 mixer configuration could also be used.

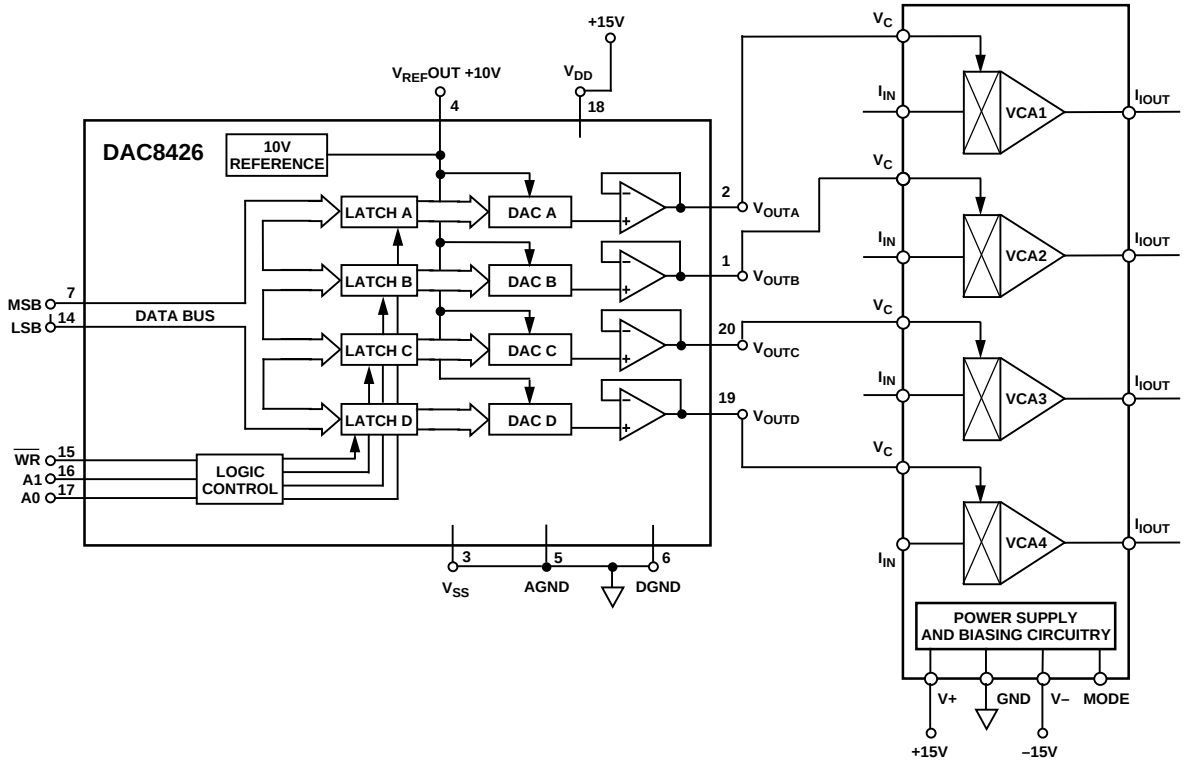


Figure 26. Digital Control of VCA Gain

Single Supply Operation

The SSM2164 can easily be operated from a single power supply as low as +8 V or as high as +36 V. The key to using a single supply is to reference all ground connections to a voltage midway between the supply and ground as shown in Figure 27. The OP176 is used to create a pseudo-ground reference for the SSM2164. Both the OP482 and OP176 are single supply amplifiers and can easily operate over the same voltage range as the SSM2164 with little or no change in performance.

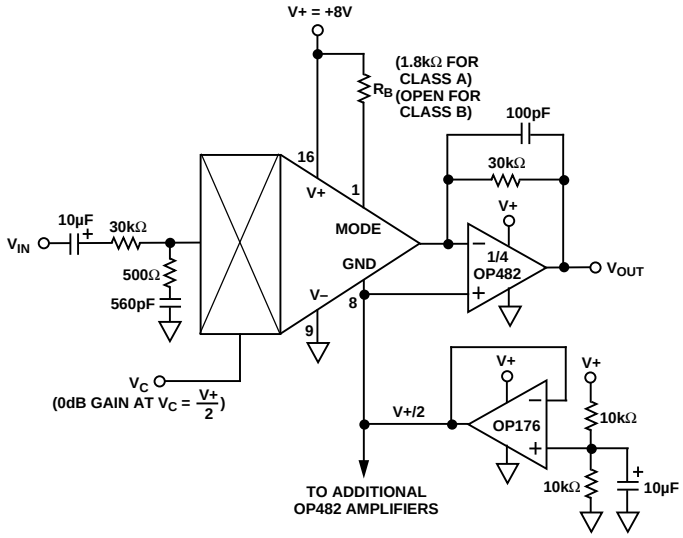


Figure 27. Single Supply Operation of the SSM2164 (One Channel Shown)

The reference voltage is set by the resistor divider from the positive supply. Two 10 kΩ resistors create a voltage equal to the positive supply divided by 2. The 10 µF capacitor filters the supply voltage, providing a low noise reference to the circuit. This reference voltage is then connected to the GND pin of the SSM2164 and the noninverting inputs of all the output amplifiers. It is important to buffer the resistor divider with the OP176 to ensure a low impedance pseudo-ground connection for the SSM2164.

The input can either be referenced to this same mid-supply voltage or ac coupled as is done in this case. If the entire system is single supply, then the input voltage will most likely already be referenced to the midpoint; if this is the case, the 10 µF input capacitor can be eliminated. Unity gain is set when V_C equals the voltage on the GND pin. Thus, the control voltage should also be referenced to the same midsupply voltage.

The value of the MODE setting resistor may also change depending on the total supply voltage. Because the GND pin is at a pseudo-ground potential, the equation to set the MODE current now becomes:

$$I_{MODE} = \frac{(V+) - V_{GND} - 0.6\,V}{R_B}$$

The value of 1.8 kΩ results in Class A biasing for the case of using a +8 V supply.

Upgrading SSM2024 Sockets

The SSM2164 is intended to replace the SSM2024, an earlier generation quad VCA. The improvements in the SSM2164 have resulted in a part that is not a drop-in replacement to the SSM2024, but upgrading applications with the SSM2024 is a simple task. The changes are shown in Figure 28. Both parts have identical pinouts with one small exception. The MODE input (Pin 1) does not exist on the SSM2024. It has fixed internal biasing, whereas flexibility was designed into the SSM2164. A MODE set resistor should be added for Class A operation, but if the SSM2164 is going to be operated in Class AB, no external resistor is needed.

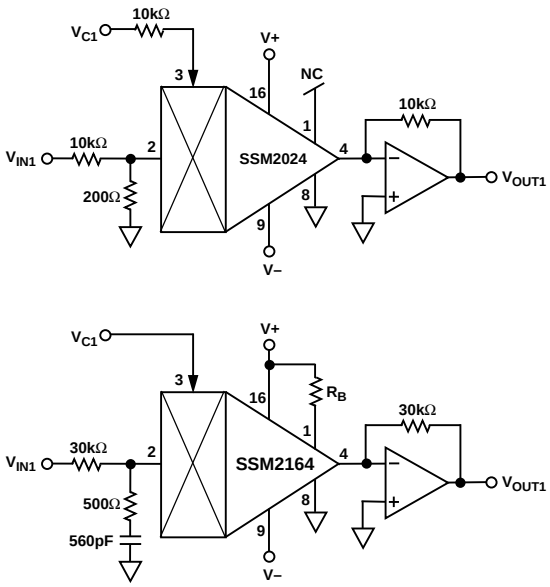


Figure 28. Upgrading SSM2024 Sockets with SSM2164

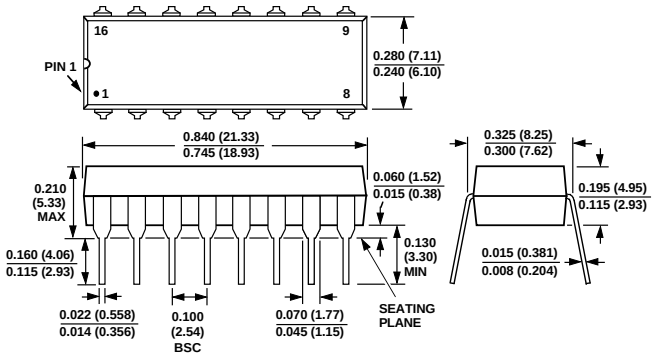
Since both parts are current output devices, the output configuration is nearly identical, except that the 10 kΩ resistors should be increased to 30 kΩ to operate the SSM2164 in its optimum range. The 10 kΩ input resistor for the SSM2024 should also be increased to 30 kΩ to match the output resistor. Additionally, the 200 Ω resistor should be replaced by a 500 Ω resistor in series with 560 pF for the SSM2164 circuit.

One last change is the control port configuration. The SSM2024's control input is actually a current input. Thus, a resistor was needed to change the control voltage to a current. This resistor should be removed for the SSM2164 to provide a direct voltage input. In addition, the SSM2024 has a log/log control relationship in contrast to the SSM2164's linear/log gain constant. The linear input is actually much easier to control, but the difference may necessitate adjusting a SSM2024 based circuit's control voltage gain curve. By making these relatively simple changes, the superior performance of the SSM2164 can easily be realized.

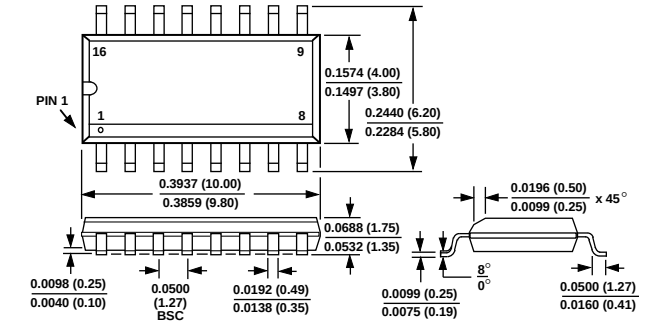
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic DIP (N-16)



16-Pin Narrow SOIC (R-16A)



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