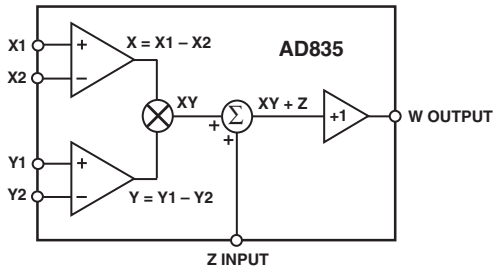
250 MHz, Voltage Output 4-Quadrant Multiplier

AD835

FEATURES
Simple: Basic Function is W = XY + Z
Complete: Minimal External Components Required
Very Fast: Settles to 0.1% of FS in 20 ns
DC-Coupled Voltage Output Simplifies Use
High Differential Input Impedance X, Y, and Z Inputs
Low Multiplier Noise: 50 nV/$\sqrt{Hz}$

APPLICATIONS
Very Fast Multiplication, Division, Squaring
Wideband Modulation and Demodulation
Phase Detection and Measurement
Sinusoidal Frequency Doubling
Video Gain Control and Keying
Voltage Controlled Amplifiers and Filters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD835 is a complete four-quadrant voltage output analog multiplier, fabricated on an advanced dielectrically isolated complementary bipolar process. It generates the linear product of its X and Y voltage inputs with a –3 dB output bandwidth of 250 MHz (a small signal rise time of 1 ns). Full scale (–1 V to +1 V) rise to fall times are 2.5 ns (with the standard R_L of 150 Ω), and the settling time to 0.1% under the same conditions is typically 20 ns.

Its differential multiplication inputs (X, Y) and its summing input (Z) are at high impedance. The low impedance output voltage (W) can provide up to ±2.5 V and drive loads as low as 25 Ω. Normal operation is from ±5 V supplies.

Though providing state-of-the-art speed, the AD835 is simple to use and versatile. For example, as well as permitting the addition of a signal at the output, the Z input provides the means to operate the AD835 with voltage gains up to about ×10. In this capacity, the very low product noise of this multiplier (50 nV/$\sqrt{Hz}$) makes it much more useful than earlier products.

The AD835 is available in an 8-lead PDIP package (N) and an 8-lead SOIC package (R) and is specified to operate over the –40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD835 is the first monolithic 250 MHz four quadrant voltage output multiplier.
2. Minimal external components are required to apply the AD835 to a variety of signal processing applications.
3. High input impedances (100 kΩ‖2 pF) make signal source loading negligible.
4. High output current capability allows low impedance loads to be driven.
5. State of the art noise levels achieved through careful device optimization and the use of a special low noise band gap voltage reference.
6. Designed to be easy to use and cost effective in applications which formerly required the use of hybrid or board level solutions.

REV. B

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AD835—SPECIFICATIONS (T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, $C_L \leq$ 5 pF, unless otherwise noted.)

Model		AD835AN/AR835			
TRANSFER FUNCTION		$W = \frac{(X1 - X2)(Y1 - Y2)}{U} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS (X, Y)					
Differential Voltage Range	V_{CM} = 0		±1		V
Differential Clipping Level		**±1.2**	±1.4		V
Low Frequency Nonlinearity	X = ±1 V, Y = 1 V		0.3	**0.5**	% FS
	Y = ±1 V, X = 1 V		0.1	**0.3**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]				
	X = ±1 V, Y = 1 V			0.7	% FS
	Y = ±1 V, X = 1 V			0.5	% FS
Common-Mode Voltage Range		–2.5		+3	V
Offset Voltage			±3	**±20**	mV
vs. Temperature	T_{MIN} to T_{MAX}[1]			±25	mV
CMRR	f ≤ 100 kHz; ±1 V p-p	**70**			dB
Bias Current			10	**20**	µA
vs. Temperature	T_{MIN} to T_{MAX}[1]			27	µA
Offset Bias Current			2		µA
Differential Resistance			100		kΩ
Single-Sided Capacitance			2		pF
Feedthrough, X	X = ±1 V, Y = 0 V			**–46**	dB
Feedthrough, Y	Y = ±1 V, X = 0 V			**–60**	dB
DYNAMIC CHARACTERISTICS					
–3 dB Small-Signal Bandwidth		150	250		MHz
–0.1 dB Gain Flatness Frequency			15		MHz
Slew Rate	W = –2.5 V to +2.5 V		1000		V/µs
Differential Gain Error, X	f = 3.58 MHz		0.3		%
Differential Phase Error, X	f = 3.58 MHz		0.2		Degrees
Differential Gain Error, Y	f = 3.58 MHz		0.1		%
Differential Phase Error, Y	f = 3.58 MHz		0.1		Degrees
Harmonic Distortion	X or Y = 10 dBm, Second and Third Harmonic				
	Fund = 10 MHz		–70		dB
	Fund = 50 MHz		–40		dB
Settling Time, X or Y	To 0.1%, W = 2 V p-p		20		ns
SUMMING INPUT (Z)					
Gain	From Z to W, f ≤ 10 MHz	0.990	0.995		
–3 dB Small-Signal Bandwidth			250		MHz
Differential Input Resistance			60		kΩ
Single Sided Capacitance			2		pF
Maximum Gain	X, Y to W, Z Shorted to W, f = 1 kHz		50		dB
Bias Current			50		µA
OUTPUT CHARACTERISTICS					
Voltage Swing		±2.2	±2.5		V
vs. Temperature	T_{MIN} to T_{MAX}[1]	±2.0			V
Voltage Noise Spectral Density	X = Y = 0, f < 10 MHz		50		nV/√Hz
Offset Voltage			±25	**±75**	mV
vs. Temperature[2]	T_{MIN} to T_{MAX}[1]			±10	mV
Short Circuit Current			75		mA
Scale Factor Error			±5	**±8**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±9	% FS
Linearity (Relative Error)[3]			±0.5	**±1.0**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±1.25	% FS

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Supply Voltage					
For Specified Performance		±4.5	±5	±5.5	V
Quiescent Supply Current			16	**25**	mA
vs. Temperature	T_{MIN} to T_{MAX}[1]			26	mA
PSRR at Output vs. VP	+4.5 V to +5.5 V			**0.5**	%/V
PSRR at Output vs. VN	–4.5 V to –5.5 V			0.5	%/V

NOTES
[1]T_{MIN} = –40°C, T_{MAX} = 85°C.
[2]Normalized to zero at 25°C.
[3]Linearity is defined as residual error after compensating for input offset, output voltage offset, and scale factor errors.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

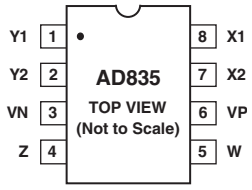
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±6 V
Internal Power Dissipation[2] . . . . . 300 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . 300°C
ESD Rating . . . . . 1500 V

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Lead PDIP (N): θ_{JC} = 35°C/W; θ_{JA} = 90°C/W
8-Lead SOIC (R): θ_{JC} = 45°C/W; θ_{JA} = 115°C/W.

PIN CONNECTIONS

8-Lead PDIP (N)
8-Lead SOIC (R)



ORDERING GUIDE

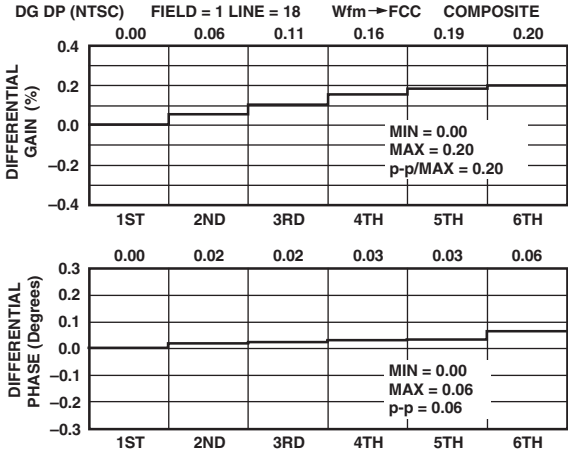
Model	Temperature Range	Package Options[1]
AD835AN	–40°C to +85°C	N-8
AD835AR	–40°C to +85°C	R-8
AD835AR-REEL	–40°C to +85°C	R-8
AD835AR-REEL7	–40°C to +85°C	R-8
AD835ARZ[2]	–40°C to +85°C	R-8

[1]N = PDIP; R = Small Outline IC Plastic Package (SOIC).
[2]The Z stands for a lead-free product.

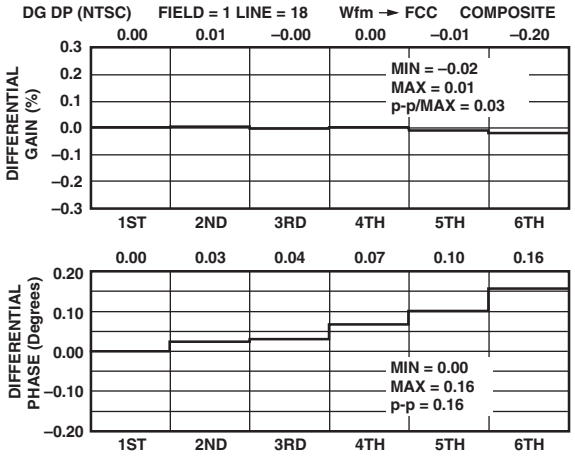
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD835 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

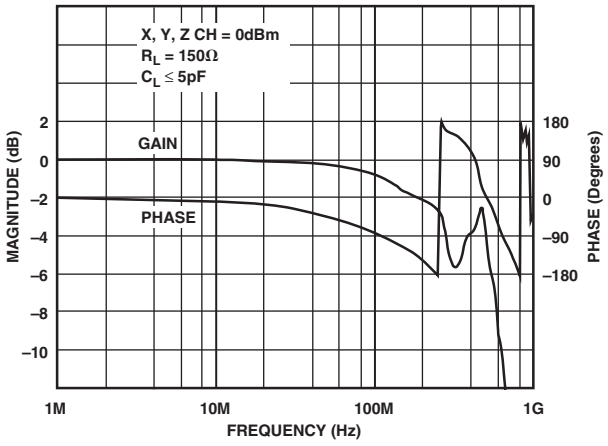
AD835–Typical Performance Characteristics



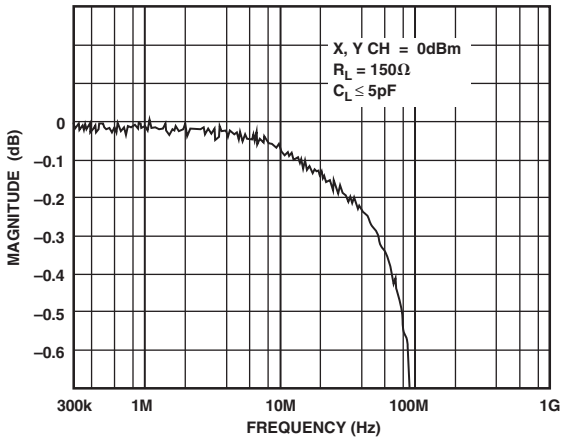
TPC 1. Typical Composite Output Differential Gain and Phase, NTSC for X Channel; f = 3.58 MHz, R_L = 150 Ω



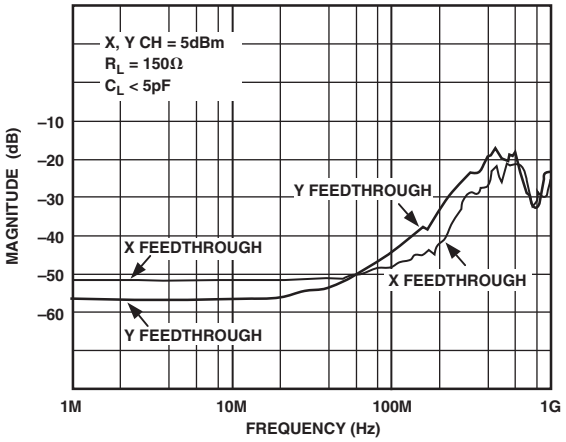
TPC 2. Typical Composite Output Differential Gain and Phase, NTSC for Y Channel; f = 3.58 MHz, R_L = 150 Ω



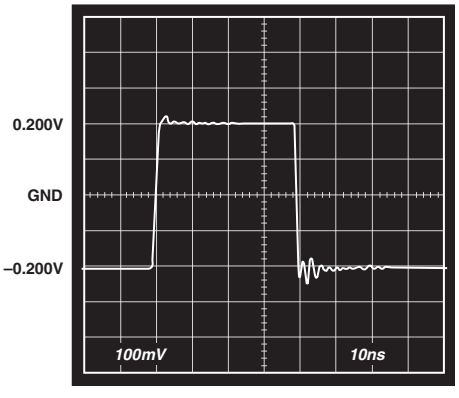
TPC 3. Gain and Phase vs. Frequency of X, Y, Z Inputs



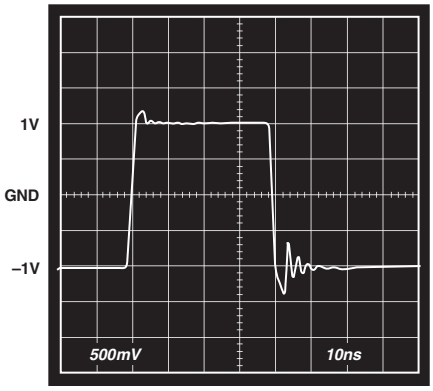
TPC 4. Gain Flatness to 0.1 dB



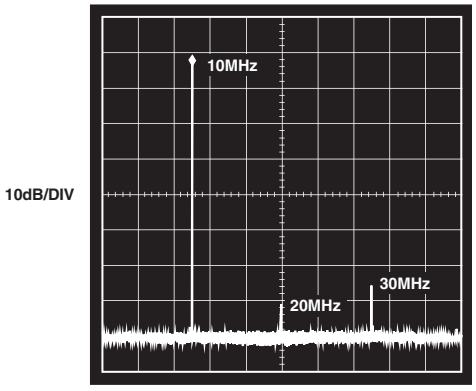
TPC 5. X and Y Feedthrough vs. Frequency



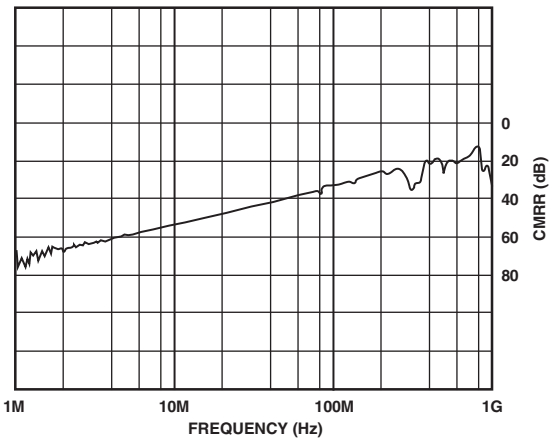
TPC 6. Small Signal Pulse Response at W Output, R_L = 150 Ω, $C_L \leq$ 5 pF, X Channel = ±0.2 V, Y Channel = ±1.0 V



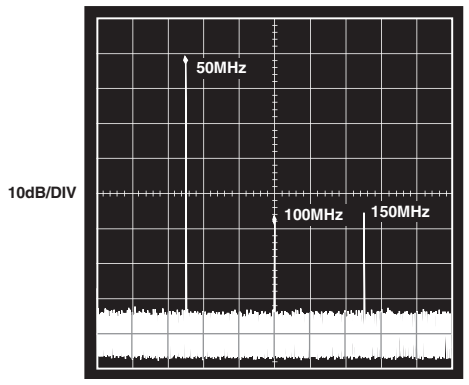
TPC 7. Large Signal Pulse Response at W Output, R_L = 150 Ω, $C_L \leq$ 5 pF, X Channel = ±1.0 V, Y Channel = ±1.0 V



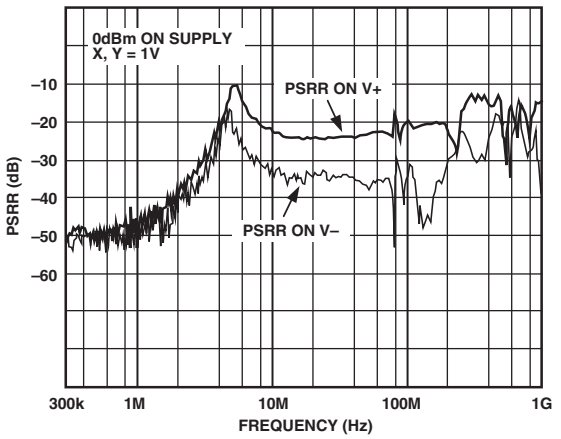
TPC 10. Harmonic Distortion at 10 MHz; 10 dBm Input to X or Y Channels, R_L = 150 Ω, $C_L = \leq$ 5 pF



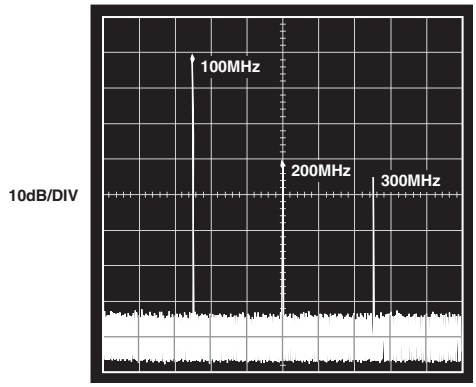
TPC 8. CMRR vs. Frequency for X or Y Channel, R_L = 150 Ω, $C_L \leq$ 5 pF



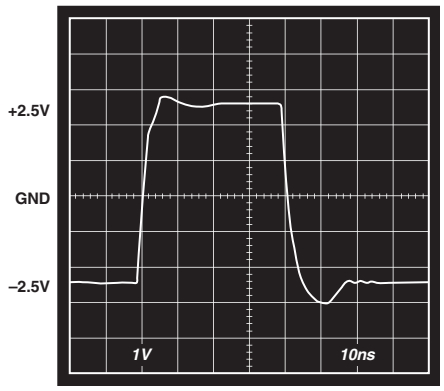
TPC 11. Harmonic Distortion at 50 MHz, 10 dBm Input to X or Y Channel, R_L = 150 Ω, $C_L \leq$ 5 pF



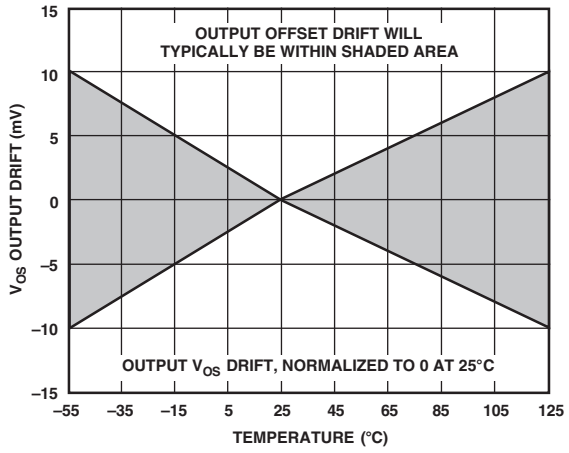
TPC 9. PSRR vs. Frequency for V+ and V– Supply



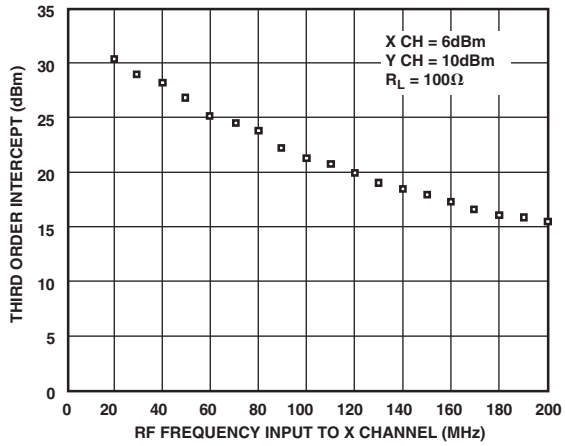
TPC 12. Harmonic Distortion at 100 MHz, 10 dBm Input to X or Y Channel, R_L = 150 Ω, $C_L \leq$ 5 pF



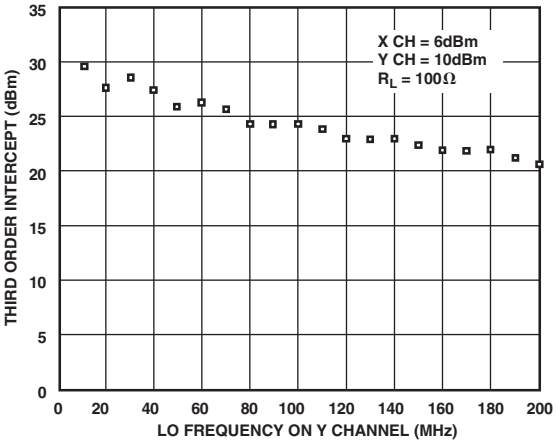
TPC 13. Maximum Output Voltage Swing, R_L = 50 Ω, $C_L \leq$ 5 pF



TPC 14. V_{OS} Output Drift vs. Temperature



TPC 15. Fixed LO on Y Channel vs. RF Frequency Input to X Channel



TPC 16. Fixed IF vs. LO Frequency on Y Channel

PRODUCT DESCRIPTION

The AD835 is a four-quadrant voltage output analog multiplier, fabricated on an advanced dielectrically isolated complementary bipolar process. In its basic mode, it provides the linear product of its X and Y voltage inputs. In this mode, the –3 dB output voltage bandwidth is 250 MHz (a small signal rise time of 1 ns). Full scale (–1 V to +1 V) rise to fall times are 2.5 ns (with the standard R_L of 150 Ω) and the settling time to 0.1% under the same conditions is typically 20 ns.

As in earlier multipliers from Analog Devices, a unique summing feature is provided at the Z input. As well as providing independent ground references for input and output and enhanced versatility, this feature allows the AD835 to operate with voltage gain. Its X-, Y-, and Z-input voltages are all nominally ±1 V FS, with an overrange of at least 20%. The inputs are fully differential at high impedance (100 kΩ‖2 pF) and provide a 70 dB CMRR (f ≤ 1 MHz).

The low impedance output is capable of driving loads as small as 25 Ω. The peak output can be as large as ±2.2 V minimum for R_L = 150 Ω, or ±2.0 V minimum into R_L = 50 Ω. The AD835 has much lower noise than the AD534 or AD734, making it attractive in low level signal-processing applications, for example, as a wideband gain-control element or modulator.

Basic Theory

The multiplier is based on a classic form, having a translinear core, supported by three (X, Y, Z) linearized voltage-to-current converters, and the load driving output amplifier. The scaling voltage (the denominator U in the equations below) is provided by a band gap reference of novel design, optimized for ultralow noise. Figure 1 shows the functional block diagram.

In general terms, the AD835 provides the function

$$W = \frac{(X1 - X2)(Y1 - Y2)}{U} + Z \tag{1}$$

where the variables *W*, *U*, *X*, *Y*, and *Z* are all voltages. Connected as a simple multiplier, with $X = X1 - X2$, $Y = Y1 - Y2$, and $Z = 0$ and with a scale factor adjustment (see Figure 1), which sets $U = 1$ V, the output can be expressed as

$$W = XY \tag{2}$$

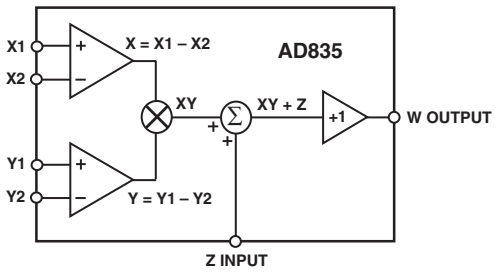


Figure 1. Functional Block Diagram

Simplified representations of this sort, where all signals are presumed to be expressed in V, are used throughout this data sheet to avoid the needless use of less-intuitive subscripted variables (such as V_{X1}). We can view all variables as being *normalized to* 1 V. For example, the input X can either be stated as being in the range –1 V to +1 V or simply –1 to +1. The latter representation will be found to facilitate the development of new functions using the AD835. The explicit inclusion of the denominator, U, is also less helpful, as in the case of the AD835, if it is not an electrical input variable.

Scaling Adjustment

The basic value of *U* in Equation 1 is nominally 1.05 V. Figure 2, which shows the basic multiplier connections, also shows how the effective value of *U* can be adjusted to have any lower voltage (usually 1 V) through the use of a resistive-divider between *W* (Pin 5) and *Z* (Pin 4). Using the general resistor values shown, we can rewrite Equation 1 as

$$W = \frac{XY}{U} + kW + (1 - k)Z' \tag{3}$$

where *Z'* is distinguished from the signal *Z* at Pin 4. It follows that

$$W = \frac{XY}{(1 - k)U} + Z' \tag{4}$$

In this way, we can modify the effective value of *U* to

$$U' = (1 - k)U \tag{5}$$

without altering the scaling of the *Z'* input. (This is to be expected since the only "ground reference" for the output is through the *Z'* input.)

Thus, to set *U'* to 1 V, remembering that the basic value of *U* is 1.05 V, we need to choose R1 to have a nominal value of 20 times R2. The values shown here allow *U* to be adjusted through the nominal range 0.95 V to 1.05 V. That is, R2 provides a 5% gain adjustment.

Note that in many applications, the exact gain of the multiplier may not be very important; in which case, this network may be omitted entirely, or R2 fixed at 100 Ω.

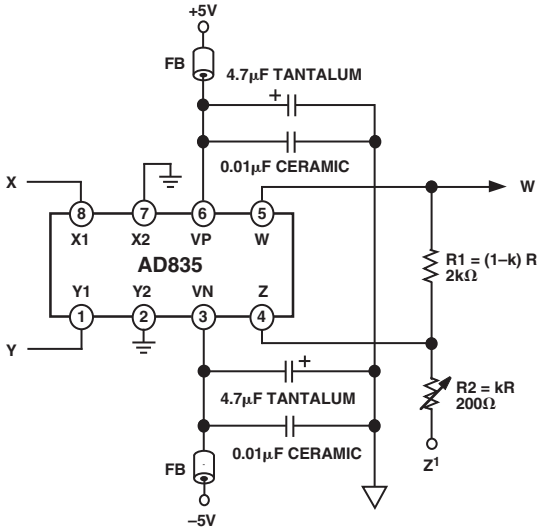


Figure 2. Multiplier Connections

APPLICATIONS

The AD835 is easy to use and versatile. The capability for adding another signal to the output at the Z input is frequently valuable. Three applications of this feature are presented here: a wideband voltage controlled amplifier, an amplitude modulator, and a frequency doubler. Of course, the AD835 may also be used as a square law detector (with its X- and Y-inputs connected in parallel). In this mode, it is useful at input frequencies to well over 250 MHz, since that is the bandwidth limitation of the *output amplifier* only.

Multiplier Connections

Figure 2 shows the basic connections for multiplication. The inputs will often be single-sided, in which case the X2 and Y2 inputs will normally be grounded. Note that by assigning Pins 7 and 2, respectively, to these (inverting) inputs, an extra measure of isolation between inputs and output is provided. The X and Y inputs may, of course, be reversed to achieve some desired overall sign with inputs of a particular polarity, or they may be driven fully differentially.

Power supply decoupling and careful board layout are always important in applying wideband circuits. The decoupling recommendations shown in Figure 2 should be followed closely. In remaining figures in this data sheet, these power supply decoupling components have been omitted for clarity but should be used wherever optimal performance with high speed inputs is required. However, they may be omitted if the full high frequency capabilities of the AD835 are not being exploited.

Wideband Voltage Controlled Amplifier

Figure 3 shows the AD835 configured to provide a gain of nominally 0 dB to 12 dB. (In fact, the control range extends from well under –12 dB to about +14 dB.) R1 and R2 set the gain to be nominally ×4. The attendant bandwidth reduction that comes with this increased gain can be partially offset by the addition of the peaking capacitor C1. Although this circuit shows the use of dual supplies, the AD835 can operate from a single 9 V supply with a slight revision.

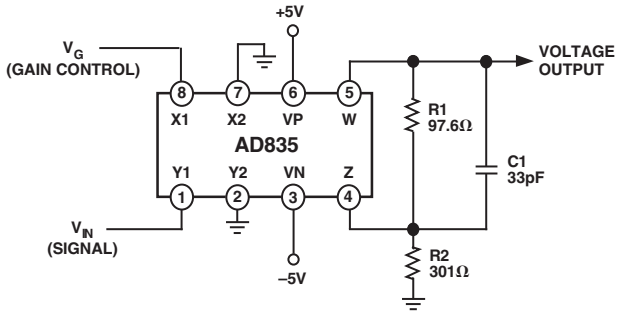


Figure 3. Voltage Controlled 50 MHz Amplifier Using the AD835

The ac response of this amplifier for gains of 0 dB (V_G = 0.25 V), 6 dB (V_G = 0.5 V), and 12 dB (V_G = 1 V) is shown in Figure 4. In this application, the resistor values have been slightly adjusted to reflect the nominal value of U = 1.05 V. The overall sign of the gain may be controlled by the sign of V_G.

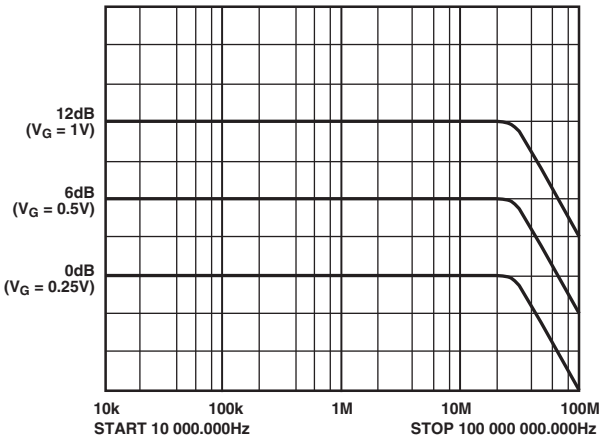


Figure 4. AC Response of VCA

Amplitude Modulator

Figure 5 shows a simple modulator. The carrier is applied to the Y input and the Z input, while the modulating signal is applied to the X input. For zero modulation, there is no product term so the carrier input is simply replicated at unity gain by the voltage follower action from the Z input. At X = 1 V, the RF output is doubled, while for X = –1 V, it is fully suppressed. That is, an X input of approximately ±1 V (actually ±U or about 1.05 V) corresponds to a modulation index of 100%. Carrier and modulation frequencies can be up to 300 MHz, somewhat beyond the nominal –3 dB bandwidth.

Of course, a suppressed carrier modulator can be implemented by omitting the feedforward to the Z input, grounding that pin instead.

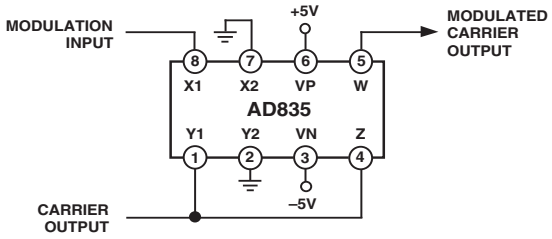


Figure 5. Simple Amplitude Modulator Using the AD835

Squaring and Frequency Doubling

Amplitude domain squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of E^2/U. The input may have either polarity, but the output in this case will always be positive. The output polarity may be reversed by interchanging either the X or Y inputs.

When the input is a sine wave $E \sin \omega t$, a signal squarer behaves as a frequency doubler, since

$$\frac{(E\sin\omega t)^2}{U} = \frac{E^2}{2U}(1-\cos 2\omega t) \qquad (6)$$

While useful, Equation 6 shows a dc term at the output, which will vary strongly with the amplitude of the input, *E*.

Figure 6 shows a frequency doubler, which overcomes this limitation and provides a relatively constant output over a moderately wide frequency range, determined by the time-constant C1 and R1. The voltage applied to the X and Y inputs are exactly in quadrature at a frequency f = 1/2 πC1R1 and their amplitudes are equal. At higher frequencies, the X input becomes smaller while the Y input increases in amplitude; the opposite happens at lower frequencies. The result is a double frequency output centered on ground whose amplitude of 1 V for a 1 V input varies by only 0.5% over a frequency range of ±10%. Because there is no squared dc component at the output, sudden changes in the input amplitude do not cause a bounce in the dc level.

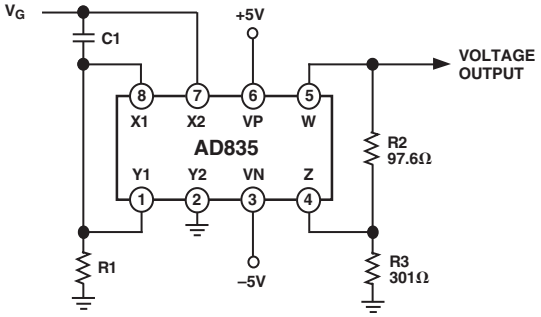


Figure 6. Broadband "Zero-Bounce" Frequency Doubler

This circuit is based on the identity

$$\cos\theta \sin\theta = \frac{1}{2}\sin 2\theta \tag{7}$$

At ω_O = 1/C1R1, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$, while the Y input lags the input signal by 45° and is also attenuated by $\sqrt{2}$. Since the X and Y inputs are 90° out of phase, the response of the circuit will be

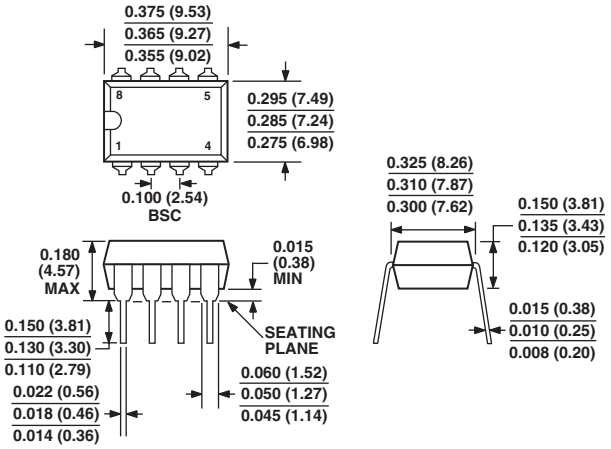
$$W = \frac{1}{U}\frac{E}{\sqrt{2}}\left(\sin\omega t - 45°\right)\frac{E}{\sqrt{2}}\left(\sin\omega t + 45°\right) = \frac{E^2}{2U}\left(\sin 2\omega t\right) \tag{8}$$

which has no dc component, R2 and R3 are included to restore the output to 1 V for an input amplitude of 1 V (the same gain adjustment as mentioned earlier). Because the voltage across the capacitor (C1) decreases with frequency, while that across the resistor (R1) increases, the amplitude of the output varies only slightly with frequency. In fact, it is only 0.5% below its full value (at its center frequency ω_O = 1/C1R1) at 90% and 110% of this frequency.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

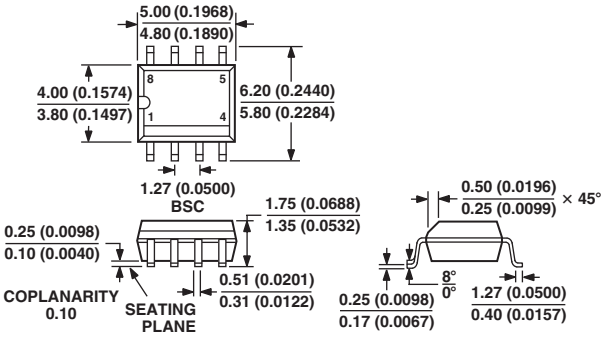


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
(R-8)

Dimensions shown in millimeters and (inches)



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Revision History

Location	Page
6/03—Data Sheet changed from REV. A to REV. B.	
Updated Format	Universal
Updated OUTLINE DIMENSIONS	10