BLUE TECHNIX

Hardware User Manual

TCM-BF537 V1.1

Including BGA and Border Pad Versions

PRELIMINARY

www.tinyboards.com

Maximum Power at Minimum Size

Contact

Bluetechnix Mechatronische Systeme GmbH

Waidhausenstr. 3/19
A-1140 Vienna
AUSTRIA/EUROPE
office@bluetechnix.at
http://www.bluetechnix.com

Document No.: 100-1225-1.1

Version 5

Date: 2007-04-17

Table of Contents

Edition 2007-02

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.
Terms of delivery and rights of technical change reserved.

We hereby disclaim any warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Bluetechnix makes and you receive no warranties or conditions, express, implied, statutory or in any communication with you. Bluetechnix specifically disclaims any implied warranty of merchantability or fitness for a particular purpose.

Bluetechnix takes no liability for any damages and errors causing of the usage of this board. The user of this board is responsible by himself for the functionality of his application. He is allowed to use the board only if he has the qualification. More information is found in the General Terms and Conditions (AGB).

Information
For further information on technology, delivery terms and conditions and prices please contact Bluetechnix (http://www.bluetechnix.com).

Warnings
Due to technical requirements components may contain dangerous substances.

The Core Boards and Development systems contain ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused core boards and development boards should be stored in the protective shipping package.

BLACKFIN Products

Core Modules:

CM-BF533:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF533 processor; up to 600MHz, 32MB RAM, 2MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537E:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated TP10/100 Ethernet physical transceiver, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537U:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated USB 2.0 Device, 120 pin expansion connector and a size of 36.5x31.5mm
TCM-BF537:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 500MHz, 32MB RAM, 8MB Flash, 28x28mm, 120 pin expansion connector, Ball Grid Array or Border Pads for reflow soldering, industrial temperature range -40°C to +85°C.
CM-BF561:	Blackfin Processor Module powered by Analog Devices dual core ADSP-BF561 processor; up to 2x 600MHz, 64MB RAM, 8MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF527:	From Q3 '07 a new Blackfin Processor Module powered by Analog Devices single core ADSP-BF527 processor will be available; key features are USB OTG 2.0 and Ethernet. 2x120pin expansion connectors are backwards compatible to other Core Modules.
CM-BF548:	From Q3 '07 a new Blackfin Processor Module powered by Analog Devices single core ADSP-BF548 processor will be available; key features are 64MB DDR SD-RAM 2x100pin expansion connectors.

Development Boards:

EVAL-BF5xx:	Low cost Blackfin processor Evaluation Board with one socket for any Bluetechnix Blackfin Core Module. Additional periphery is available, such as a SD-Card.
DEV-BF5xxDA-Lite:	Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including a USB Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including VDSP++ Evaluation Software License.

DEV-BF5xx-FPGA: Backfin Development Board with two sockets for any combination of Blackfin Core Modules. Additional periphery is available, such as SD-Card, Ethernet, USB host, multi-port JTAG including a USB based Debug Agent, connector for a LCD-TFT Display and connector for a digital camera system. A large on-board SPARTAN-3 FPGA and Soft IPs make this board the most flexible Blackfin development platforms ever developed.
Available Q2 2007

EXT-Boards: The following Extender Boards are available: EXT-BF5xx-Audio, EXT-BF5xx-Video, EXT-BF5xx-Camera, EXT-BF5xx-Exp, *EXT-BF5xx-LVDS, *EXT-BF5xx-ETH-USB, *EXT-BF5xx-AD/DA. Additional boards based on customer request
*Available Q2 2007

Software Support:

BLACKSheep: The BLACKSheep VDK is a multithreaded framework for the Analog Devices Blackfin processor family that includes driver support for a variety of hardware extensions. It is based on the real-time VDK kernel included within the VDSP++ development environment.

LabVIEW: LabVIEW embedded support for the CM-BF537E, CM-BF537U and TCM-BF537 Core Modules based on the BLACKSheep VDK driver Framework.

uClinux: All the Core Modules are supported by uClinux. The required boot loader and uClinux can be downloaded at http://blackfin.uClinux.org.

BLACKFIN Design Service

Based on over three years Blackfin experience Bluetechnix offers development assistance as well as custom design services and software development.

1 Introduction

The TCM-BF537 is a chip size Core Module designed for industrial temperature range and volume production. It combines power supply, RAM and FLASH into a module as small as a chip package. Different connector options (BGA, Boarder Pads (BP) and Connectors) offers solution for all possible requirements.

1.1 Overview

The Core Module TCM-BF537 consists of the following components shown in Figure 1-1.

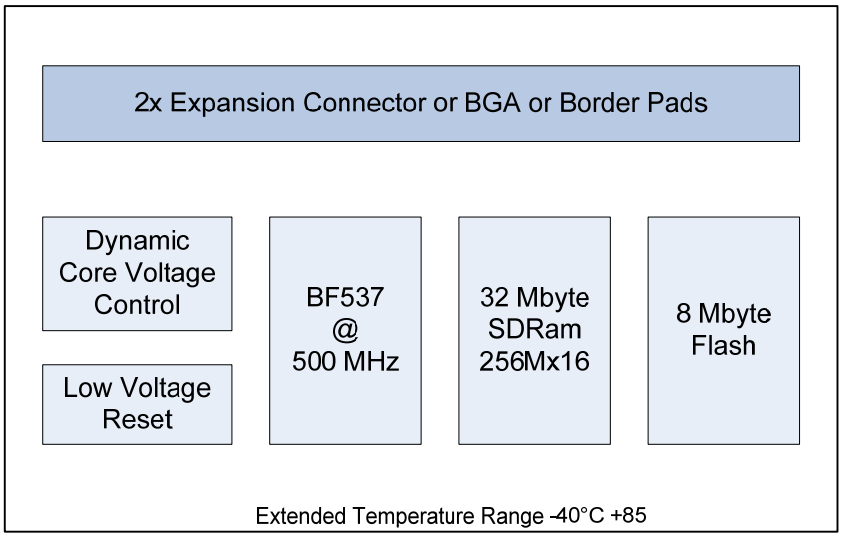


Figure 1-1: Main Components of the Core Module

- **Analog Devices Blackfin Processor BF537**
  - ADSP-BF537BBCZ-5A, 500MHz (-40°-85°C)
- **32 MB SDRAM**
  - SDRAM Clock up to 133MHz
  - MT48LC16M16A2BG-7 (16Mx16, 256Mbit at 3.3 V)
- **8 MB of Addressable Flash**
  - PF48F2000P0ZBQ0S (32Mx16, at 3.3V; all 8MByte addressable, bottom boot)
  - Additional flash memory upon request: It can be connected through the expansion board as parallel flash using asynchronous chip select lines or as a SPI flash.
- **Low Voltage Reset Circuit**
  - Resets module if power supply goes below 2.93V.

- **Dynamic Core Voltage Control**
    - Allows to adjust core voltage by setting software registers at the Blackfin processor
    - Core voltage range: 0.8 – 1.32V
- **Peripherals available on all Core Module versions**
    - Power Supply
    - SPORT 0
    - JTAG
    - UART0/Uart1
    - CAN
    - TWI (I2C compatible)
    - SPI (Serial Port Interface)
    - PPI (Parallel Port Interface)
    - Boot Mode Pins
    - GPIO's
- **Peripherals available on the Connector and BGA version only.**
    - Data Bus
    - Address Bus
    - Further GPIO's
    - Memory Control Signals

1.2 Versions

TCM-BF537: Connector Version 2x60 connector pins

TCM-BF537BGA: 169 BGAs 1.5 mm pitch for volume production

TCM-BF537Boarder: 76 Boarder Pads, no Data- and Address bus on boarder pads

1.3 Benefits

- The TCM-BF537 is very compact and measures only 28x28mm (27.4x27.4 mm in Rev. 1.0)
- Reduces development costs, faster time to market.
- Allows integration on a two layer baseboard.
- Very cost effective for small and medium volumes

1.4 Typical Applications

- Generic high performance signal processor module
- Industrial Automation
- Robotics

2 Specification

2.1 Functional Specification

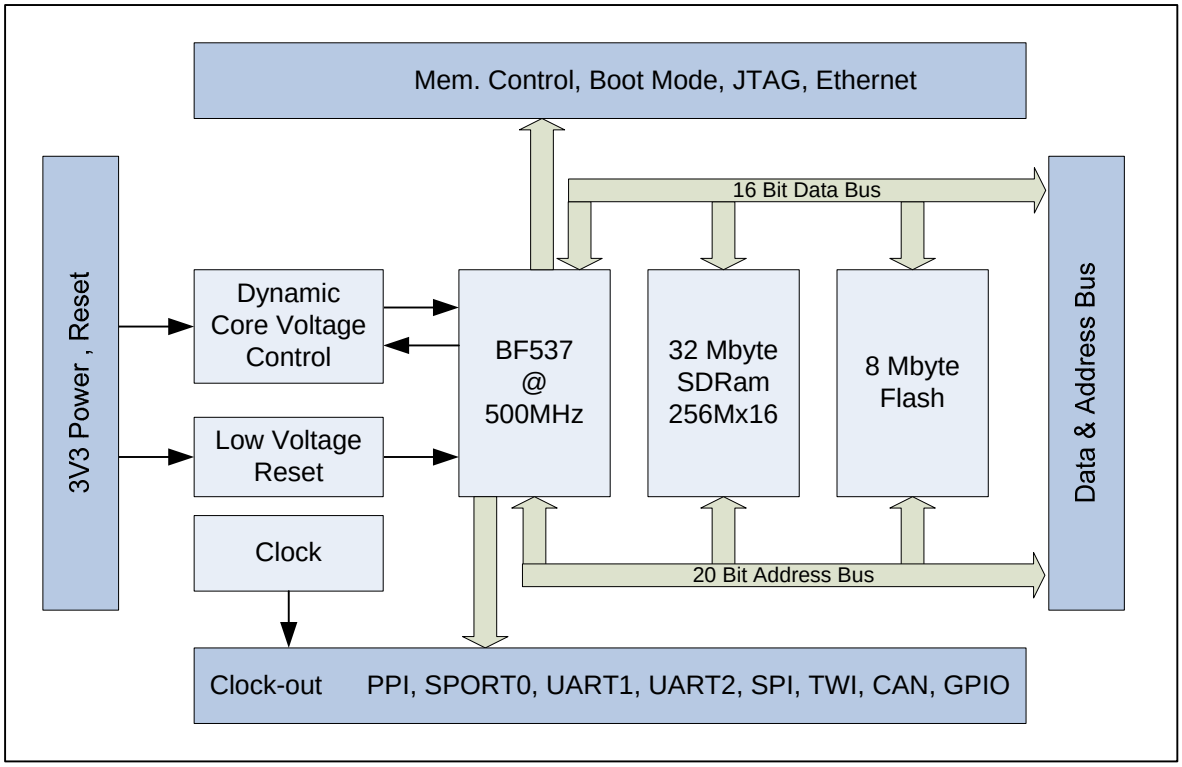


Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the TCM-BF537 module. Beside the SDRAM and a few other control pins, the TCM-BF537 has most pins of the Blackfin processor at its two 60 pin connectors, or its BGA, or its Boarder Pads.

Dynamic voltage control allows reducing power consumption to a minimum adjusting the core voltage and the clock frequency dynamically in accordance to the required processing power.
A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V for at least 140ms.

2.2 Boot Mode

By default the boot mode = 000 (BMODE2 = Low, BMODE1 = Low, BMODE0=Low). All BMODE pins have on board pull down resistors.

Boot-settings for CM-BF534 and CM-BF537

Switch Settings BMODE2,BMODE1,BMODE0	Bootmode	Description
000	0	Execute from16Bit ext. mem. Bypass ROM

001	1	Boot from 8Bit or 16Bit EEPROM/Flash
010	2	Reserved
011	3	Boot from serial SPI Memory
100	4	Boot from SPI Host (slave mode)
101	5	Boot from serial TWI memory
110	6	Boot from TWI host
111	7	Boot from UART host (slave mode)

Table 2-1: Bootmode CM-BF534/537

Connect BMODE0 to Vcc and leave BMODE1, BMODE2 pins open for Boot Mode 001 equals to 8 or 16 bit PROM/FLASH boot mode. This is the default boot mode of the Blacksheep software.

2.3 Memory MAP

Memory Type	Start Address	End Address	Size	Comment
FLASH PF4 Flag **Low** PF5 Flag **Low**	0x20000000	0x200FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH PF4 Flag **High** PF5Flag **Low**	0x20000000	0x200FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH PF4 Flag **Low** PF5 Flag **High**	0x20000000	0x200FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH PF4 Flag **High** PF5 Flag **High**	0x20000000	0x200FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
SD-RAM	0x00000000	0x01FFFFFF	32MB	16Bit Bus, Micron MT48LC16M16A2FG

Table 2-2: Memory Map

2.4 Electrical Specification

2.4.1 Supply Voltage

- 3.3V DC +/-10%

2.4.2 Supply Voltage Ripple

- 100mV peak to peak 0-20 MHz

2.4.3 Processor Oscillator Frequency

- 25MHz

2.4.4 Real Time Clock Crystal

- 32.768kHz

2.4.5 Supply Current

- Maximum current: 200mA at 3.3V
- Typical operating conditions at 25°C environment temperature:
    - Processor running at 500MHz, Core Voltage 1.2V, SDRAM 50% bandwidth utilization at 125MHz; 150mA at 3.3V
    - Processor running at 250MHz, Core Voltage 0.85V SDRAM 50% bandwidth utilization at 83,3MHz; ; Ethernet Idle: 85mA at 3.3V
    - Processor running at 600MHz, Core Voltage 1.2V, SDRAM 50% bandwidth utilization at 120MHz, 160mA at 3.3V

2.5 Environmental Specification

2.5.1 Temperature

- Operating at full 500MHz:: -40 to + 85° C

2.5.2 Humidity

Operating: 10% to 90% (non condensing)

3 TCM-BF537 (Connector Version)

3.1 Mechanical Outline

Figure 3-1 shows the top view of the Core Module (All dimensions are given in millimeters!)

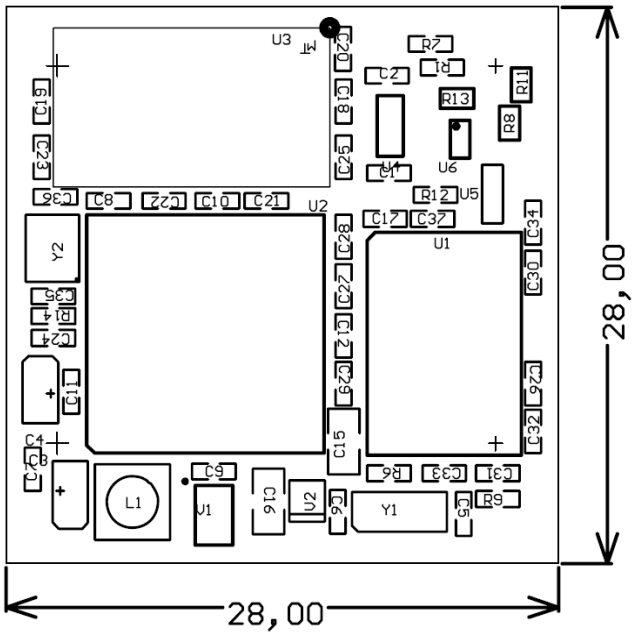


Figure 3-1: Mechanical Outline (TOP VIEW)

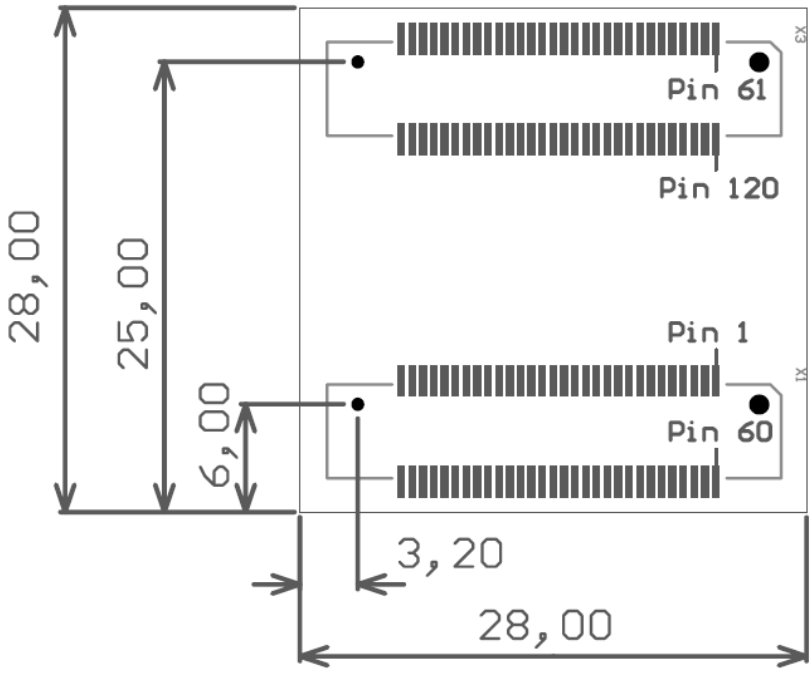


Figure 3-2: Mechanical Outline (BOTTOM VIEW)

Figure 3-3 shows a side view of the Core Module with mounted connectors.

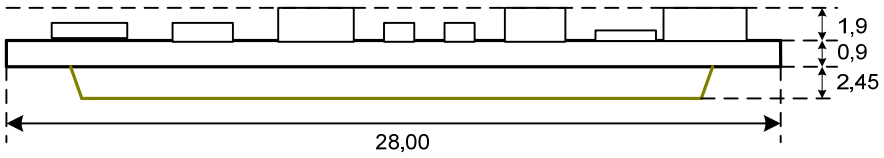


Figure 3-3: Side View with Connectors mounted

The total minimum mounting height including receptacle at the motherboard is 5.8mm.

The mechanical outline in Figure 3-4 shows the footprint for the connectors on your base board (TOP VIEW).

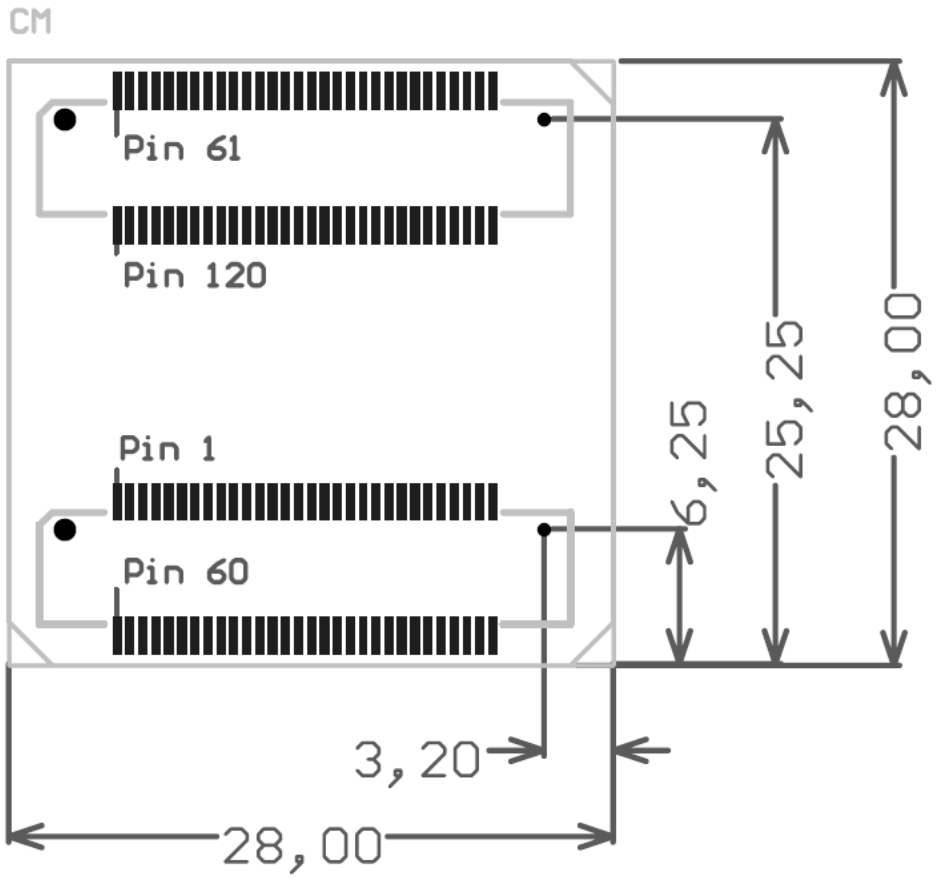


Figure 3-4: Connector Footprint for Base Board (TOP VIEW)

3.2 Connector Footprint of Baseboard

For the Connector version (2x Hirose 0.6mm pitch) the footprint for the base board looks like shown in Figure 3-4.

For the baseboard the following connectors have to be used.

Part Baseboard	**Manufacturer**	**Manufacturer Part No**.
P1,P2	Hirose	FX8-60S-SV

Table 3-1: Baseboard connector types

The Connectors on the TCM-BF537 are of the following type:

Part	**Manufacturer**	**Manufacturer Part No.**
P1,P2	Hirose 3mm height	FX8-60P-SV

Table 3-2: Core Module connector types

3.3 Schematic Symbol of Connector Version

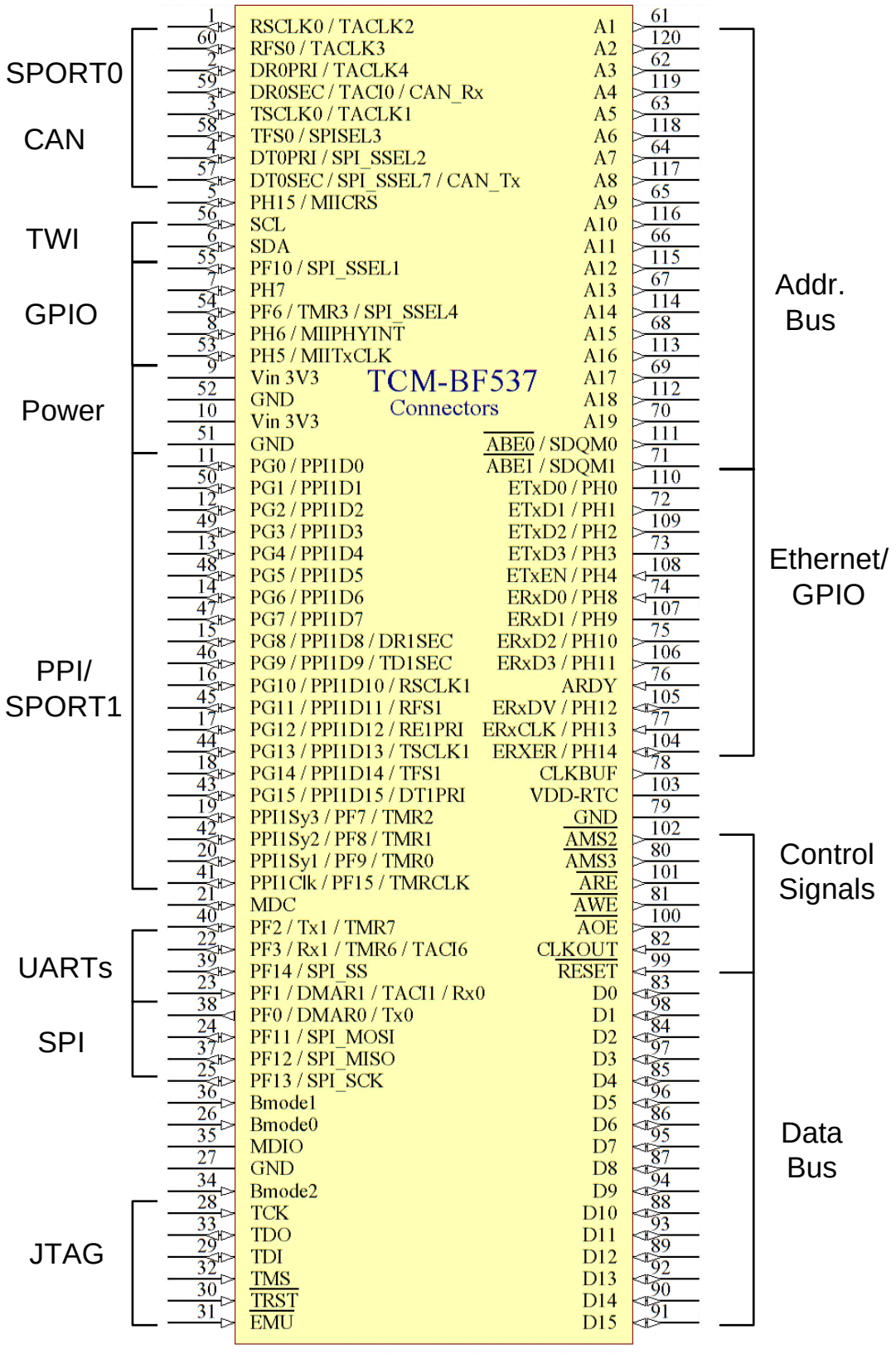


Figure 3-5: Schematics Symbol of Connector Version of the TCM-BF537

3.4 Connectors PIN Assignment

3.4.1 Connector P1 – (1-60)

Pin No.	Signal	Signal type	Pin No.	Signal	Signal type
1	RSCLK0/TACLK2	I/O	2	DR0PRI/ TACLK4	I
3	TSCLK0/TACLK1	I/O	4	DT0PRI/SPI_SSEL2	O
5	PH15 / MIICRS	I/O	6	SDA	I/O
7	PH7 / COL	I/O	8	PH6/MIIPHYINT	I/O
9	Vin 3.3V	PWR	10	Vin 3.3V	PWR
11	PG0/PPI1D0	I/O	12	PG2/PPI1D2	I/O
13	PG4/PPI1D4	I/O	14	PG6/PPI1D6	I/O
15	PG8/PPI1D8/DR1SEC	I/O	16	PG10/PPI1D10/RSCLK1	I/O
17	PG12/PPI1D12/RE1PRI	I/O	18	PG14/PPI1D14/TFS1	I/O
19	PPI1SY3/PF7/TMR2	I/O	20	PPI1SY1/PF8/TMR0	I/O
21	MDC	I/O	22	PF3/Rx1/TMR6/TACI6	I/O
23	PF1/DMAR1/TACI1/Rx0	I/O	24	PF11/SPI_MOSI	I/O
25	PF13/SPI_SCK	I/O	26	BMODE0	I
27	GND	PWR	28	TCK	I
29	TDI	I	30	nTRST	I
31	nEMU	O	32	TMS	I
33	TDO	O	34	BMODE2	I
35	MDIO	I/O	36	BMODE1	I
37	PF12/SPI_MISO	I/O	38	PF0/DMAR0/Tx0	I/O
39	PF14/SPI_SS	I/O	40	PF2/Tx1/TMR7	I/O
41	PPI1Clk/PF15/TMRCLK	I/O	42	PPI1Sy2/PF8/TMR1	I/O
43	PG15/PPI1D15/DT1PRI	I/O	44	PG13/PPI1D13/TSCLK1	I/O
45	PG11/PPI1D11/RFS1	I/O	46	PG9/PPI1D9/TD1SEC	I/O
47	PG7/PPI1D7	I/O	48	PG5/PPI1D5	I/O
49	PG3/PPI1D3	I/O	50	PG1/PPI1D1	I/O
51	GND	PWR	52	GND	PWR
53	PH5/MIITxCLK	I/O	54	PF6/TMR3/SPI_SSEL4	I/O
55	PF10/SPI_SSEL1	I	56	SCL	I/O
57	DT0SEC/CANTX/SPI_SSEL7	O	58	TFS0	I/O
59	DR0SEC/TACI0/CANRX	I	60	RFS0/TACLK3	I/O

Table 3-3: Connector P1 pin assignment

NOTE: The processor pins PF4 and PF5 are used for flash addressing on the Core Module. They are not accessible at the connectors.

3.4.2 Connector P2 – (61-120)

Pin No.	Signal	Signal type	Pin No.	Signal	Signal type
61	A1	O	62	A3	O
63	A5	O	64	A7	O
65	A9	O	66	A11	O
67	A13	O	68	A15	O
69	A17	O	70	A19	O
71	nABE1 / SDQM1	O	72	PH1/ETxD1	I/O
73	PH3/ETxD3	I/O	74	PH8/ERxD0	I/O
75	PH10/ERxD2	I/O	76	ADRY	I
77	PH13/ERxCLK	I/O	78	CLKBUF	O
79	GND	PWR	80	nAMS3	O
81	nAWE	O	82	CLKOUT (SCLK)	I
83	D0	I/O	84	D2	I/O
85	D4	I/O	86	D6	I/O
87	D8	I/O	88	D10	I/O
89	D12	I/O	90	D14	I/O
91	D15	I/O	92	D13	I/O
93	D11	I/O	94	D9	I/O
95	D7	I/O	96	D5	I/O
97	D3	I/O	98	D1	I/O
99	nReset	I	100	nAOE	O
101	nARE	O	102	nAMS2	O
103	VDD-RTC	PWR	104	PH14/ERXER	I/O
105	PH12/ERxDV	I/O	106	PH11/ERxD3	PWR
107	PH9/ERxD1	I/O	108	PH4/ETxEN	I/O
109	PH2/ETxD2	I/O	110	PH0/ETxD0	I/O
111	nABE0 / SDQM0	O	112	A18	O
113	A16	O	114	A14	O
115	A12	O	116	A10	O
117	A8	O	118	A6	O
119	A4	O	120	A2	O

Table 3-4: Connector P2 pin assignment

4 TCM-BF537BP (Boarder Pad Version)

4.1 Mechanical Outline

Figure 4-1 shows the Top view of the Core Module (All dimensions are given in millimeters!)

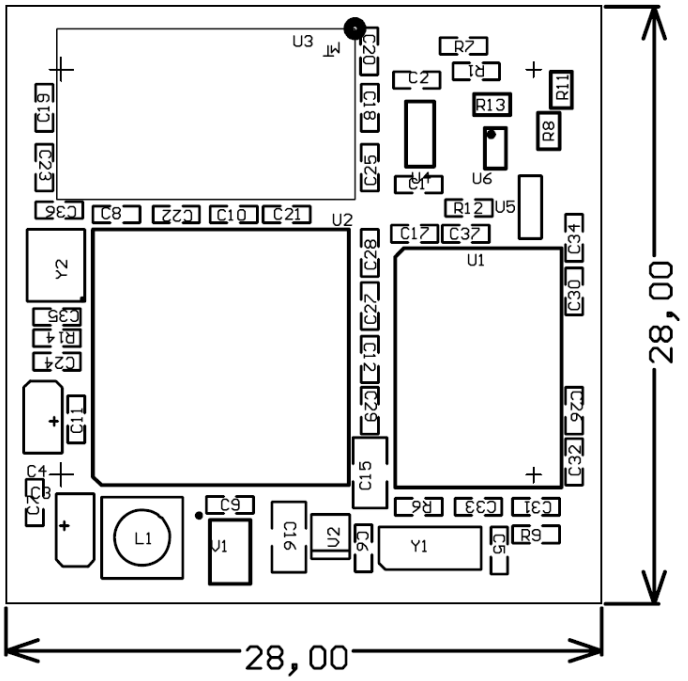


Figure 4-1: Mechanical Outline (TOP VIEW)

Figure 4-2 shows a side view of the Core Module with boarder pads.

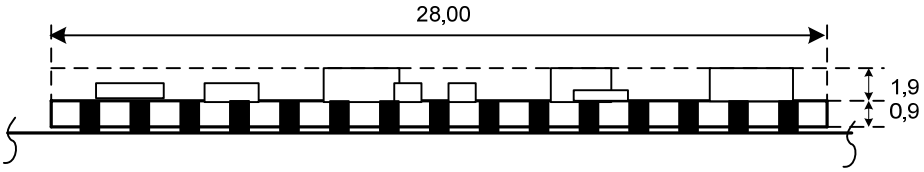
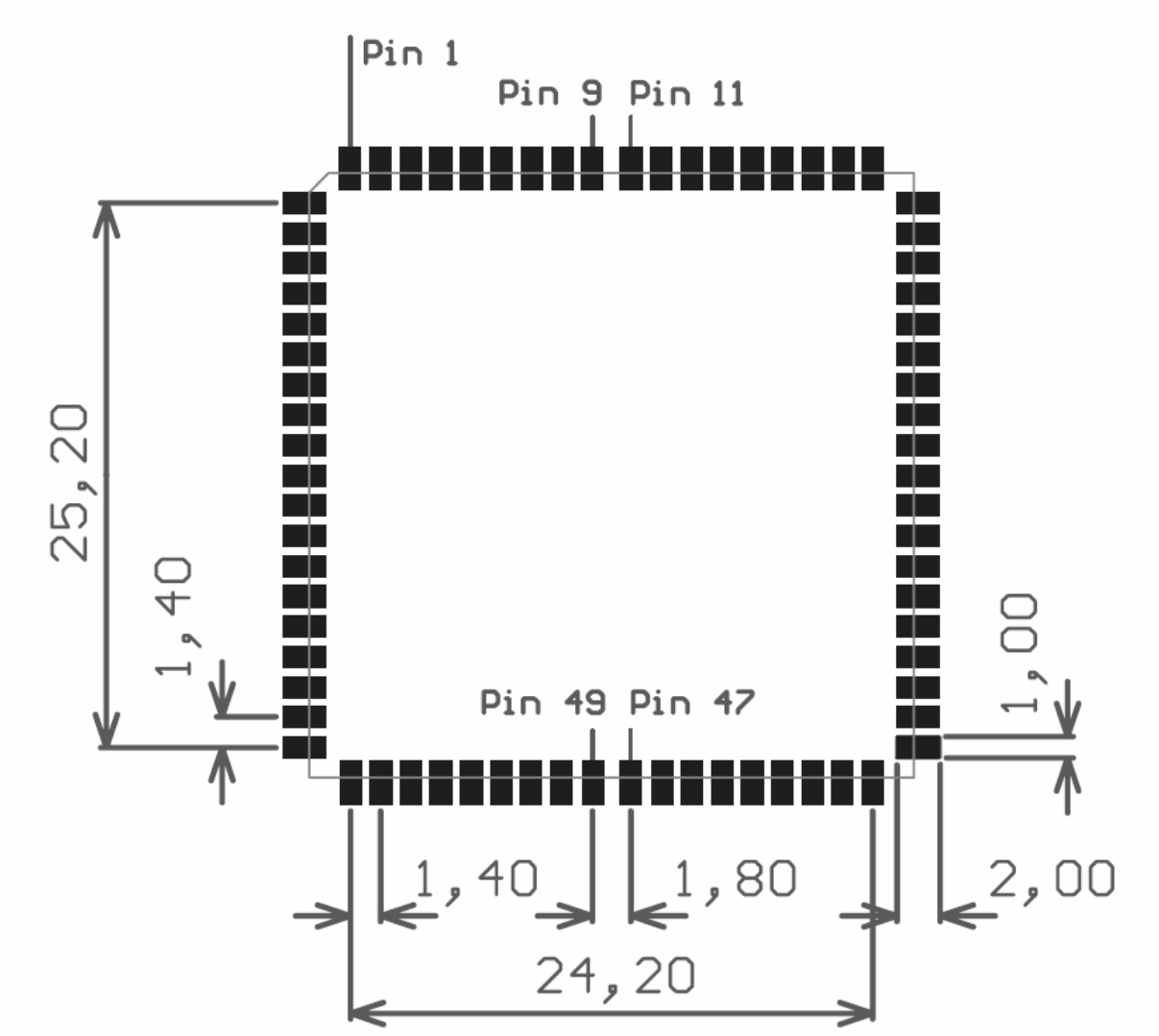


Figure 4-2: Side View of the Boarder Pads

The total minimum mounting height of the Boarder Pad version is only 3.1mm!

4.2 Footprint of Boarder Pad Baseboard

Figure 4-3 shows the pin assignment of the Boarder Pad Version.



Numbering of PINs is clockwise ascending

Figure 4-3: Boarder Pad Footprint for the Base Board (TOP VIEW)

Note: Conducting paths and Vias within the footprint must be **solder resistant**. Do not place any component within the footprint either.

4.3 Schematic Symbol of Boarder Pad Version

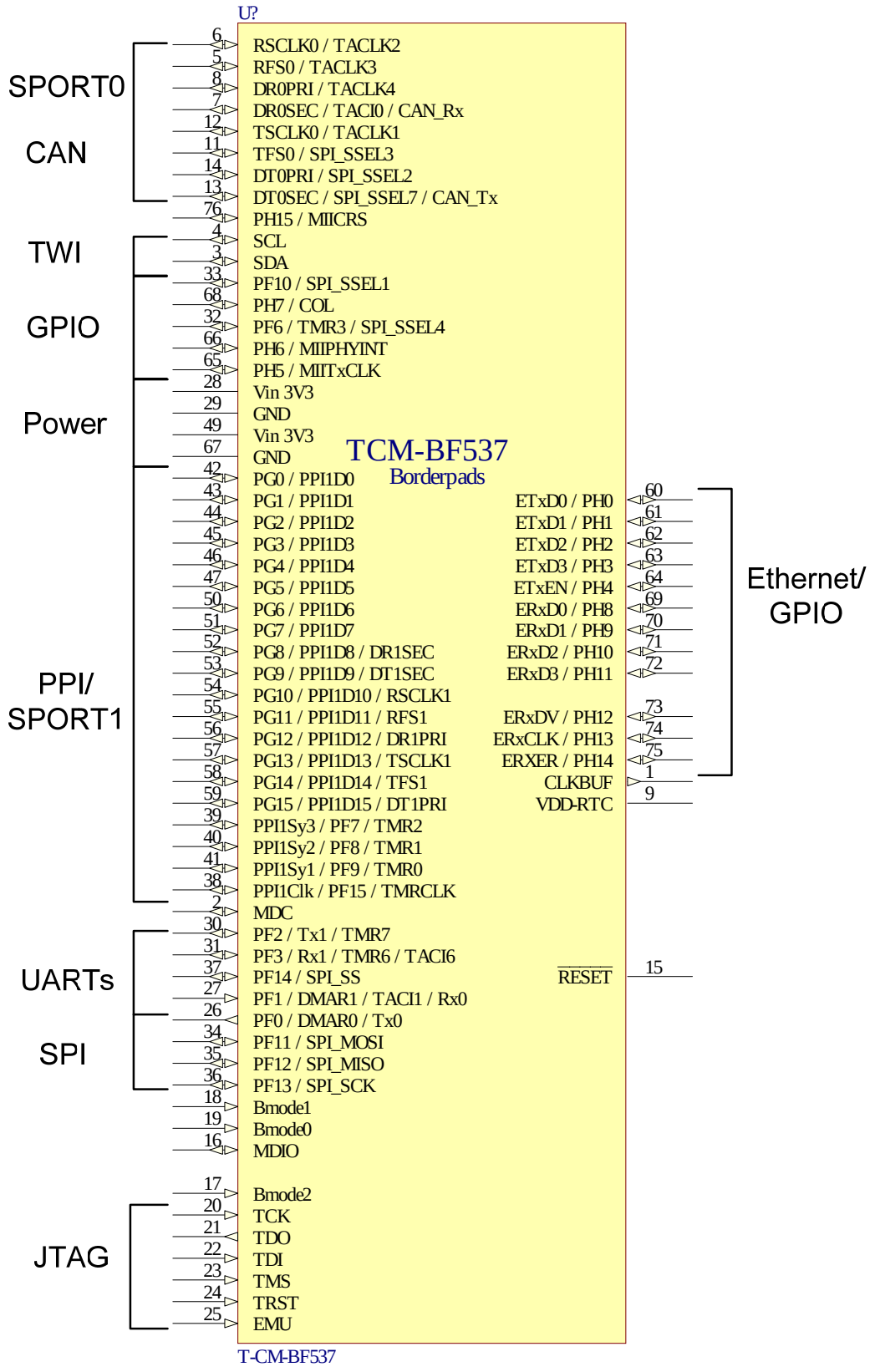


Figure 4-4: Schematics of the Boarder Pad Version of the TCM-BF537BP

4.4 Boarder Pad Pin Assignment

Pin No.	Signal	Signal type	Pin No.	Signal	Signal type
1	CLKBUF	O	39	PPI1Sy3/PF7/TMR2	I/O
2	MDC	O	40	PPI1Sy2/PF8/TMR1	I/O
3	SDA	I/O	41	PPI1Sy1/PF9/TMR0	I/O
4	SCL	I/O	42	PG0/PPI1D0	I/O
5	RFS0/TACLK3	I/O	43	PG1/PPI1D1	I/O
6	RSCLK0/TACLK2	I/O	44	PG2/PPI1D2	I/O
7	DR0SEC/TACI0/CAN_Rx	I	45	PG3/PPI1D3	I/O
8	DR0PRI/ TACLK4	I	46	PG4/PPI1D4	I/O
9	VDD-RTC	PWR	47	PG5/PPI1D5	I/O
10	not available		48	not available	
11	TFS0/SPI_SSEL3	I/O	49	Vin 3.3V	PWR
12	TSCLK0/TACLK1	I/O	50	PG6/PPI1D6	I/O
13	DT0SEC/SPI_SSEL7/CAN_Tx	O	51	PG7/PPI1D7	I/O
14	DT0PRI/SPI_SSEL2	O	52	PG8/PPI1D8/DR1SEC	I/O
15	nReset	I	53	PG9/PPI1D9/TD1SEC	I/O
16	MDIO	I/O	54	PG10/PPI1D10/RSCLK1	I/O
17	BMODE2	I	55	PG11/PPI1D11/RFS1	I/O
18	BMODE1	I	56	PG12/PPI1D12/RE1PRI	I/O
19	BMODE0	I	57	PG13/PPI1D13/TSCLK1	I/O
20	TCK	I	58	PG14/PPI1D14/TFS1	I/O
21	TDO	O	59	PG15/PPI1D15/DT1PRI	I/O
22	TDI	I	60	PH0/ETxD0	I/O
23	TMS	I	61	PH1/ETxD1	I/O
24	TRST	I	62	PH2/ETxD2	I/O
25	EMU	O	63	PH3/ETxD3	I/O
26	PF0/DMAR0/Tx0	I/O	64	PH4/ETxEN	I/O
27	PF1/DMAR1/TACI1/Rx0	I/O	65	PH5/MIITxCLK	I/O
28	Vin 3.3V	PWR	66	PH6/MIIPHYINT	I/O
29	GND	PWR	67	GND	PWR
30	PF2/Tx1/TMR7	I/O	68	PH7 / COL	I/O
31	PF3/Rx1/TMR6/TACI6	I/O	69	PH8/ERxD0	I/O
32	PF6/TMR3/SPI_SSEL4	I/O	70	PH9/ERxD1	I/O
33	PF10/SPI_SSEL1	I/O	71	PH10/ERxD2	I/O
34	PF11/SPI_MOSI	I/O	72	PH11/ERxD3	I/O
35	PF12/SPI_MISO	I/O	73	PH12/ERxDV	I/O
36	PF13/SPI_SCK	I/O	74	PH13/ERxCLK	I/O
37	PF14/SPI_SS	I/O	75	PH14/ERXER	I/O
38	PPI1Clk/PF15/TMRCLK	I/O	76	PH15 / MIICRS	I/O

Table 4-1: Boarder pin assignment

5 TCM-BF537BGA (Ball Grid Array version)

5.1 Mechanical Outline

Figure 5-1 shows the top view of the Core Module (All dimensions are given in millimeters!)

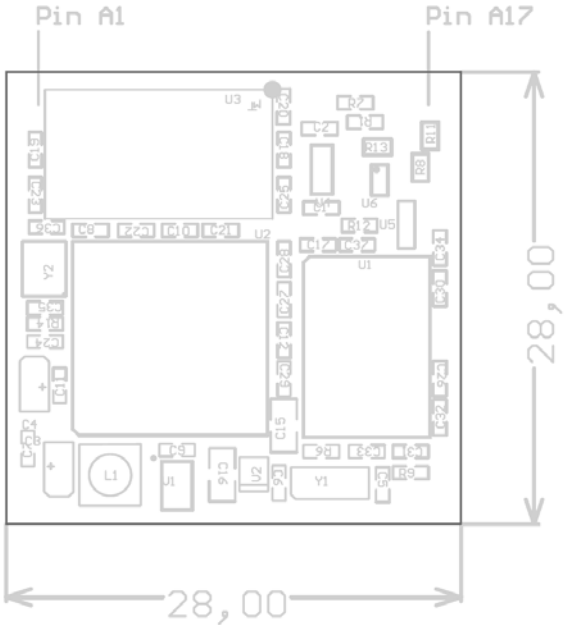


Figure 5-1: Mechanical Outline (TOP VIEW)

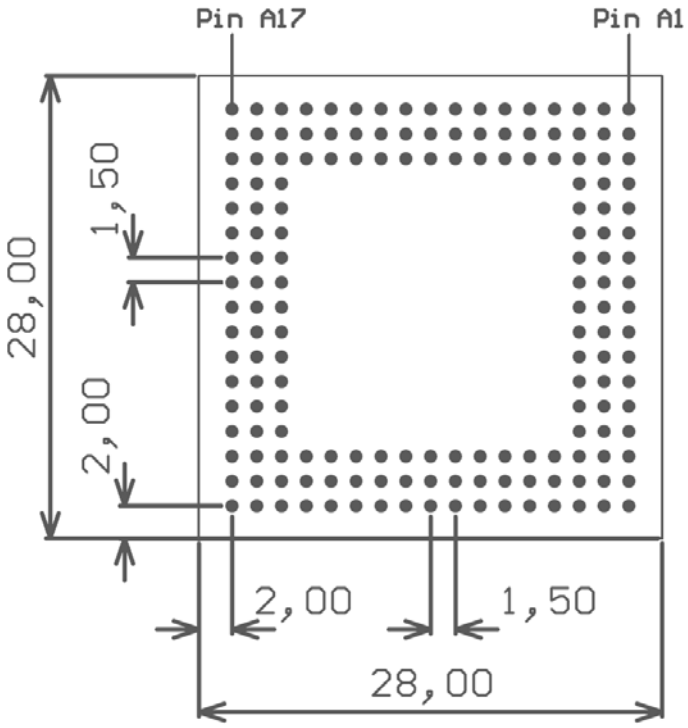


Figure 5-2: Mechanical Outline (BOTTOM VIEW)

Figure 5-3 shows the side view of the TCM-BF537BGA Core Module.

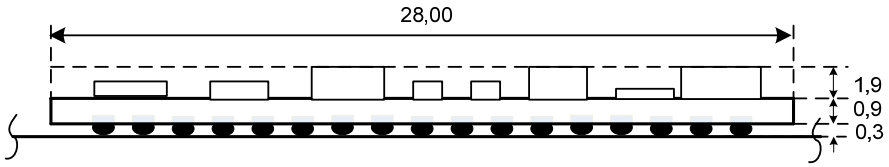


Figure 5-3: Side View of the BGA version

The total minimum mounting height of the BGA version is only 3.1mm!

5.2 BGA PAD Numbering

Figure 5-4 shows the pin assignment of the BGA version of the Core Module. The Rows I, O, Q and S are not present!

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17
D1	D2	D3												D15	D16	D17
E1	E2	E3												E15	E16	E17
F1	F2	F3												F15	F16	F17
G1	G2	G3												G15	G16	G17
H1	H2	H3												H15	H16	H17
J1	J2	J3												J15	J16	J17
K1	K2	K3												K15	K16	K17
L1	L2	L3												L15	L16	L17
M1	M2	M3												M15	M16	M17
N1	N2	N3												N15	N16	N17
P1	P2	P3												P15	P16	P17
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17

Figure 5-4: BGA Pin Assignment (TOP VIEW)

5.3 Footprint of BGA Baseboard

Figure 5-5 shows the top view of the BGA footprint for your base board.

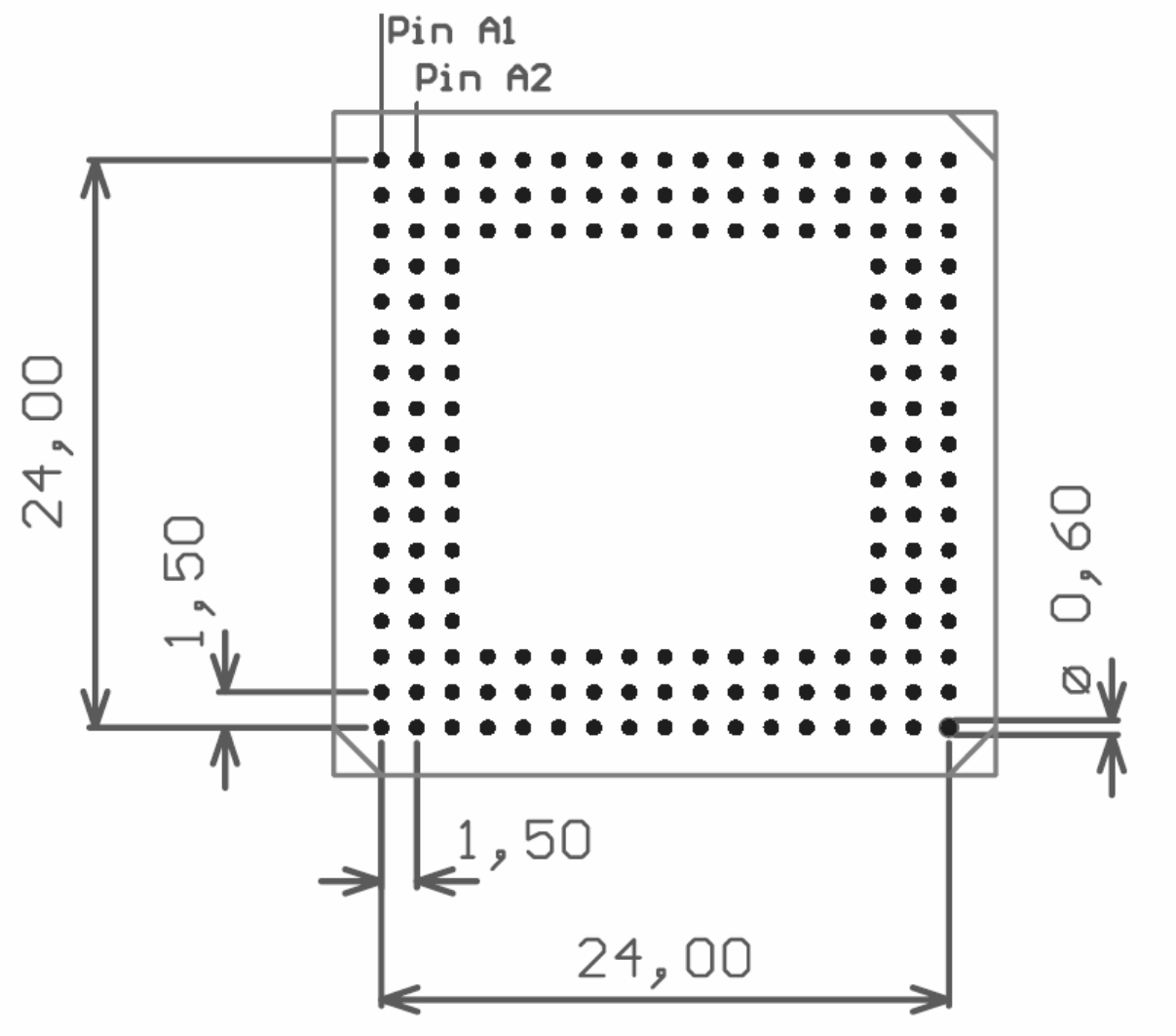


Figure 5-5: BGA Footprint for the Base Board (TOP VIEW)

5.4 Schematic Symbol of BGA Version

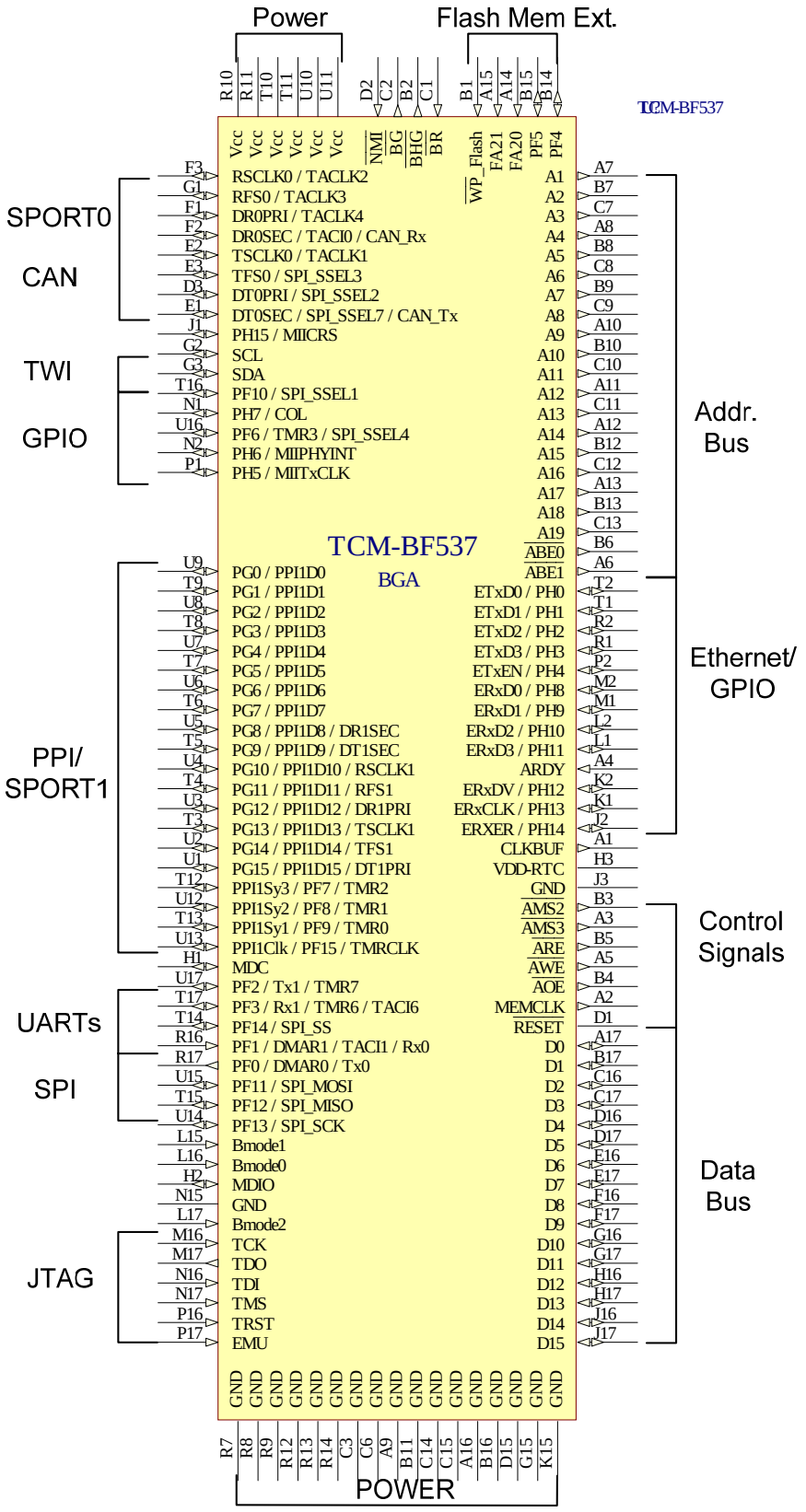


Figure 5-6: Schematics Symbol of the BGA Version of the TCM-BF537BGA

5.5 BGA Pin Assignment

Pin No.	Signal	Signal type	Pin No.	Signal	Signal type
A1	CLKBUF	O	C9	A8	O
A2	MEMCLK	O	C10	A11	O
A3	nAMS3	O	C11	A13	O
A4	ARDY	I	C12	A16	O
A5	nAWE	O	C13	A19	O
A6	nABE1	O	C14	GND	PWR
A7	A1	O	C15	GND	PWR
A8	A4	O	C16	D2	I/O
A9	GND	PWR	C17	D3	I/O
A10	A9	O	D1	nReset	I
A12	A14	O	D2	nNMI	I
A13	A17	O	D3	DT0PRI/SPI_SSEL2	O
A14	A12	O	D15	GND	PWR
A14	FA20	I	D16	D4	I/O
A15	FA21	I	D17	D5	I/O
A16	GND	PWR	E1	DT0SEC/CANTX/SPI_SSEL7	O
A17	D0	I/O	E2	TSCLK0/TACLK1	I/O
B1	nWP_Flash	I	E3	TFS0	I/O
B2	nBGH	O	E16	D6	I/O
B3	nAMS2	O	E17	D7	I/O
B4	nAOE	O	F1	DR0PRI/ TACLK4	I
B4	nAOE	O	F2	DR0SEC/TACI0/CANRX	I
B5	nARE	O	F3	RSCLK0/TACLK2	I/O
B6	nABE0	O	F16	D8	I/O
B7	A2	O	F17	D9	I/O
B8	A5	O	G1	RFS0/TACLK3	I/O
B9	A7	O	G2	SCL	I/O
B10	A10	O	G3	SDA	I/O
B11	GND	PWR	G15	GND	PWR
B12	A15	O	G16	D10	I/O
B13	A18	O	G17	D11	I/O
B14	PF4/TMR5/SPI_SSL6	I/O	H1	MDC	I/O
B15	PF5/TMR4/SPI_SSL5	I/O	H2	MDIO	I/O
B16	GND	PWR	H3	VDD-RTC	PWR
B17	D1	I/O	H16	D12	I/O
C1	nBR	I	H17	D13	I/O
C2	nBG	O	J1	PH15/MIICRS	I/O
C3	GND	PWR	J2	PH14/ERXER	I/O
C6	GND	PWR	J3	GND	PWR
C7	A3	O	J17	D15	I/O
C8	A6	O	K1	PH13/ERxCLK	I/O
K2	PH12/ERxDV	I/O	T2	PH0/ETxD0	I/O
K15	GND	PWR	T3	PG13/PPI1D13/TSCLK1	I/O
L1	PH11/ERxD3	PWR	T4	PG11/PPI1D11/RFS1	I/O

L2	PH10/ERxD2	I/O	T5	PG9/PPI1D9/TD1SEC	I/O
L15	BMODE1	I	T6	PG7/PPI1D7	I/O
L16	BMODE0	I	T7	PG5/PPI1D5	I/O
L17	BMODE2	I	T8	PG3/PPI1D3	I/O
M1	PH9/ERxD1	I/O	T9	PG1/PPI1D1	I/O
M2	PH8/ERxD0	I/O	T10	Vcc	PWR
M16	TCK	I	T11	Vcc	PWR
M17	TDO	O	T12	PPI1SY3/PF7/TMR2	I/O
N1	PH7 / COL	I/O	T13	PPI1SY1/PF9/TMR0	I/O
N2	PH6/MIIPHYINT	I/O	T14	PF14/SPI_SS	I/O
N15	GND	PWR	T15	PF12/SPI_MISO	I/O
N16	TDI	I	T16	PF10/SPI_SSEL1	I/O
N17	TMS	I	T17	PF3/Rx1/TMR6/TACI6	I/O
P1	PH5/MIITxCLK	I/O	U1	PG15/PPI1D15/DT1PRI	I/O
P2	PH4/ETxEN	I/O	U2	PG14/PPI1D14/TFS1	I/O
P16	TRST	I	U3	PG12/PPI1D12/RE1PRI	I/O
P17	EMU	I	U4	PG10/PPI1D10/RSCLK1	I/O
R1	PH3/ETxD3	I/O	U5	PG8/PPI1D8/DR1SEC	I/O
R2	PH2/ETxD2	I/O	U6	PG6/PPI1D6	I/O
R7	GND	PWR	U7	PG4/PPI1D4	I/O
R8	GND	PWR	U8	PG2/PPI1D2	I/O
R9	GND	PWR	U9	PG0/PPI1D0	I/O
R10	Vcc	PWR	U10	Vcc	PWR
R11	Vcc	PWR	U11	Vcc	PWR
R12	GND	PWR	U12	PPI1Sy2/PF8/TMR1	I/O
R13	GND	PWR	U13	PPI1Clk/PF15/TMRCLK	I/O
R14	GND	PWR	U14	PF13/SPI_SCK	I/O
R16	PF1/DMAR1/TACI1/Rx0	I/O	U15	PF11/SPI_MOSI	I/O
R17	PF0/DMAR0/Tx0	I/O	U16	PF6/TMR3/SPI_SSEL4	I/O
T1	PH1/ETxD1	I/O	U17	PF2/Tx1/TMR7	I/O

Table 5-1: BGA Version Pin Assignment

5.6 Flash Memory Extension PINS

5.6.1 PINS FA20 and FA21

These pins are the Address lines A20 and A21 of the Intel P30 Flash and are pulled down by default.
If only 2MB of Flash are needed leave these pins open. PF4 and PF5 can be used as IO pins.
If 4MB are needed connect PF4 to FA20 for addressing the upper 2MB
If 8MB are needed connect PF5 to FA21 for addressing the upper 4MB

5.6.2 PINS PF4 and PF5

Can be used to extend the addressable Flash memory or as PF4 and PF5 Processor IO pins. Please see Table 5-1 for the pin Assignment.

5.6.3 /WP_FLASH

Is pulled high by default so flash is unprotected. To write protect the flash connect this pin to GND

6 Application Example Schematics

In the following two examples of connecting a Physical Ethernet chip and a USB 2.0 chip to the Core Module are given.

6.1 Schematic Example for Connecting a Physical Ethernet Chip

Since the ADSP-BF537 Blackfin Chip from Analog Devices contains already Ethernet functionality only a physical Ethernet chip has to be connected to the TCM-BF537 Core Module in order to use this feature.

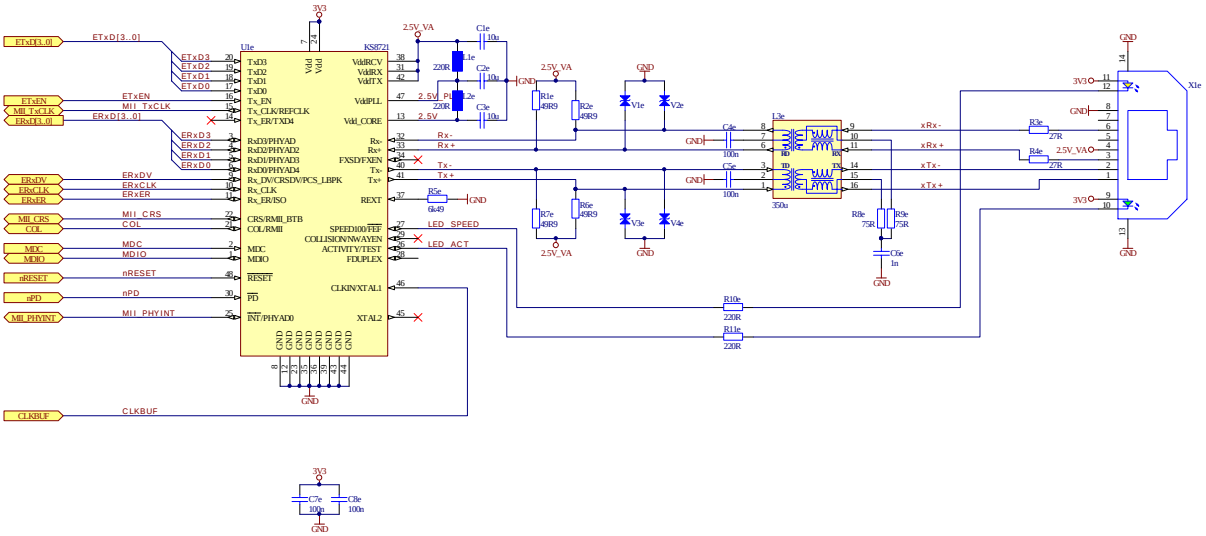


Figure 6-1: Configuration with Physical Chip

Designator	Value	Part Number	Description	Quantity
C1e, C2e, C3e	10u	C0805C106K9PAC	Capicator non-polarized	3
C4e, C5e, C7e, C8e	100n	2238 246 19876	Capicator non-polarized	4
C6e	1n	2238 586 15623	Capicator non-polarized	1
L1e, L2e	220Z	74279263	Ferrite	2
L3e	350u	749010010	Inductor	1
R1e, R2e, R6e, R7e	49R9	MC 0.063W 0603 1% 49R9	Resistor	4
R3e, R4e	27R	MC 0.063W 0603 1% 27R	Resistor	2
R5e	6k49	MC 0.063W 0603 1% 6K49	Resistor	1
R8e, R9e	75R	MC 0.0654W 0603 1% 75R	Resistor	2
R10e, R11e	220R	MC 0.063W 0603 1% 220R	Resistor	2
U1e		KS8721BLI	10/100BASE Physical Layer Transceiver	1
V1e, V2e, V3e, V4e		CDS3C05GTA	ESD Protection Diode	4
X1e		2-406549-1	RJ45-Connector with LEDs	1

Table 6-1: Bill of Material of Sample Schematic

6.2 Schematic Example for Connecting a USB 2.0 Chip

The following example shows how to connect a USB 2.0 chip to the TCM-BF537 core Module.

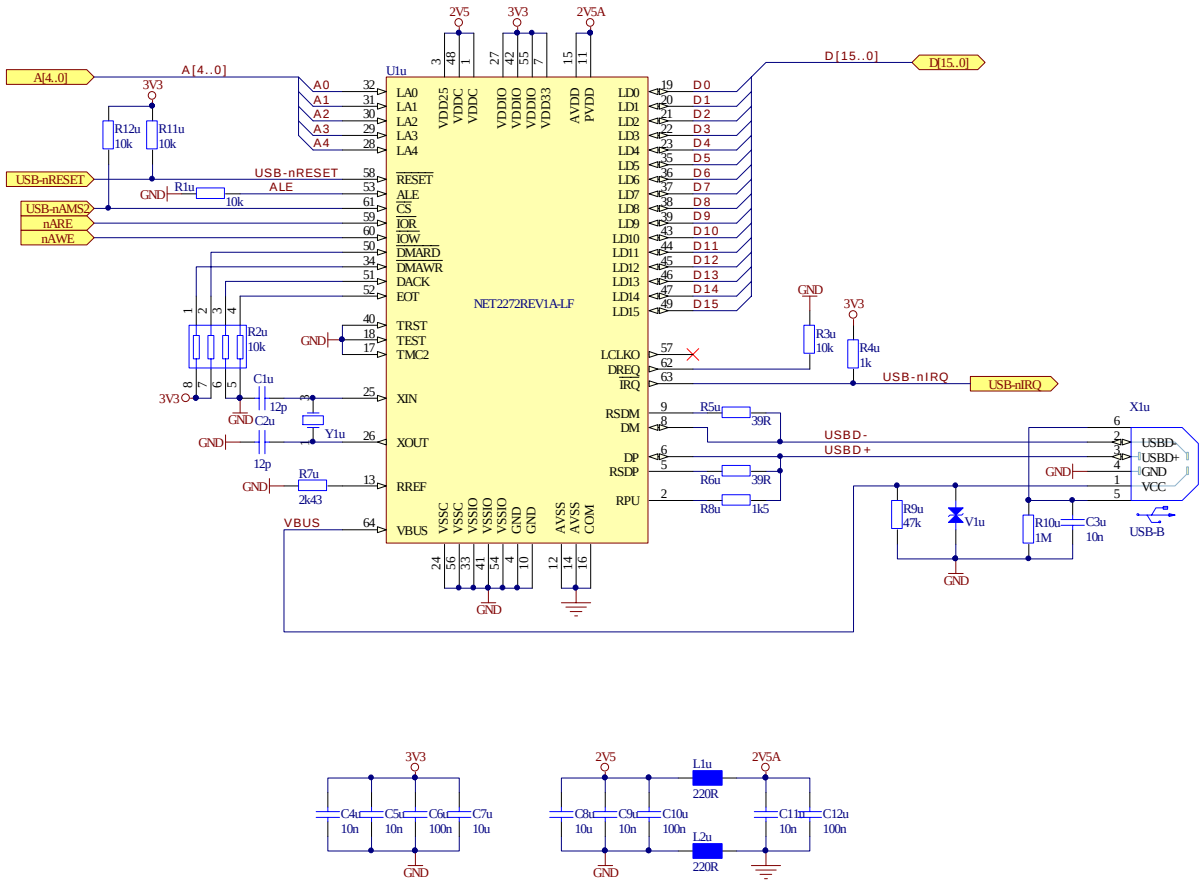


Figure 6-2: Configuration with USB 2.0 Chip

Designator	Value	Part Number	Description	Quantity
C1u, C2u	12p	2238 867 15129	Capicator non-polarized	2
C3u, C4u, C5u, C9u, C11u	10n	2238 916 15636	Capicator non-polarized	5
C6u, C10u, C12u	100n	2238 246 19876	Capicator non-polarized	3
C7u, C8u	10u	C0805C106K9PAC	Capicator non-polarized	2
L1u, L2u	220R	74279263	Ferrite	2
R1u, R3u, R11u, R12u	10k	MC 0.063W 0603 1% 10K	Resistor	4
R2u	10k	2350 025 11003	4-Resistor Array	1
R4u	1k	MC 0.063W 0603 1% 1k	Resistor	1
R5u, R6u	39R	MC 0.0654W 0603 1% 39R	Resistor	2
R7u	2k43	MULTICOMP	Resistor	1
R8u	1k5	MC 0.063W 0603 1% 1K5	Resistor	1
R9u	47k	MC 0.063W 0603 1% 47k	Resistor	1
R10u	1M	MC 0.063W 0603 1% 1M	Resistor	1
U1u		NET2272REV1A-LF	USB 2.0 Peripheral Controller TQPF	1
V1u		CDS3C05GTA		1

X1u		2411 01	USB-Device Normal	1
Y1u		Q 30.0-JXS32-12-10/20	Crystal Oscillator	1

Table 6-2: Bill of Material of Sample Schematic

7 Software Support

7.1 BLACKSheep

The Core Module is delivered with a pre-flashed basic version of the BLACKSheep VDK multithreaded framework. It contains a boot-loader for flashing the Core Module via the serial port.

Please mind the software development documents.

7.2 uClinux

The Core Module is supported by the open source platform at http://blackfin.uclinux.org. Since the Core Modules are pre-flashed with BLACKSheep you have to flash uBoot first. For flashing the uBoot you can use the BLACKSheep boot-loader.

For using the Ethernet functionality of the TCM-BF537 Core Modules you need the EXT-BF5xx-ETH-USB Blackfin Extension Board.

8 Known Bugs

	NONE

Table 8-1: Known Bugs

9 Product Changes

Version	Changes
V1.1	Boarder Pad and BGA Versions added, 28mmx28mm outline

Table 9-1: Product Changes

10 Document Revision History

Date	Document Revision
2007 04 17	Borderpad and BGA symbols corrected; Rx1 and Tx1 were mixed up
2007 04 04	Corrections of the description of the BP and BGA versions.
2007 01 08	Corrected Typo in page 7 Table 2-2: PF5 one time instead of two times PF4
2006 10 02	Release V1.1 of TCM Boards Main updates: Separate Connector, Boarder and BGA pad version Boader Pads: 76 Boarder pads without Data and Address bus pins Connector Version: As in version V1.0 BGA Version: Additional Processor pins, added Flash addressing flexibility Removed limited address range, all 8MB addressable
2006 04 26	Updated bug list: only 4MB addressable.
2006 04 26	Updated document: Connector symbol, fixed Bug naming of pin 22 and pin 40 (connector version) Rx and Tx was flipped.
2006 03 07	First release V1.0 of the Document

Table 10-1: Revision History

A List of Figures and Tables

Figures

Tables