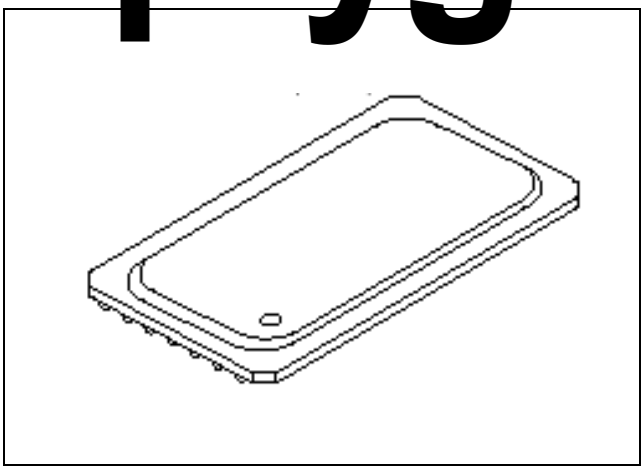
[redacted]

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 250/200/170 mA at minimum cycle time
- Single 3.3 V ± 0.3V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- [redacted]mperature Option: –40 to 85°C
- [redacted]ckage
  - [redacted]mm, 119-bump, 1.27mm pitch BGA
  - [redacted]iant 119-bump BGA*



The GS7[redacted]24A is a high speed CMOS Static RAM organized as 131,072 words by 24 bits. Static design eliminates the need for [redacted] or timing strobes. Operating on a single 3[redacted]y, and all inputs and outputs are T[redacted]3024A is availa[redacted]-bump B[redacted]

[redacted]

A[redacted]	Address [redacted]ut	DQ[redacted]Q[redacted]	Data input/[redacted]put
$\overline{WE}$	Write enable input	$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input	V_{SS}	Ground
V_{DD}	+3.3 V power supply		

***All GSI Technology packages are at least 5/6 RoHS compliant.**
Packages listed with the additional "G" designator are 6/6 RoHS compliant.

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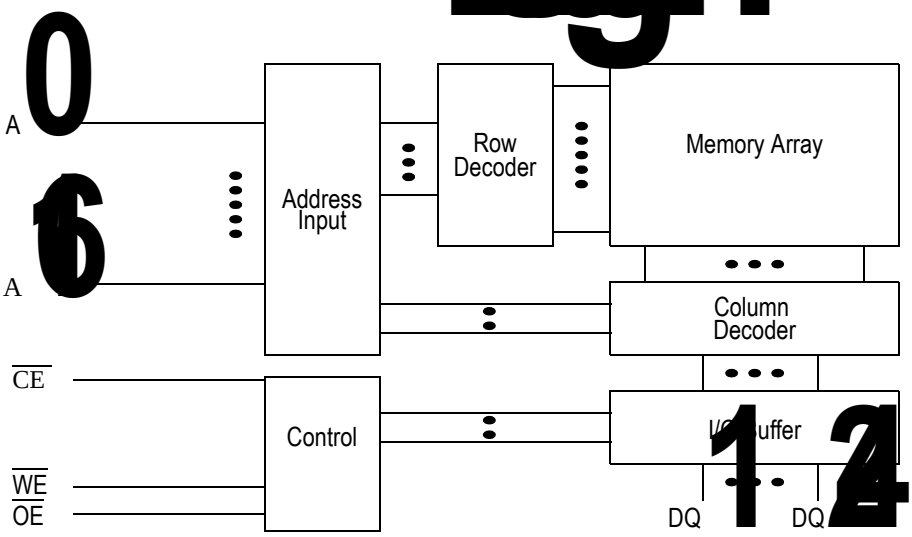

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H	X	X	Not selected	High Z	ISB1, ISB2
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	
	H		Output disable	High Z	

X: "

Supply Voltage		–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
llowable BGA power dissipation	PD	1.5	W
Storage temperature	T_{STG}	–55 to 150	°C

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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Supply Voltage for -10/12	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for -8	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	–40	—	85	°C

1. ltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. should be greater than – a exceed 20 ns.

Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
I/O Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

1.
2. 0% tested.

Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
Output Leakage Current	I_{OL}	Output High Z, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—
Output Low Voltage	V_{OL}	I_{OL} = +4 mA	—	0.4 V

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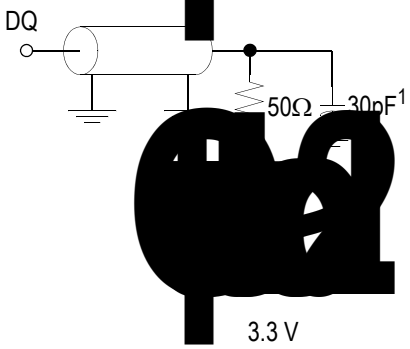
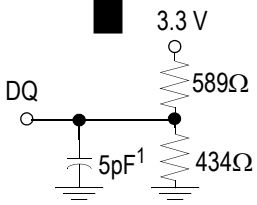
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	t = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	[illegible]
[illegible]tput reference level	[illegible]
[illegible] Output load	[illegible]





1. Includes scope and jig capacitance
2. [illegible]s a[illegible]ified with output loading as shown in [illegible] unl[illegible] othe[illegible] noted
3. [illegible]ad t_{OHZ}

Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	250 mA	200 mA	170 mA	260 mA	210 mA	180 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	40 mA	40 mA	30 mA	50 mA	50 mA	40 mA
Standby Current	I_{SB2}	CE $\ge V_{DD}$ - 0.2V All other inputs $\ge V_{DD}$ - 0.2V or $\le$ 0.2V	10 mA			20 mA		

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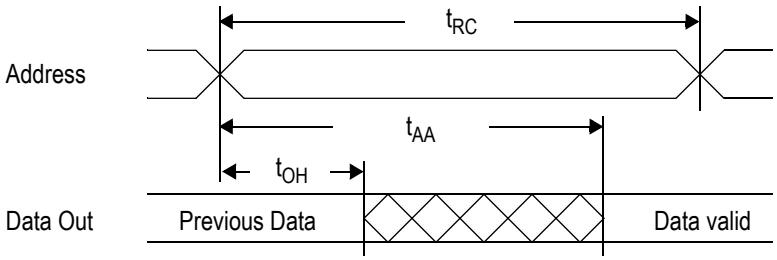
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	8	—	10	—	12	ns
MUX control to output valid (V/$\overline{S}$)	t_{AV}	—	8	—	10	—	12	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	4	—	5	—	6	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Output hold from MUX controls change	t_{OH1}	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	[illegible]*	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	[illegible]	—	4	—	5	—	6	ns

* These parameters are sampled and are not 100

[redacted]



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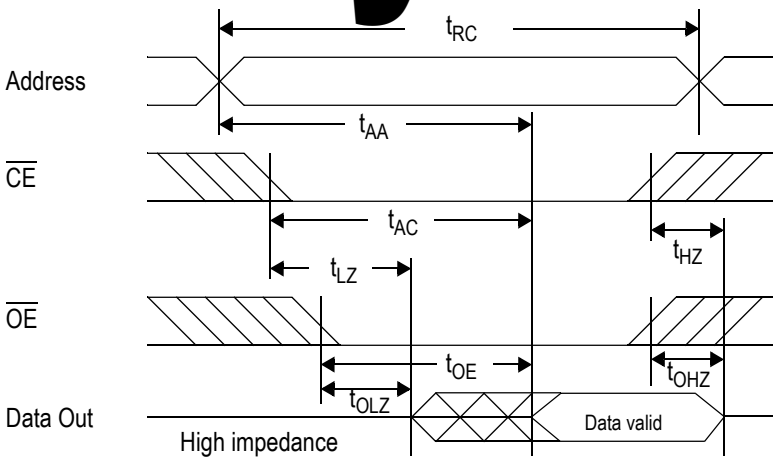

Write cycle time	t_{WC}	8	—	10	—	12	—	ns
Address valid to end of write	t_{AW}	5.5	—	7	—	8	—	ns
Chip enable to end of write ($\overline{CE}$)	t_{CW}	5.5	—	7	—	8	—	ns
Data set up time	t_{DW}	4	—	5	—	6	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	5.5	—	7	—	8	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output Low Z from end of write	t_{WLZ}*	2	—	3	—	3	—	ns
Write to output in High Z	t_{WHZ}*	—	4	—	5	—	6	ns

* These parameters are sampled and are not 100% tested

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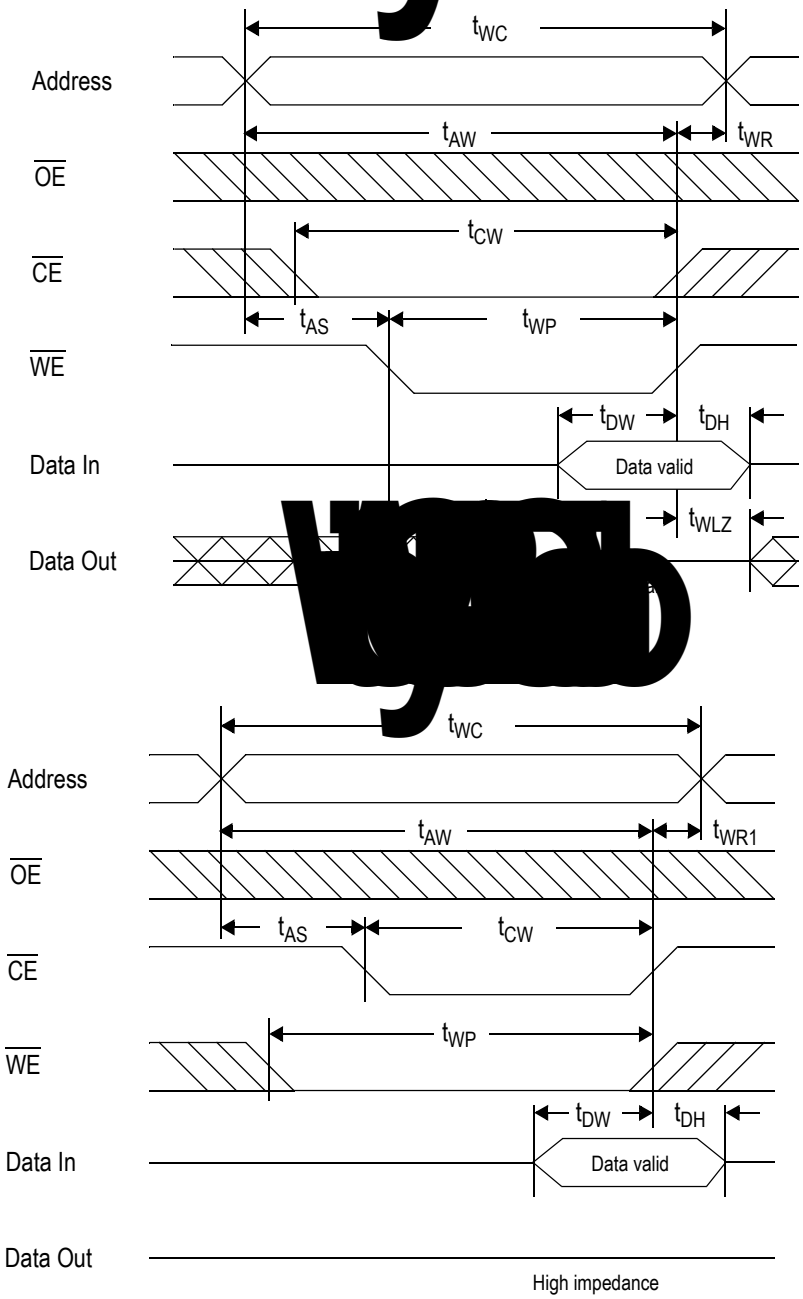

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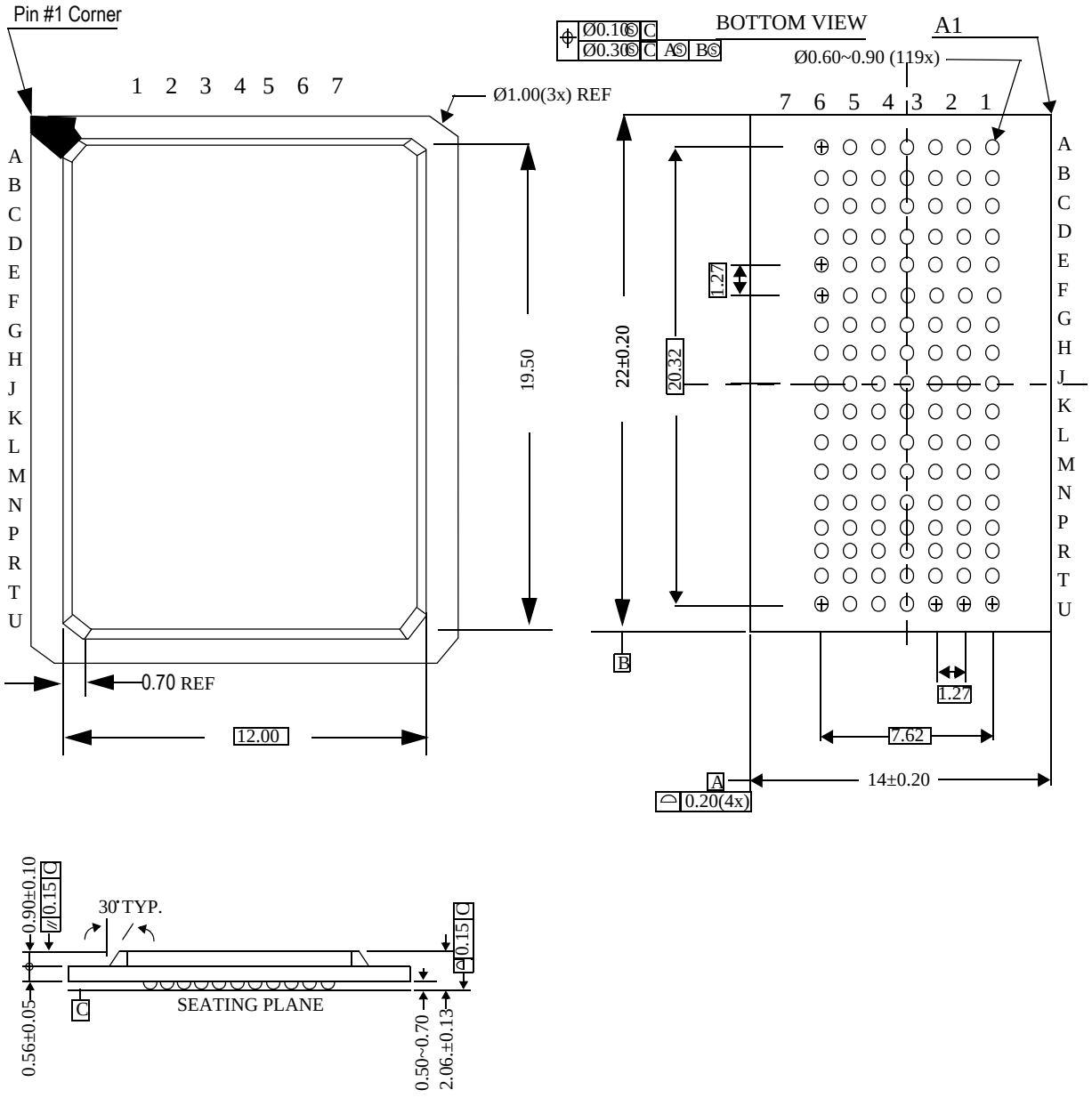
Package Dimensions—119-Bump FPBGA (Package B, Variation 1)

(Date Code: yyww.31)



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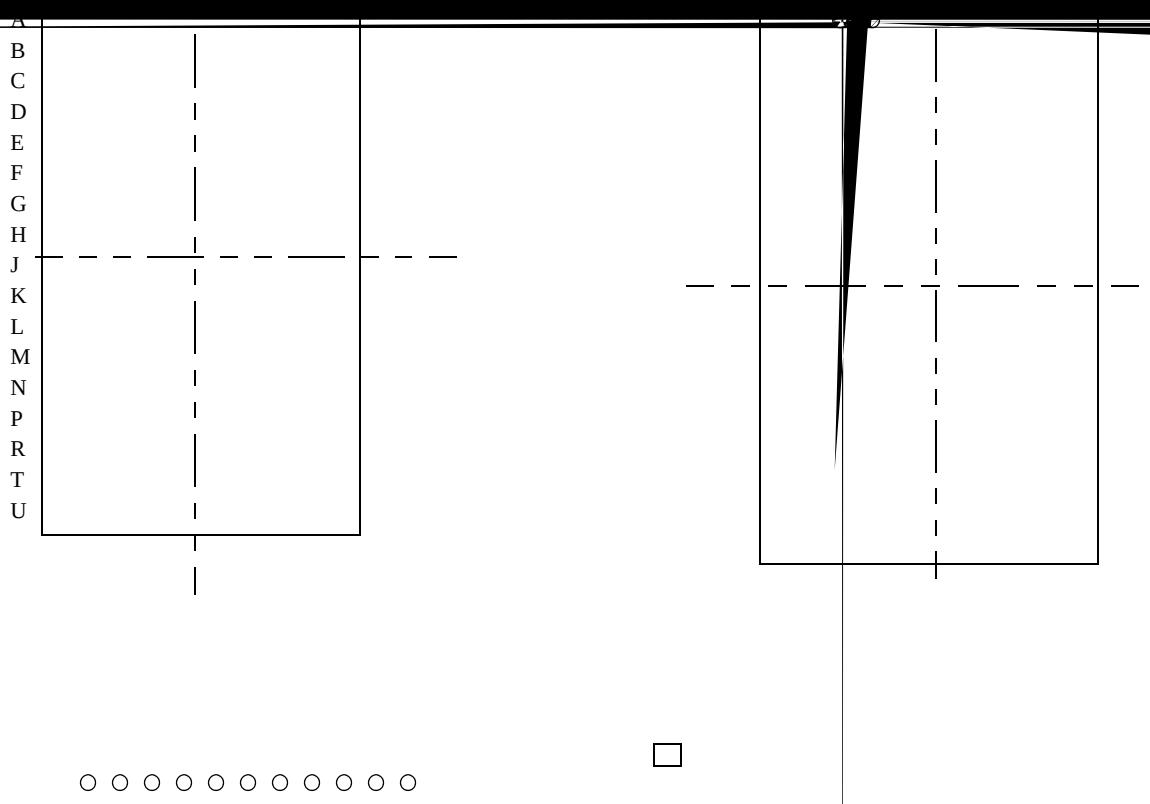

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GS73024AB-8	119-Bump BGA	8 ns	Commercial	MP
GS73024AB-10	119-Bump BGA	10 ns	Commercial	MP
GS73024AB-12	119-Bump BGA	12 ns	Commercial	MP
GS73024AB-8I	119-Bump BGA	8 ns	Industrial	MP
GS73024AB-10I	119-Bump BGA	10 ns	Industrial	MP
GS73024AB-12I	119-Bump BGA	12 ns	Industrial	MP
GS73024AGB-8	RoHS-compliant 119-Bump BGA	8 ns	Commercial	PQ
GS73024AGB-10	RoHS-compliant 119-Bump BGA	10 ns	Commercial	PQ
GS73024AGB-12	RoHS-compliant 119-Bump BGA	12 ns	Commercial	PQ
GS73024AGB-8I	RoHS-compliant 119-Bump BGA	8 ns	Industrial	PQ
GS73024AGB-10I	RoHS-compliant 119-Bump BGA	10 ns	Industrial	PQ
GS73024AGB-12I	RoHS-compliant 119-Bump BGA	12 ns	Industrial	PQ

1. Customers requiring Tape and Reel should add the character “T” to the end of the part number. For example: GS73024AB-12T.
2. All GSI Technology packages are at least 5/6 RoHS compliant. Packages listed with the additional “G” designator are 6/6 RoHS compliant.
3. Please see pages 9 and 10 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.

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Rev. Code: Old; New	Types of Changes Format or Content	Page/Revisions/Reason
GS73024A_r1		• Creation of new datasheet
GS73024A_r1; GS73024A_r1_01	Content	• Corrected pinout (balls C3, C5, R2, R3, R5, R6 changed to NC) • Corrected pin description table to reflect pinout corrections • Corrected truth table to reflect pinout corrections
GS73024A_r1_01; GS73024A_r1_02	Content/Format	• Updated format • Added variation informtion to package mechanical
GS73024A_r1_02; GS73024A_r1_03	Content	• Added Variation 2 119 BGA to datasheet • Added date codes to mechanicals
GS73024A_r1_03; GS73024A_r1_04	Content	• Added RoHS-compliant package information • Added RoHS-compliant disclaimers

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