19-4209; Rev 0; 7/08

EVALUATION KIT AVAILABLE

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

MAX5134

General Description

The MAX5134 is a low-power, quad 16-bit, buffered voltage-output, high-linearity digital-to-analog converter (DAC). It uses a precision internal reference or a precision external reference for rail-to-rail operation. The MAX5134 accepts a wide +2.7V to +5.25V supply-voltage range to accommodate most low-power and low-voltage applications. The device accepts a 3-wire SPI™-/QSPI™-/MICROWIRE™-/DSP-compatible serial interface to save board space and reduce the complexity of optically isolated and transformer-isolated applications. The digital interface's double-buffered hardware and software LDAC provide simultaneous output update. The serial interface features a READY output for easy daisy-chaining of several MAX5134 devices and/or other compatible devices. The MAX5134 includes a hardware input to power-up or reset the DAC outputs to zero or midscale, providing additional safety for applications that drive valves or other transducers that need to be off during power-up. The high linearity of the DACs makes these devices ideal for precision control and instrumentation applications. The MAX5134 is available in an ultra-small (4mm x 4mm), 24-pin TQFN package and is specified over the -40°C to +105°C extended industrial temperature range.

Applications

- Automatic Test Equipment
- Automatic Tuning
- Communication Systems
- Data Acquisition
- Gain and Offset Adjustment
- Portable Instrumentation
- Power-Amplifier Control
- Process Control and Servo Loops
- Programmable Voltage and Current Sources

Functional Diagram and Typical Operating Circuit appear at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.

Features

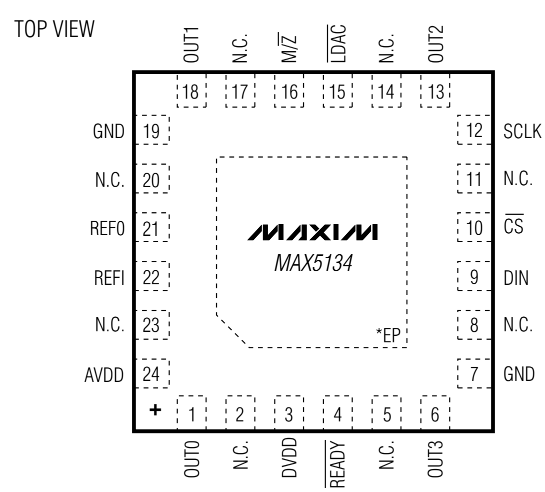
- ♦ **16-Bit Resolution in a 4mm x 4mm, 24-Pin TQFN Package**
- ♦ **Hardware-Selectable Power-Up or Reset-to-Zero/ Midscale DAC Output**
- ♦ **Double-Buffered Input Registers**
- ♦ **LDAC Asynchronously Updates DAC Outputs Simultaneously**
- ♦ **READY Facilitates Daisy Chaining**
- ♦ **High-Performance 10ppm/°C Internal Reference**
- ♦ **Guaranteed Monotonic Over All Operating Conditions**
- ♦ **Wide +2.7V to +5.25V Supply Range**
- ♦ **Rail-to-Rail Buffered Output Operation**
- ♦ **Low Gain Error (Less Than ±0.5%FS) and Offset (Less Than ±10mV)**
- ♦ **30MHz 3-Wire SPI-/QSPI-/MICROWIRE-/ DSP-Compatible Serial Interface**
- ♦ **CMOS-Compatible Inputs with Hysteresis**
- ♦ **Low-Power Consumption (I_{SHDN} = 2µA max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5134AGTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



THIN QFN
4mm x 4mm

*EXPOSED PAD.

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

ABSOLUTE MAXIMUM RATINGS

AVDD to GND ....-0.3V to +6V
DVDD to GND..-0.3V to +6V
OUT0–OUT3 to GND ....-0.3V to the lower of (AVDD + 0.3V) and +6V
REFI, REFO, M/$\overline{Z}$ to GND ....-0.3V to the lower of (AVDD + 0.3V) and +6V
SCLK, DIN, $\overline{CS}$ to GND ....-0.3V to the lower of (DVDD + 0.3V) and +6V
$\overline{LDAC}$, $\overline{READY}$ to GND ....-0.3V to the lower of (DVDD + 0.3V) and +6V

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate at 17.5mW/°C above +70°C) 2222.2mW
Maximum Current into Any Input or Output with the Exception of M/$\overline{Z}$ Pin ....±50mA
Maximum Current into M/$\overline{Z}$ Pin ....±5mA
Operating Temperature Range ....-40°C to +105°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{GND} = 0, V_{REFI} = V_{AVDD} - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY (Notes 1, 2)							
Resolution	N			16			Bits
Integral Nonlinearity	INL	V_{REFI} = 5V, AVDD = 5.25V	(Note 3)	-8	±2	+10	LSB
			T_A = +25°C			±6	
Differential Nonlinearity	DNL	Guaranteed monotonic		-1.0		+1.0	LSB
Offset Error	OE	(Note 4)		-10	±1	+10	mV
Offset-Error Drift					±4		µV/°C
Gain Error	GE	(Note 4)		-0.5	±0.2	+0.5	% of FS
Gain Temperature Coefficient					±2		ppm FS/°C
REFERENCE INPUT							
Reference-Input Voltage Range	V_{REFI}	AVDD = 3V to 5.25V		2		AVDD	V
		AVDD = 2.7V to 3V		2		AVDD - 0.2	
Reference-Input Impedance					113		kΩ
INTERNAL REFERENCE							
Reference Voltage	V_{REFO}	T_A = +25°C		2.434	2.440	2.443	V
Reference Temperature Coefficient		(Note 5)			10	25	ppm/°C
Reference Output Impedance					1		Ω
Line Regulation					100		ppm/V
Maximum Capacitive Load	C_R				0.1		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{GND} = 0, $V_{REFI} = V_{AVDD}$ - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUT VOLTAGE (Note 2)						
Output Voltage Range		No load	0.02		AVDD - 0.02	V
DC Output Impedance				0.1		Ω
Maximum Capacitive Load (Note 5)	C_L	Series resistance = 0		0.2		nF
		Series resistance = 500Ω		15		µF
Resistive Load	R_L		2			kΩ
Short-Circuit Current	I_{SC}	AVDD = 5.25V		±35		mA
		AVDD = 2.7V	-40	±20	+40	
Power-Up Time		From power-down mode		25		µs
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$) (Note 6)						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Leakage Current	I_{IN}	V_{IN} = 0 or DVDD	-1	±0.1	+1	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS ($\overline{READY}$)						
Output High Voltage	V_{OH}	I_{SOURCE} = 3mA	DVDD - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	Positive and negative		1.25		V/µs
Voltage-Output Settling Time	t_S	1/4 scale to 3/4 scale V_{REFI} = AVDD = 5V settle to ±2 LSB (Note 5)		5		µs
Digital Feedthrough		Code 0, all digital inputs from 0 to DVDD		0.5		nV•s
Major Code Transition Analog Glitch Impulse				12		nV•s
Output Noise		10kHz		120		nV/√Hz
Integrated Output Noise		1Hz to 10kHz		18		µV
DAC-to-DAC Crosstalk				25		nV•s

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 2.7V to 5.25V, V_{DVDD} = 2.7V to 5.25V, $V_{AVDD} \geq V_{DVDD}$, V_{GND} = 0, $V_{REFI} = V_{AVDD}$ - 0.25V, C_{OUT} = 200pF, R_{OUT} = 10kΩ, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS (Note 7)						
Analog Supply Voltage Range	AVDD		2.7		5.25	V
Digital Supply Voltage Range	DVDD		2.7		AVDD	V
Supply Current	I_{AVDD}	No load, all digital inputs at 0 or DVDD		2.5	3.6	mA
	I_{DVDD}			1	10	µA
Power-Down Supply Current	I_{AVPD}	No load, all digital inputs at 0 or DVDD		0.2	2	µA
	I_{DVPD}			0.1	2	
TIMING CHARACTERISTICS (Note 8) (Figure 1)						
Serial-Clock Frequency	f_{SCLK}		0		30	MHz
SCLK Pulse-Width High	t_{CH}		13			ns
SCLK Pulse-Width Low	t_{CL}		13			ns
$\overline{CS}$ Fall-to-SCLK Fall Setup Time	t_{CSS}		8			ns
SCLK Fall-to $\overline{CS}$-Rise Hold Time	t_{CSH}		5			ns
DIN-to-SCLK Fall Setup Time	t_{DS}		10			ns
DIN-to-SCLK Fall Hold Time	t_{DH}		2			ns
SCLK Fall to $\overline{READY}$ Transition	t_{SRL}	(Note 9)			30	ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		33			ns
$\overline{LDAC}$ Pulse Width	$t_{LDACPWL}$		33			ns

Note 1: Static accuracy tested without load.
Note 2: Linearity is tested within 20mV of GND and AVDD, allowing for gain and offset error.
Note 3: Codes above 2047 are guaranteed to be within ±8 LSB.
Note 4: Gain and offset tested within 100mV of GND and AVDD.
Note 5: Guaranteed by design.
Note 6: Device draws current in excess of the specified supply current when a digital input is driven with a voltage of VI < DVDD - 0.6V or VI > 0.5V. At VI = 2.2V with DVDD = 5.25V, this current can be as high as 2mA. The SPI inputs are CMOS-input level compatible. The 30MHz clock frequency cannot be guaranteed for a minimum signal swing.
Note 7: Excess current from AVDD is 10mA when powered without DVDD. Excess current from DVDD is 1mA when powered without AVDD.
Note 8: All timing specifications are with respect to the digital input and output thresholds.
Note 9: Maximum daisy-chain clock frequency is limited to 25MHz.

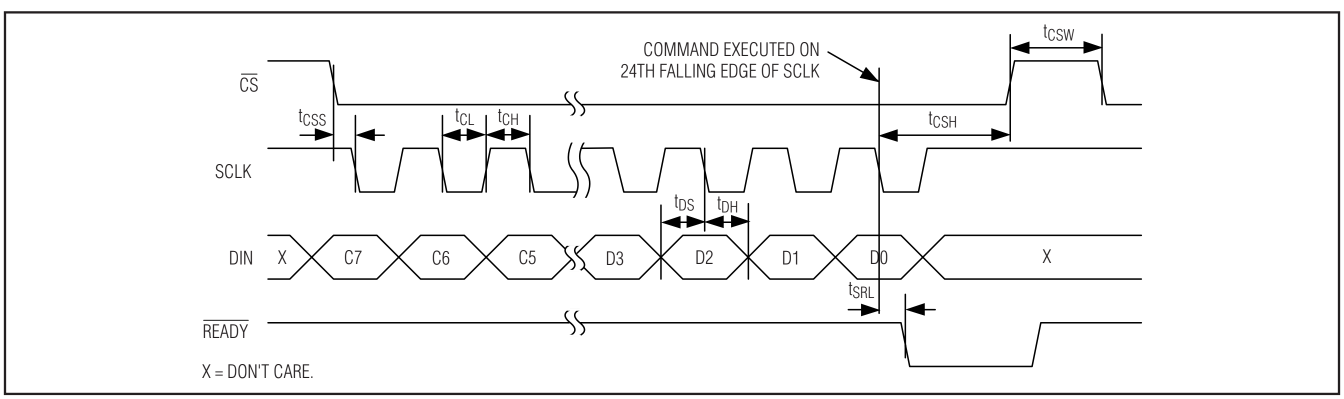
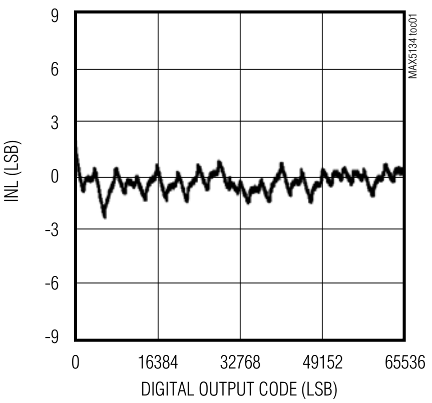


Figure 1. Serial-Interface Timing Diagram

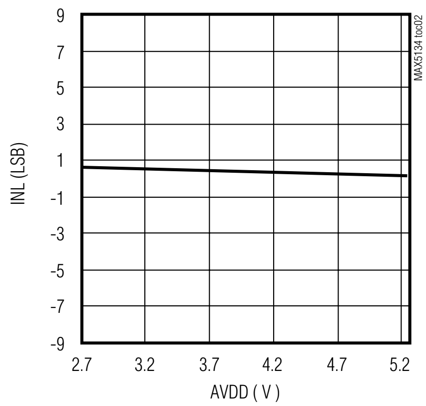
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

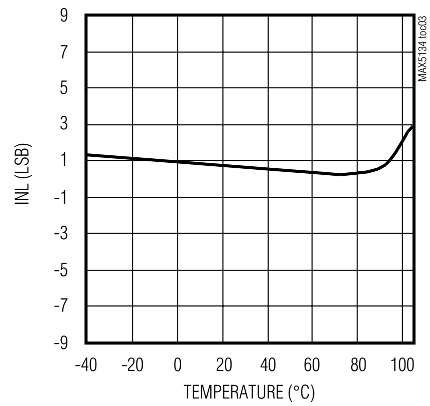
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



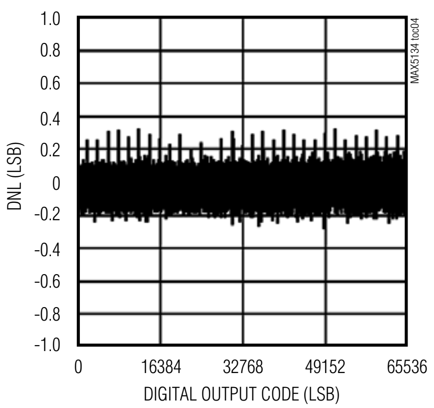
INTEGRAL NONLINEARITY vs. ANALOG SUPPLY VOLTAGE



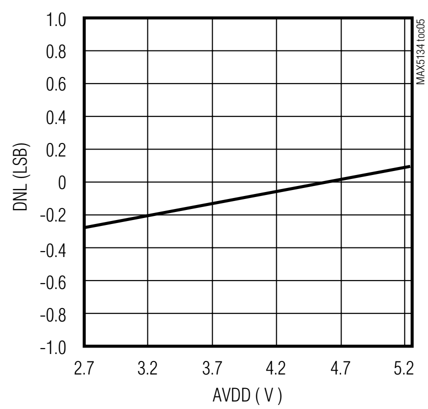
INTEGRAL NONLINEARITY vs. TEMPERATURE



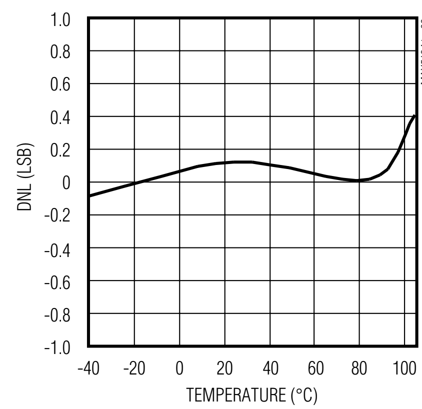
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



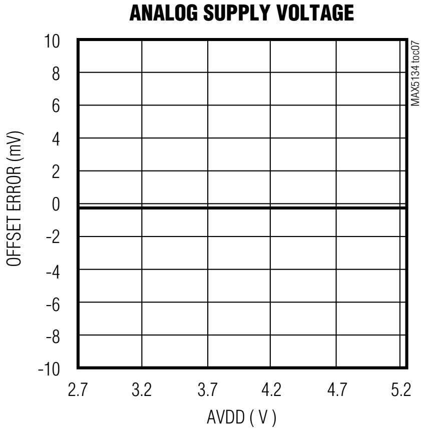
DIFFERENTIAL NONLINEARITY vs. ANALOG SUPPLY VOLTAGE



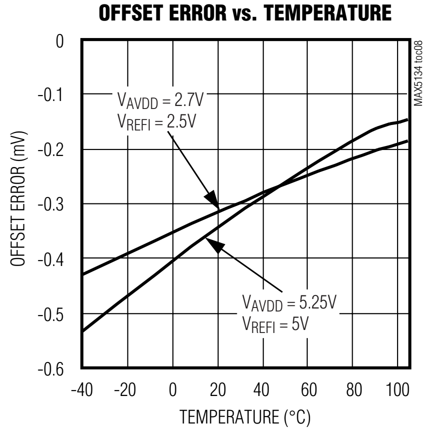
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



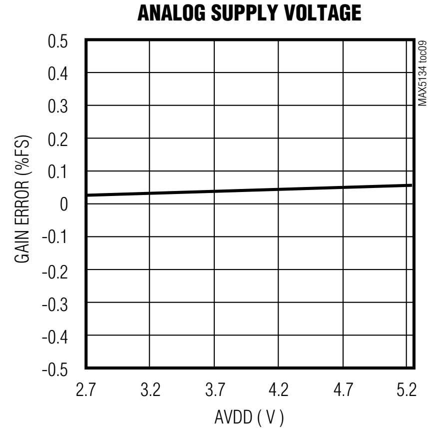
OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. ANALOG SUPPLY VOLTAGE

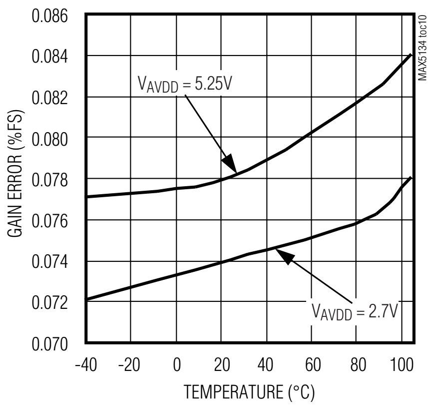


Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

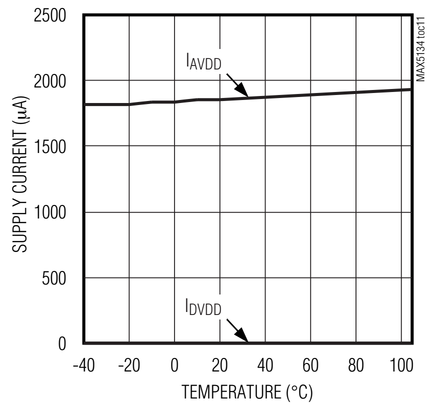
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

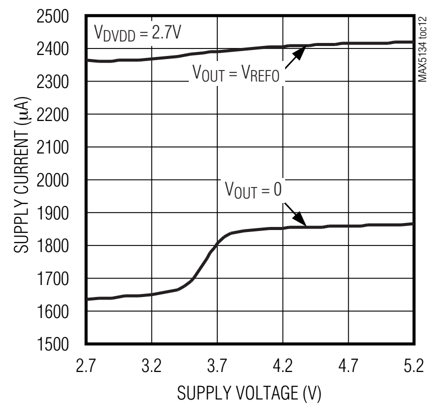
GAIN ERROR vs. TEMPERATURE



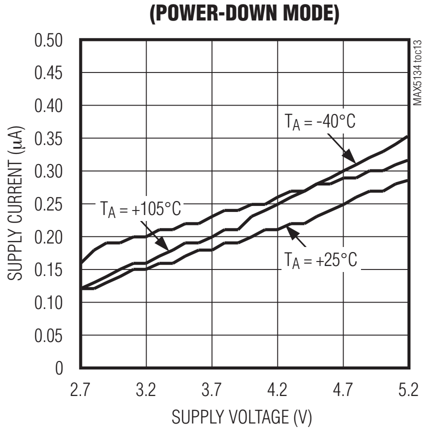
SUPPLY CURRENT vs. TEMPERATURE



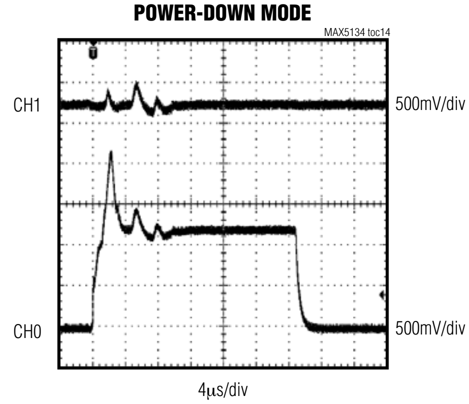
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



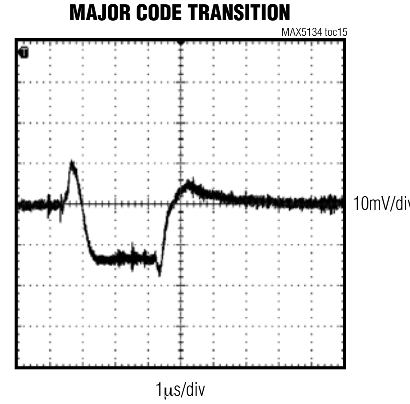
SUPPLY CURRENT vs. SUPPLY VOLTAGE (POWER-DOWN MODE)



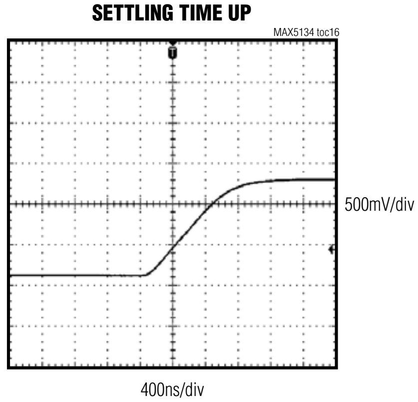
EXITING/ENTERING POWER-DOWN MODE



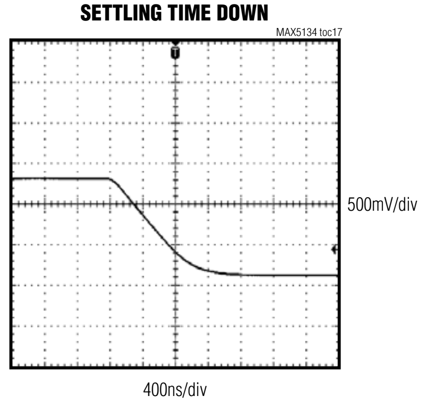
MAJOR CODE TRANSITION



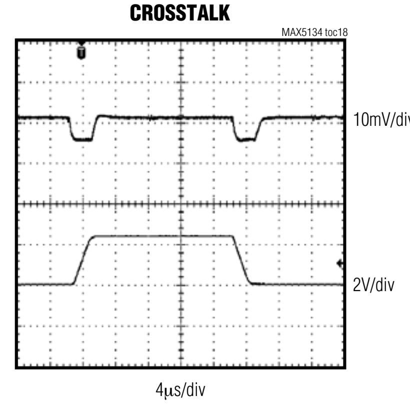
SETTLING TIME UP



SETTLING TIME DOWN



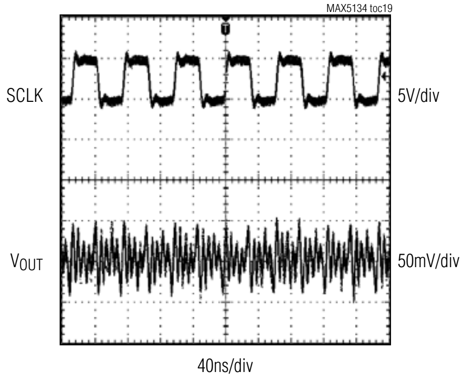
CROSSTALK



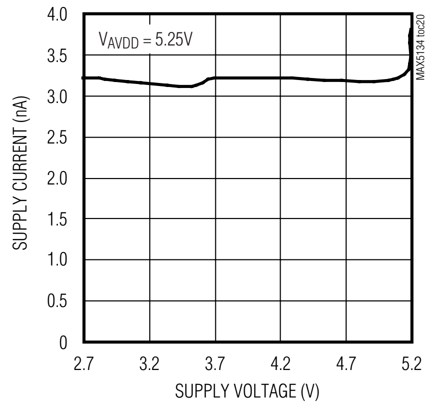
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

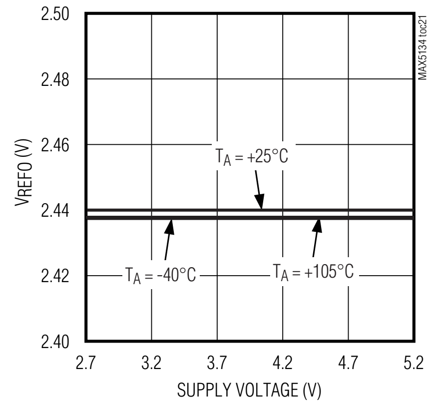
DIGITAL FEEDTHROUGH



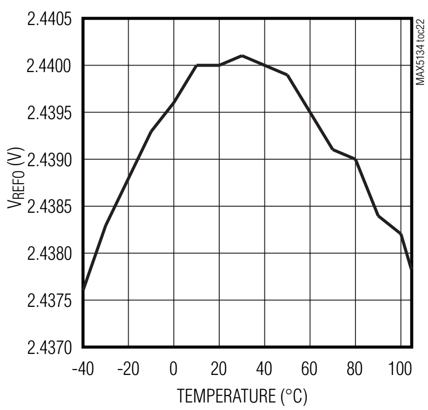
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



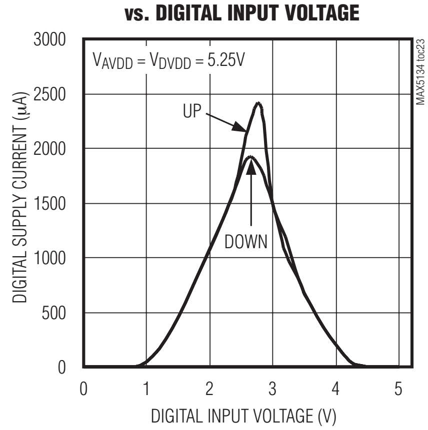
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



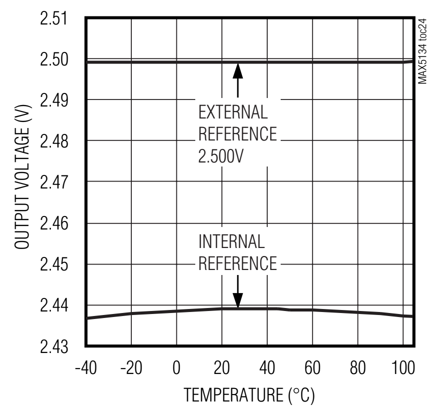
REFERENCE VOLTAGE vs. TEMPERATURE



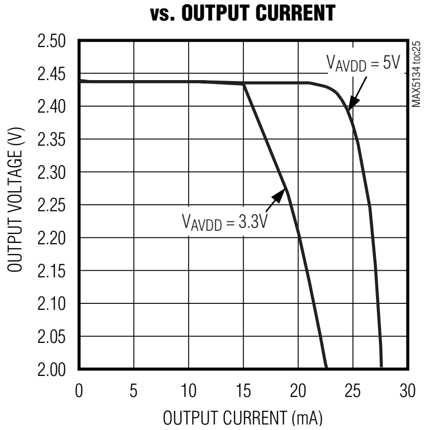
DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



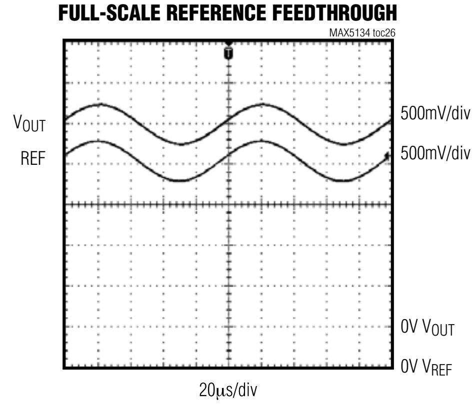
FULL-SCALE OUTPUT vs. TEMPERATURE



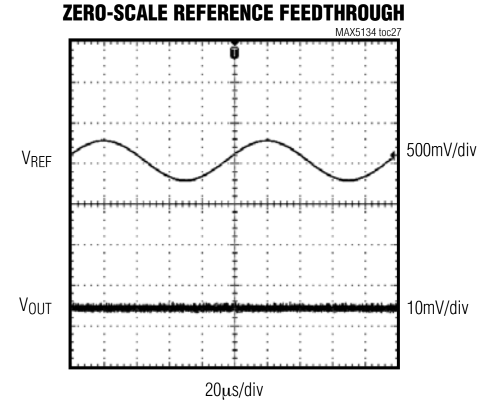
OUTPUT VOLTAGE vs. OUTPUT CURRENT



FULL-SCALE REFERENCE FEEDTHROUGH



ZERO-SCALE REFERENCE FEEDTHROUGH

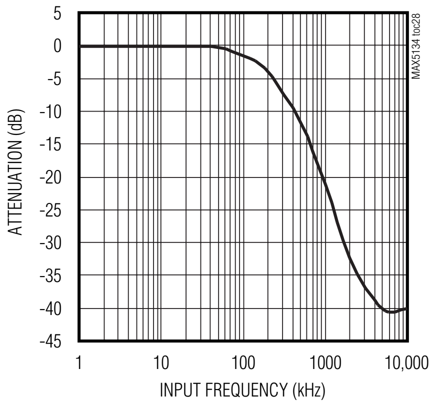


Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

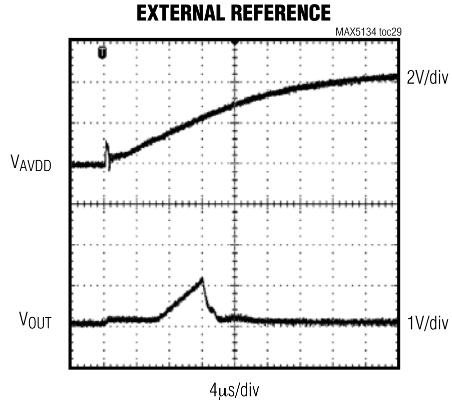
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

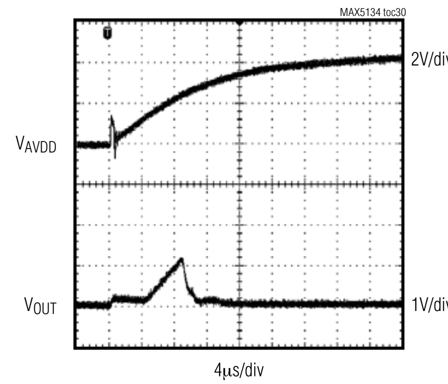
REFERENCE INPUT BANDWIDTH vs. FREQUENCY



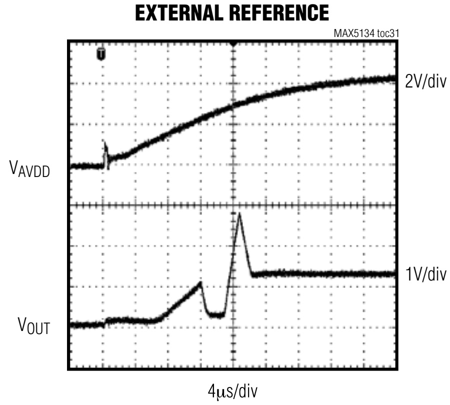
POWER-UP GLITCH, ZERO SCALE, EXTERNAL REFERENCE



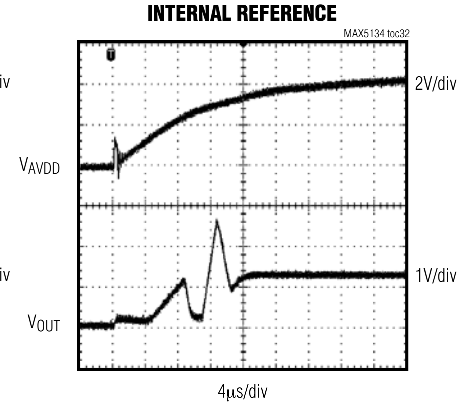
POWER-UP GLITCH, ZERO SCALE, INTERNAL REFERENCE



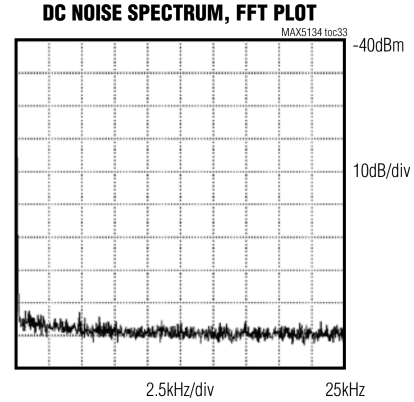
POWER-UP GLITCH, MIDSCALE, EXTERNAL REFERENCE



POWER-UP GLITCH, MIDSCALE, INTERNAL REFERENCE



DC NOISE SPECTRUM, FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1	OUT0	Channel 0 Buffered DAC Output
2, 5, 8, 11, 14, 17, 20, 23	N.C.	No Connection. Not internally connected.
3	DVDD	Digital Power Supply. Bypass DVDD with a 0.1μF capacitor to GND.
4	$\overline{\text{READY}}$	Active-Low Ready. Indicated configuration ready. Use $\overline{\text{READY}}$ as $\overline{\text{CS}}$ for consecutive part or as feedback to the μC.
6	OUT3	Channel 3 Buffered DAC Output
7, 19	GND	Ground
9	DIN	Data In
10	$\overline{\text{CS}}$	Active-Low Chip-Select Input
12	SCLK	Seria-Clock Input
13	OUT2	Channel 2 Buffered DAC Output
15	$\overline{\text{LDAC}}$	Load DAC Input. Active-low hardware load DAC input.
16	M/$\overline{\text{Z}}$	Power-Up Reset Select. Connect M/$\overline{\text{Z}}$ to DVDD to power up the DAC outputs to midscale. Connect M/$\overline{\text{Z}}$ to GND to power up the DAC outputs to zero.
18	OUT1	Channel 1 Buffered DAC Output
21	REFO	Reference Voltage Output
22	REFI	Reference Voltage Input. Bypass REFI with a 0.1μF capacitor to GND when using external reference.
24	AVDD	Analog Power Supply. Bypass AVDD with a 0.1μF capacitor to GND.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX5134 low-power, quad 16-bit, digital-to-analog converter (DAC) uses a precision internal reference or an external reference for rail-to-rail operation to provide high-linearity buffered voltage outputs. The MAX5134 minimizes the digital noise feedthrough from input to output by powering down the SCLK and DIN input buffers after completion of each 24-bit serial input. On power-up, the MAX5134 resets the DAC outputs to zero or midscale, depending on the state of the M/$\overline{\text{Z}}$ input, providing additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5134 contains a segmented resistor string-type DAC, a serial-in parallel-out shift register, a DAC register, power-on reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first. During power-down, an internal 80kΩ resistor pulls DAC outputs to GND.

Output Amplifiers (OUT0–OUT3)

The MAX5134 includes internal buffers for all DAC outputs. The internal buffers provide improved load regulation and transition glitch suppression for the DAC outputs. The output buffers slew at 1.25V/μs and drive up to 2kΩ in parallel with 200pF. The analog supply voltage (AVDD) determines the maximum output voltage range of the device as AVDD powers the output buffers.

DAC Reference

Internal Reference

The MAX5134 features an internal reference with a nominal output of +2.44V. Connect REFO to REFI when using the internal reference. Bypass REFO to GND with a 47pF (maximum 100pF) capacitor. Alternatively if heavier decoupling is required, use a 1kΩ series resistor with a 1μF capacitor to ground. REFO can deliver up to 100μA of current with no degradation in performance. Configure other reference voltages by applying a resistive potential divider with a total resistance greater than 33kΩ from REFO to GND.

External Reference

The external reference input features a typical input impedance of 113kΩ and accepts an input voltage from +2V to AVDD. Connect an external voltage supply between REFI and GND to apply an external reference. Leave REFO unconnected. Visit **www.maxim-ic.com/products/references** for a list of available external voltage-reference devices.

AVDD as Reference

Connect AVDD to REFI to use AVDD as the reference voltage. Leave REFO unconnected.

Serial Interface

The MAX5134 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSPs (Figures 2, 3). The interface provides three inputs, SCLK, $\overline{\text{CS}}$, and DIN and one output, $\overline{\text{READY}}$. Use $\overline{\text{READY}}$ to verify communication or to daisy-chain multiple devices (see the *$\overline{\text{READY}}$* section). $\overline{\text{READY}}$ is capable of driving a 20pF load with a 30ns (max) delay from the falling edge of SCLK. The chip-select input ($\overline{\text{CS}}$) frames the serial data loading at DIN. Following a chip-select input's high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 24 bits. The first 8 bits are the control word followed by 16 data bits (MSB first), as shown in Table 1. The serial input register transfers its contents to the input registers after loading 24 bits of data. To initiate a new data transfer, drive $\overline{\text{CS}}$ high, keep $\overline{\text{CS}}$ high for a minimum of 33ns before the next write sequence. The SCLK can be either high or low between $\overline{\text{CS}}$ write pulses. Figure 1 shows the timing diagram for the complete 3-wire serial-interface transmission.

The MAX5134 digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without effecting the DAC register(s) using the write command. To update the DAC registers, either pulse the $\overline{\text{LDAC}}$ input low to asynchronously update all DAC outputs, or use the software $\overline{\text{LDAC}}$ command. Use the write through commands (see Table 1) to update the DAC outputs immediately after the data is received. Only use the write through command to update the DAC output immediately.

Table 1. Operating Mode Truth Table

24-BIT WORD																		DESC	FUNCTION
CONTROL BITS								DATA BITS											
MSB																	LSB		
C7	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6–D0		
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP	No operation.
0	0	0	0	0	0	0	1	X	X	X	X	DAC 3	DAC 2	DAC 1	DAC 0	X	X	LDAC	Move contents of input to DAC registers indicated by 1's. No effect on registers indicated by 0's.
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	CLR	Software clear.
0	0	0	0	0	0	1	1	X	X	X	X	DAC 3	DAC 2	DAC 1	DAC 0	READY_EN	X	Power Control	Power down DAC's indicated by 1's. Set READY_EN = 1 to enable $\overline{\text{READY}}$.
0	0	0	0	0	1	0	1	0	0	0	0	0	0	LIN	0	0	0	Linearity	Optimize DAC linearity.
0	0	0	1	DAC 3	DAC 2	DAC 1	DAC 0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Write	Write to selected input registers (DAC output not affected).
0	0	1	1	DAC 3	DAC 2	DAC 1	DAC 0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Write Through	Write to selected input and DAC registers, DAC outputs updated (write through).
0	0	1	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP	No operation.

The 16-bit DAC code is unipolar binary with V_{OUT} = (code/65536) x V_{REF}. See Table 1 for the serial interface commands

Connect the MAX5134 DVDD supply to the supply of the host DSP or microprocessor. The AVDD supply may be set to any voltage within the operating range of 2.7V to 5.25V, but must be greater than or equal to the DVDD supply.

Writing to the MAX5134

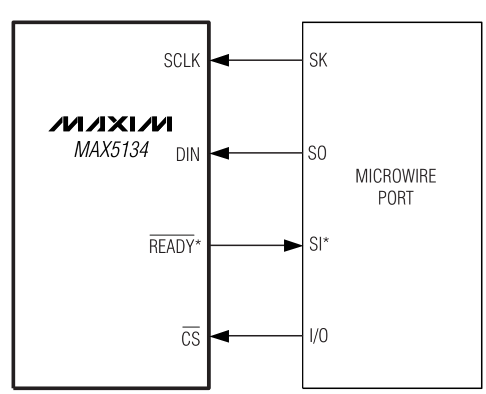
Write to the MAX5134 using the following sequence:

1) Drive $\overline{CS}$ low, enabling the shift register.
2) Clock 24 bits of data into DIN (C7 first and D0 last), observing the specified setup and hold times. Bits D15–D0 are the data bits that are written to the internal register.
3) After clocking in the last data bit, drive $\overline{CS}$ high. $\overline{CS}$ must remain high for 33ns before the next transmission is started.

Figure 1 shows a write operation for the transmission of 24 bits. If $\overline{CS}$ is driven high at any point prior to receiving 24 bits, the transmission is discarded.

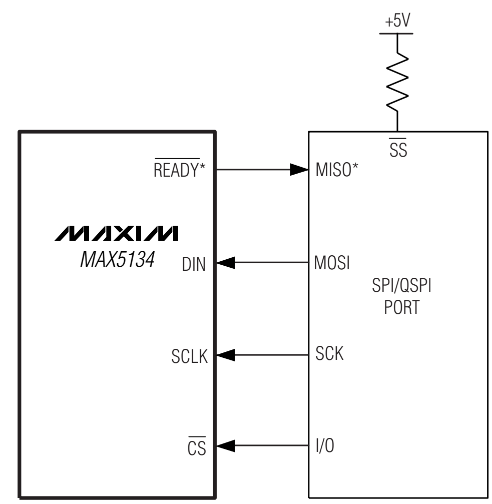
$\overline{READY}$

Connect $\overline{READY}$ to a microcontroller (µC) input to monitor the serial interface for valid communications. The $\overline{READY}$ pulse appears 24 clock cycles after the negative edge of $\overline{CS}$ (Figure 4). Since the MAX5134 looks at the first 24 bits of the transmission following the falling edge of $\overline{CS}$, it is possible to daisy chain devices with different command word lengths. $\overline{READY}$ goes high 16ns after $\overline{CS}$ is driven high.



*THE $\overline{READY}$-TO-SI CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX5134 BUT MAY BE USED FOR TRANSMISSION VERIFICATION.

Figure 2. Connections for MICROWIRE



*THE $\overline{READY}$-TO-MISO CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX5134 BUT MAY BE USED FOR TRANSMISSION VERIFICATION.

Figure 3. Connections for SPI/QSPI

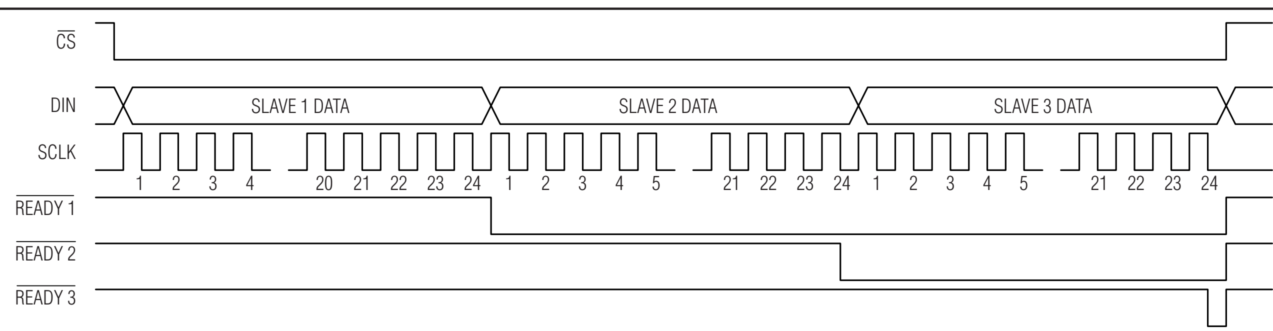


Figure 4. $\overline{READY}$ Timing

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

Daisy chain multiple MAX5134 devices by connecting the first device conventionally, then connect its READY output to the CS of the following device. Repeat for any other devices in the chain, and drive the SCLK and DIN lines in parallel (Figure 5). When sending commands to daisy-chained MAX5134s, the devices are accessed serially starting with the first device in the chain. The first 24 data bits are read by the first device, the second 24 data bits are read by the second device and so on (Figure 4). Figure 6 shows the configuration when CS is not driven by the µC.

To perform a daisy-chain write operation, drive CS low and output the data serially to DIN. The propagation of the READY signal then controls how the data is read by each device. As the data propagates through the daisy chain, each individual command in the chain is executed on the 24th falling clock edge following the falling edge of the respective CS input. To update just one device in a daisy chain, send the no-op command to the other devices in the chain.

If READY is not required, write command 0x03 (power control) and set READY_EN = 0 (see Table 1) to disable the READY output.

Clear Command

The MAX5134 features a software clear command (0x02). The software clear command acts as a software POR, erasing the contents of all registers. All outputs return to the state determined by the M/Z input.

Power-Down Mode

The MAX5134 features a software-controlled individual power-down mode for each channel. The internal reference and biasing circuits power down to conserve power when all 4 channels are powered down. In power-down, the outputs disconnect from the buffers and are grounded with an internal 80kΩ resistor. The DAC register holds the retained code so that the output is restored when the channel powers up. The serial interface remains active in power-down mode.

Load DAC (LDAC) Input

The MAX5134 features an active-low LDAC logic input that allows the outputs to update asynchronously. Keep LDAC high during normal operation (when the device is controlled only through the serial interface). Drive LDAC low to simultaneously update all DAC outputs with data from their respective input registers. Figure 7 shows the LDAC timing with respect to OUT_. Holding LDAC low causes the input registers to become transparent and data written to the DAC registers to immediately update the DAC outputs. A software command can also activate the LDAC operation. To activate LDAC by software, set control word 0x01 and data bits A11–A8 to select which DAC to load, and all other data bits to don't care. See Table 1 for the data format. This operation updates only the DAC outputs that are flagged with a "1". DAC outputs flagged with a "0" remain unchanged.

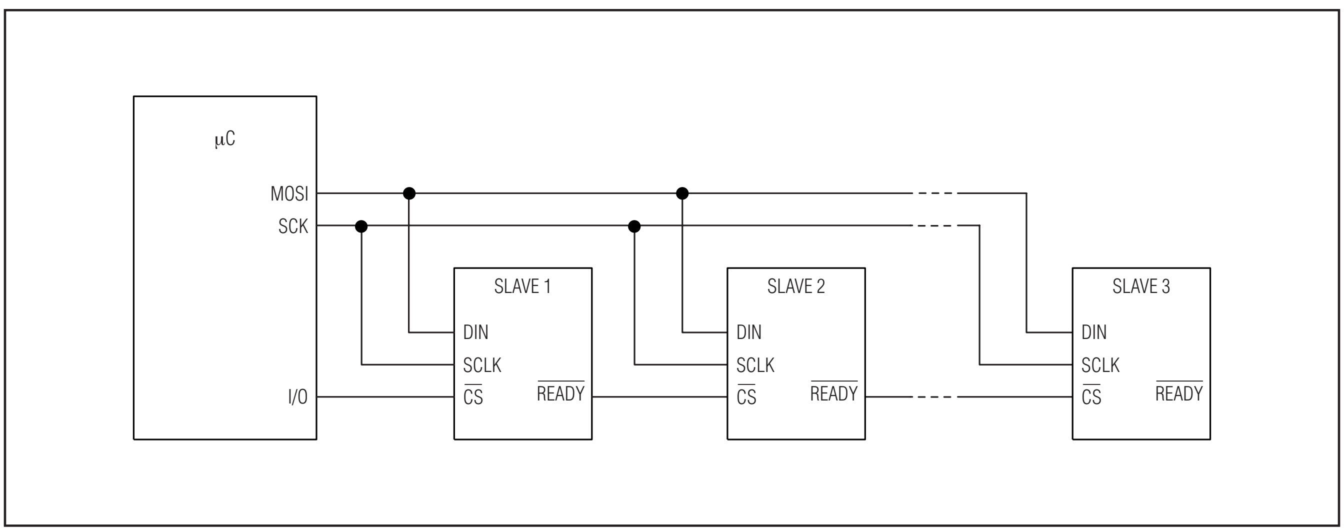


Figure 5. Daisy-Chain Configuration

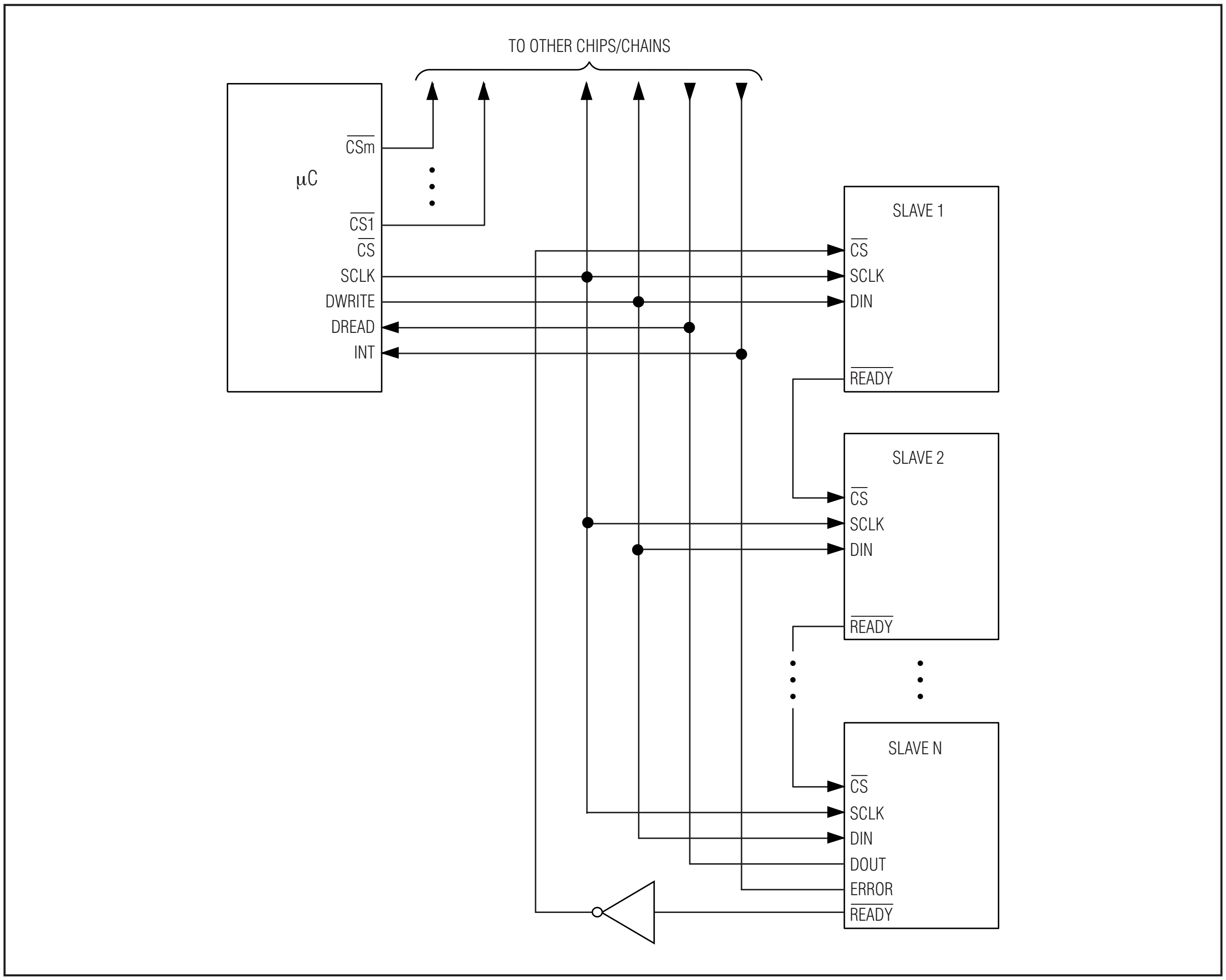


Figure 6. Daisy Chain (CS Not Used)

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

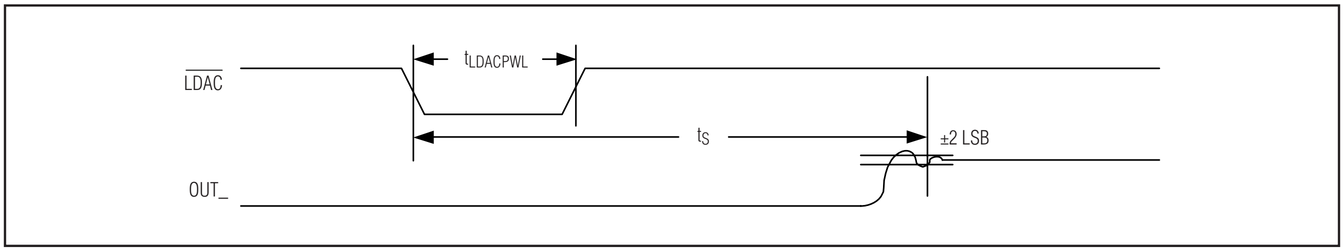


Figure 7. Output Timing

Applications Information

Power-On Reset (POR)

On power-up, the input registers are set to zero, DAC outputs power up to zero or midscale, depending on the configuration of M/$\overline{Z}$. Connect M/$\overline{Z}$ to GND to power the outputs to GND. Connect M/$\overline{Z}$ to AVDD to power the outputs to midscale.

To optimize DAC linearity, wait until the supplies have settled. Set the LIN bit in the DAC linearity register; wait 10ms, and clear the LIN bit.

Unipolar Output

The MAX5134 unipolar output voltage range is 0 to V_{REFI}. The output buffers each drive a load of 2kΩ in parallel with 200pF.

Bipolar Output

Use the MAX5134 in bipolar applications with additional external components (see the *Typical Operating Circuit*).

Power Supplies and Bypassing Considerations

For best performance, use a separate supply for the MAX5134. Bypass both DVDD and AVDD with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect both MAX5134 GND inputs to the analog ground plane.

Table 2. Input Code vs. Output Voltage

DAC LATCH CONTENTS MSB … LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535/65,536)
1000 0000 0000 0000	V_{REF} x (32,768/65,536) = 1/2 V_{REF}
0000 0000 0000 0001	V_{REF} x (1/65,536)
0000 0000 0000 0000	0

Layout Considerations

Digital and AC transient signals on GND inputs can create noise at the outputs. Connect both GND inputs to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5134 GND. Carefully lay out the traces between channels to reduce AC crosscoupling and crosstalk. Do not use wire-wrapped boards and sockets. Use shielding to improve noise immunity. Do not run analog and digital signals parallel to one another (especially clock signals) and avoid routing digital lines underneath the MAX5134 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a best fit straight line drawn between two codes. This best fit line is a line drawn between codes 3072 and 64,512 of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL is greater than -1 LSB, the DAC guarantees no missing codes and is monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero-scale point of the transfer function.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

Digital-to-Analog Glitch Impulse

A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

Digital-to-Analog Power-Up Glitch Impulse

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

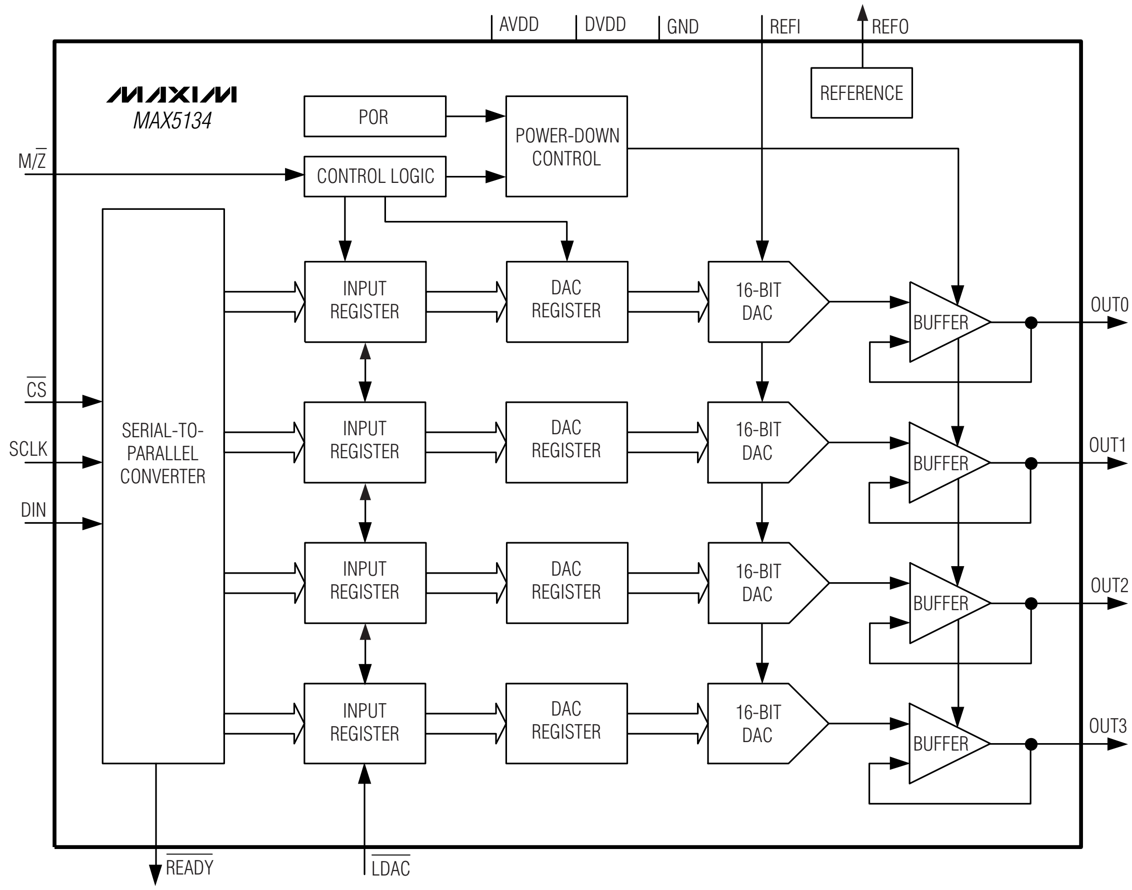
DC DAC-to-DAC Crosstalk

Crosstalk is the amount of noise that appears on a DAC output set to 0 when the other DAC is updated from 0 to AVDD

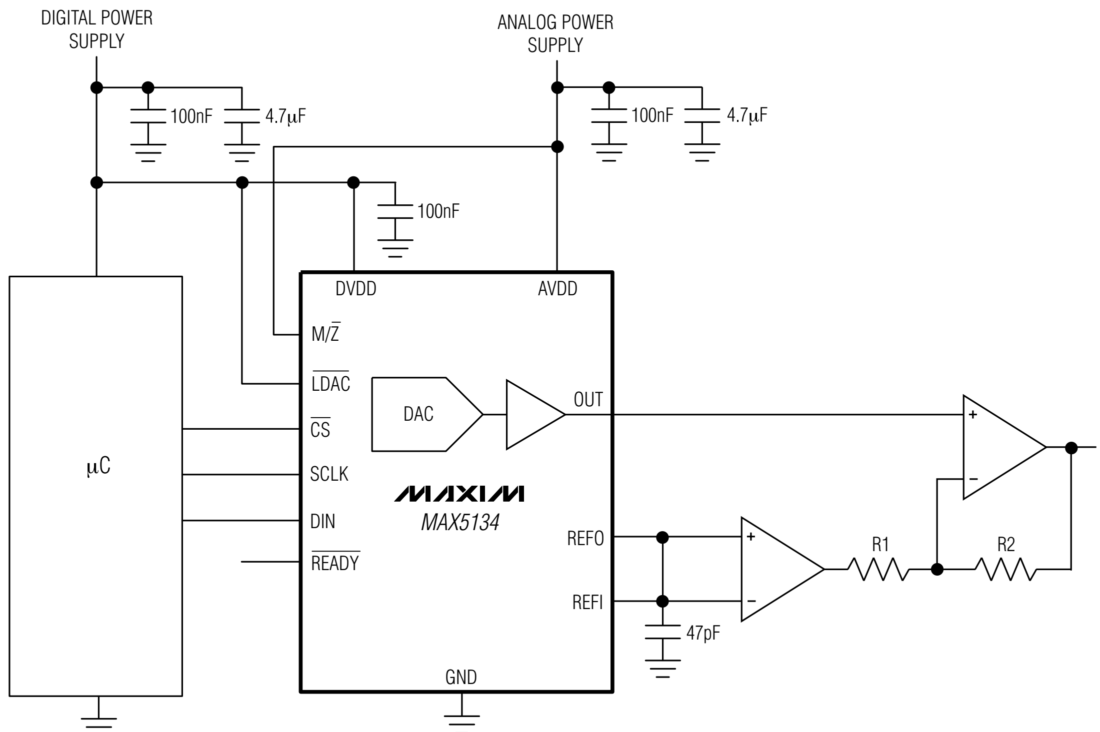
Chip Information

PROCESS: BiCMOS

Functional Diagram



Typical Operating Circuit



*SHOWN IN BIPOLAR CONFIGURATION

Low-Power, Quad 16-Bit, Buffered Voltage-Output DAC

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN	T2444-4	21-0139