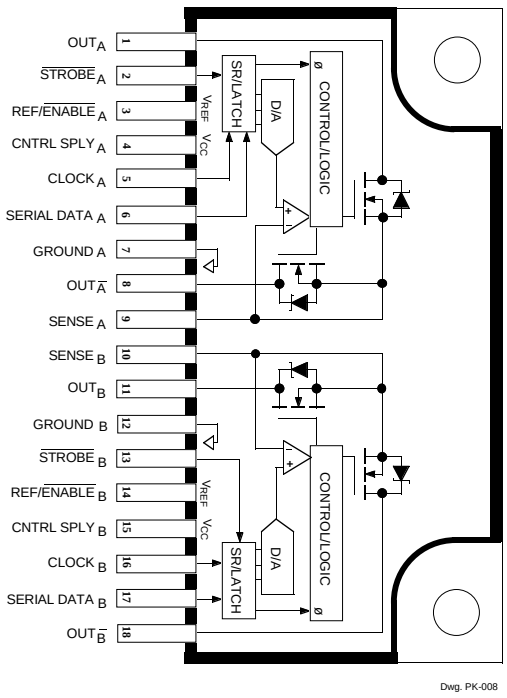
Motor Drivers

SLA7042M AND SLA7044M

Data Sheet 28202A†

MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVER



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ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} . . . . . **46 V**

FET Output Voltage, V_{DS} . . . . . **100 V**

Control Supply Voltage, V_{DD} . . . . . **7.0 V**

Peak Output Current,
I_{OUTM} ($t_w \le 10$ µs) . . . . . **5.0 A**

Continuous Output Current, I_{OUT}
SLA7042M . . . . . **1.5 A**
SLA7044M . . . . . **3.0 A**

Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**

Reference Voltage, V_{REF} . . . . . **V_{DD}**

Package Power Dissipation, P_D . **See Graph**

Junction Temperature, T_J . . . . . **+150°C**

Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**

Storage Temperature Range,
T_{stg} . . . . . **-40°C to +150°C**

The SLA7042M and SLA7044M are designed for high-efficiency and high-performance microstepping operation of 2-phase, unipolar stepper motors. Microstepping provides improved resolution without limiting step rates, and provides much smoother low-speed motor operation. An automated, innovative packaging technology combined with power NMOS FETs and monolithic CMOS logic/control circuitry advances power multi-chip modules (PMCMs™) toward the complete integration of motion control. Each half of these stepper motor controller/drivers operate independently. The 4-bit shift registers are serially loaded with motor phase information and output current-ratio data (eight levels). The combination of user-selectable current-sensing resistor, linearly adjustable reference voltage, and digitally selected output current ratio provides users with a broad, variable range of of full, half, and microstepping motor control ($I_{OUT} \approx [V_{REF}/3 \bullet R_S] \bullet$ Current Ratio).

Each PMCM is rated for a maximum motor supply voltage of 46 V and utilizes advanced NMOS FETs for the high-current, high-voltage driver outputs. The avalanche-rated (≥100 V) FETs provide excellent ON resistance, improved body diodes, and very-fast switching. The multi-chip ratings and performance afford significant benefits and advantages for stepper drives when compared to the higher dissipation and slower switching speeds associated with bipolar transistors. Highly automated manufacturing techniques provide low-cost and exceptionally reliable PMCMs suitable for controlling and directly driving a broad range of 2-phase, unipolar stepper motors. The SLA7042M and SLA7044M are identical except for $r_{DS(on)}$ and output current ratings.

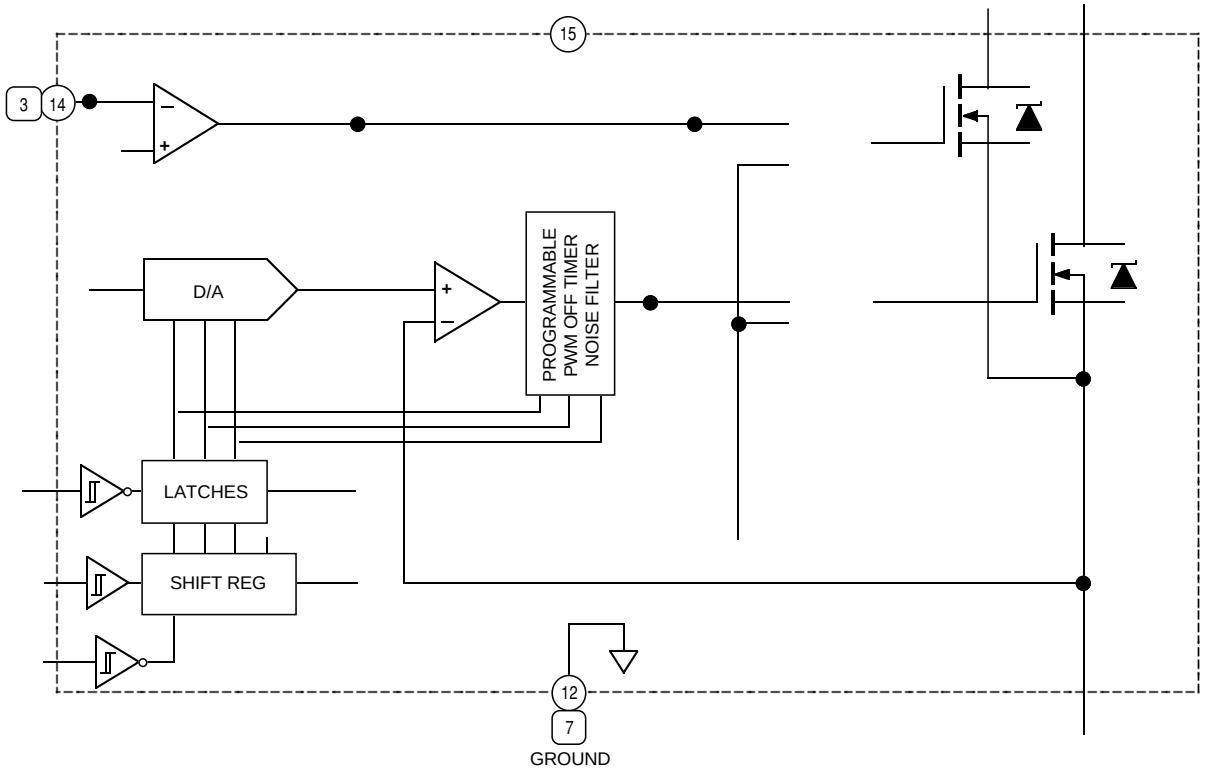
Complete applications information is given on the following pages. PWM current is regulated by appropriately choosing current-sensing resistors, a voltage reference, and digitally programmable current ratio. Inputs are compatible with 5 V logic and microprocessors.

BENEFITS AND FEATURES

- Cost-Effective, Multi-Chip Solution
- 'Turn-Key' Motion-Control Module
- Motor Operation to 3 A and 46 V
- 3rd Generation High-Voltage FETs
- 100 V, Avalanche-Rated NMOS
- Low $r_{DS(on)}$ NMOS Outputs
- Advanced, Improved Body Diodes
- Microstepping Unipolar Drive
- High-Efficiency, High-Speed PWM
- Independent PWM Current Control (2-Phase)
- Digitally Programmable PWM Current Control
- Low Component-Count PWM Drive
- Low Internal-Power Dissipation
- Electrically Isolated Power Tab
- Logic IC- and µP-Compatible Inputs
- Machine-Insertable Package

Always order by complete part number: **SLA7042M** .

FUNCTIONAL BLOCK DIAGRAM



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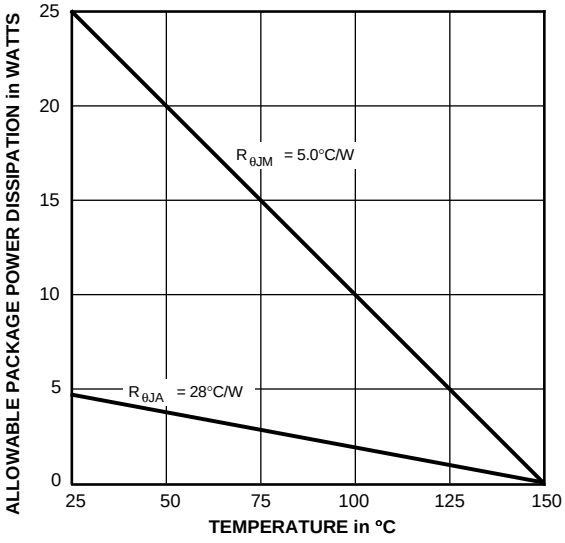
Note that channels A and B are electrically isolated.

ALLOWABLE PACKAGE POWER DISSIPATION



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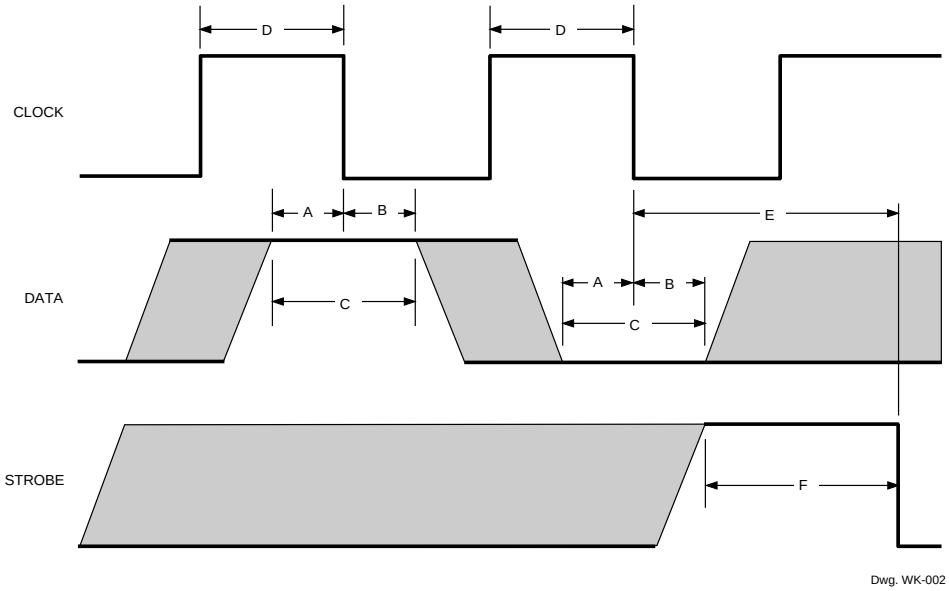
DC ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits			
			Min	Typ	Max	Units
FET Leakage Current	I_{DSS}	V_{DS} = 100 V	—	—	4.0	mA
FET ON Voltage	$V_{DS(ON)}$	SLA7042M, I_{OUT} = 1.2 A	—	—	800	mV
		SLA7044M, I_{OUT} = 3 A	—	—	855	mV
FET ON Resistance	$r_{DS(on)}$	SLA7042M, I_{OUT} = 1.2 A	—	—	0.67	Ω
		SLA7044M, I_{OUT} = 3 A	—	—	0.285	Ω
Body Diode Forward Voltage	V_{SD}	SLA7042M, I_{OUT} = –1.2 A	—	—	1.2	V
		SLA7044M, I_{OUT} = –3 A	—	—	1.6	V
Control Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Control Supply Current	I_{DD}	Each controller, V_{DD} = 5.5 V	—	—	7.0	mA
Logic Input Voltage	$V_{IN(1)}$		3.5	—	—	V
	$V_{IN(0)}$		—	—	1.5	V
Logic Input Current	$I_{IN(1)}$	$V_{IN(1)} = V_{DD}$	—	—	1.0	µA
	$I_{IN(0)}$	$V_{IN(0)}$ = 0	—	—	–1.0	µA
REF/ENABLE Input Voltage	$V_{REF/EN}$	DATA, CLOCK, STROBE, and OUT Enabled	0.4	—	2.5	V
		DATA, CLOCK, STROBE, and OUT Disabled	V_{DD} - 1	—	—	V
REF/ENABLE Input Current	$I_{REF/EN}$	0 V ≤ $V_{REF/EN}$ ≤ 5 V	—	—	±1.0	µA
Step Reference Current Ratio First Bit Entered (X) = Phase Second Bit Entered = LSB Last Bit Entered = MSB	SRCR	DATA Input = 000X	—	0	—	%
		DATA Input = 001X	—	20	—	%
		DATA Input = 010X	—	40	—	%
		DATA Input = 011X	—	55.5	—	%
		DATA Input = 100X	—	71.4	—	%
		DATA Input = 101X	—	83	—	%
		DATA Input = 110X	—	91	—	%
		DATA Input = 111X	—	100	—	%

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

TYPICAL AC CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, I_{OUT} = 1 A, Logic Levels are V_{DD} and Ground

PWM OFF Time		DATA Input = 001X	**7 µs**
		DATA Input = 010X	**7 µs**
		DATA Input = 011X	**9 µs**
		DATA Input = 100X	**9 µs**
		DATA Input = 101X	**9 µs**
		DATA Input = 110X	**11 µs**
		DATA Input = 101X	**11 µs**
Output RiseTime	t_r	10% to 90%	**0.5 µs**
Output Fall Time	t_f	90% to 10%	**0.1 µs**
Strobe-to-Output Switching Time	t_{pd}	50% to 50%	**0.7 µs**



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SERIAL PORT TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Falling Edge (Data Set-Up Time) ..... **150 ns**
B. Minimum Data Active Time After Clock Falling Edge (Data Hold Time) ..... **150 ns**
C. Minimum Data Pulse Width ..... **350 ns**
D. Minimum Clock Pulse Width ..... **350 ns**
E. Minimum Time Between Clock and Strobe Falling Edges ..... **650 ns**
F. Minimum Strobe Pulse Width ..... **500 ns**

APPLICATIONS INFORMATION

The SLA7042M and SLA7044M modules integrate two CMOS controller ICs and four NMOS FETs. Each half of the device operates independently, although the CLOCK inputs may be connected together and the STROBE inputs may be connected together. Pulling $V_{REF/EN}$ low (<2.5 V) allows the 4-bit shift registers to be serially loaded with motor phase and output currrent ratioing data.

The first bit selects the motor phase (logic high = Output A or B, logic low = Output A or B); the next three bits determine the motor current ratio (eight steps, 0% to 100%). The internal D/A converter, in conjunction with a current-sensing resistor and input reference voltage, completes the microstepping current control.

Pulling $V_{REF/EN}$ high (within 1 V of V_{DD}) resets the shift register and latches to turn the MOS drivers OFF and inhibits the serial DATA input.

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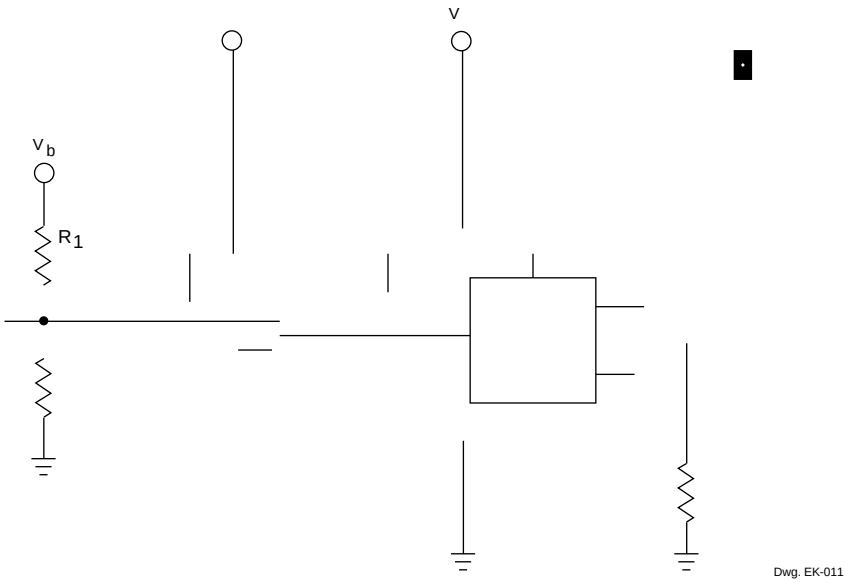

FIGURE 2. PWM CONTROL (RUN MODE)

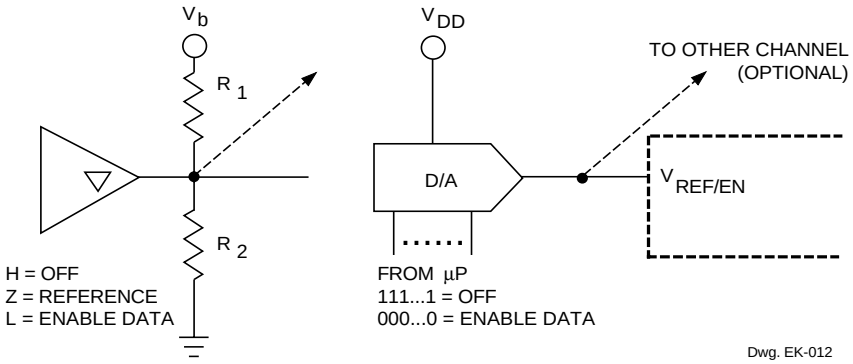

FIGURE 3. COMPLETE CONTROL

SERIAL DATA INPUT

The serial DATA input port is enabled (active low) by the REFERENCE/ENABLE input. When $V_{REF/EN}$ is between 0.4 V and 2.5 V, information on the DATA input is read into the shift register on each high-to-low transition of the CLOCK.

There are four bits: the first bit entered controls the motor phase — a high level enables OUT_A or OUT_B, a low level enables $OUT_{\overline{A}}$ or $OUT_{\overline{B}}$. The next three bits set the step reference voltage ratio and PWM OFF time as shown in the Characteristics Tables — the least-significant bit first and the most-significant bit last.

Data written into the serial data port is latched and becomes active on a high-to-low transition at STROBE.

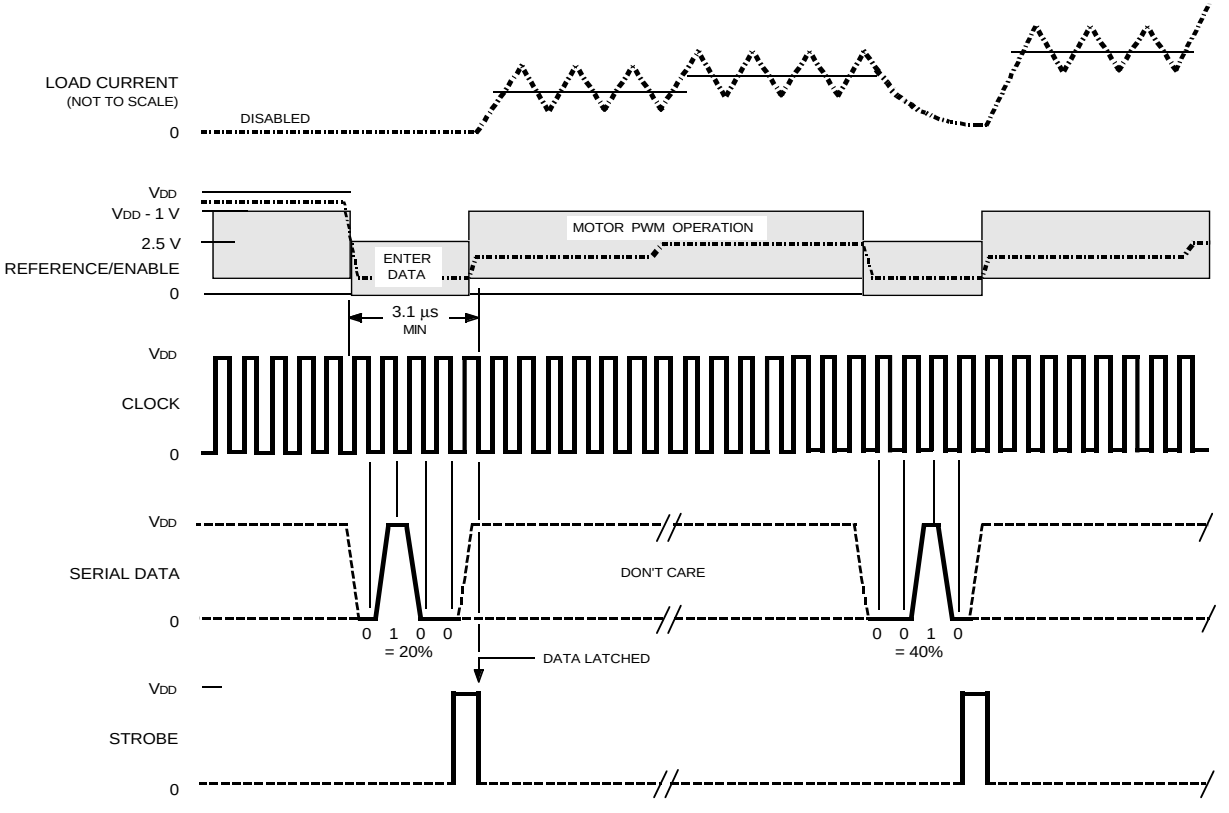

FIGURE 4. TIMING RELATIONSHIPS

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REFERENCE/ENABLE INPUT

The serial DATA input port is enabled (active low) by the REFERENCE/ENABLE input when $V_{REF/EN}$ is between 0.4 V and 2.5 V.

With $V_{REF/EN}$ greater than V_{DD} - 1 V, the serial DATA input port is disabled, the outputs are OFF, the internal logic is reset, and the controller/driver will not be affected by changes at the DATA, CLOCK, or STROBE inputs.

With $V_{REF/EN}$ between 0.4 V and 2.5 V, the output current limit is a linear function of V_{REF} and the step reference current ratio.

$$I_{OUT} \approx \frac{V_{REF}}{3 \bullet R_S} \bullet SRCR$$

In a typical (SLA7042M) application where V_{DD} = 5 V, a $V_{REF/EN}$ between 0.4 V and 2.5 V, and a maximum allowable load current of 1.2 A, the maximum value of R_S is 0.69 Ω and I_{OUT}min is 0.11 A when SRCR is 100% (DATA input = 111X).

POWER DISSIPATION CALCULATIONS

The SLA7042/44M normally do not require special heat sinking except under unusual circumstances (two phases operating near maximum output current and T_A >65°C). However, as with all power drivers, the basic constituents of power dissipation should be evaluated. Conduction losses (internal power dissipation) include:

(a) FET output power dissipation ($I_{OUT}^2 \bullet r_{DS(on)}$ or $I_{OUT} \bullet V_{DS(ON)}$),
(b) FET body diode power dissipation ($V_{SD} \bullet I_{OUT}$), and
(c) control circuit power dissipation ($V_{DD} \bullet I_{DD}$).

PACKAGE RATINGS/DERATING FACTORS

Thermal calculations must also consider the temperature effects on the output FET ON resistance. The applicable thermal ratings for the 18-lead power-tab SIP PMCM package are:

$R_{\theta JA}$ = 28°C/W (junction to ambient with no heat sink) or 4.5 W at +25°C and a derating factor of -36 mW/°C for operation above +25°C.
$R_{\theta JM}$ = 5°C/W (junction to mounting surface).

TEMPERATURE EFFECTS ON FET $r_{DS(on)}$

Analyzing safe, reliable operation includes a concern for the relationship of NMOS ON resistance to junction temperature. Device package power calculations must include the increase in ON resistance (producing higher output ON voltages) caused by higher operating junction temperatures. Figure 5 provides a normalized ON resistance curve, and all thermal calculations should consider increases from the given +25°C limits, which may be caused by internal heating during normal operation.

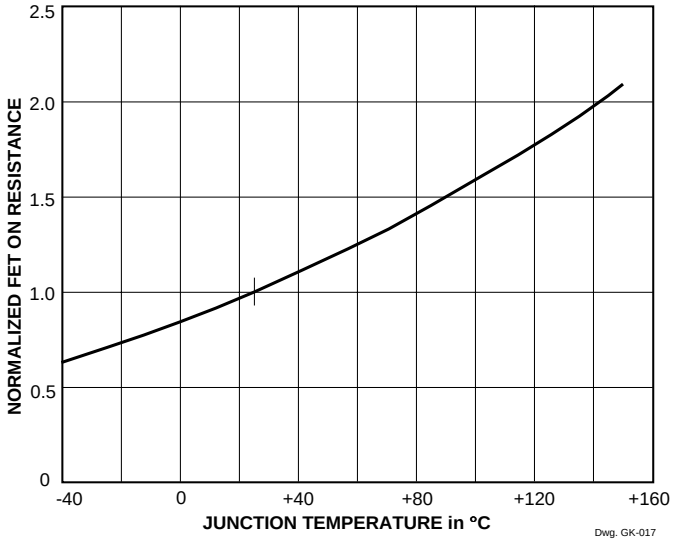
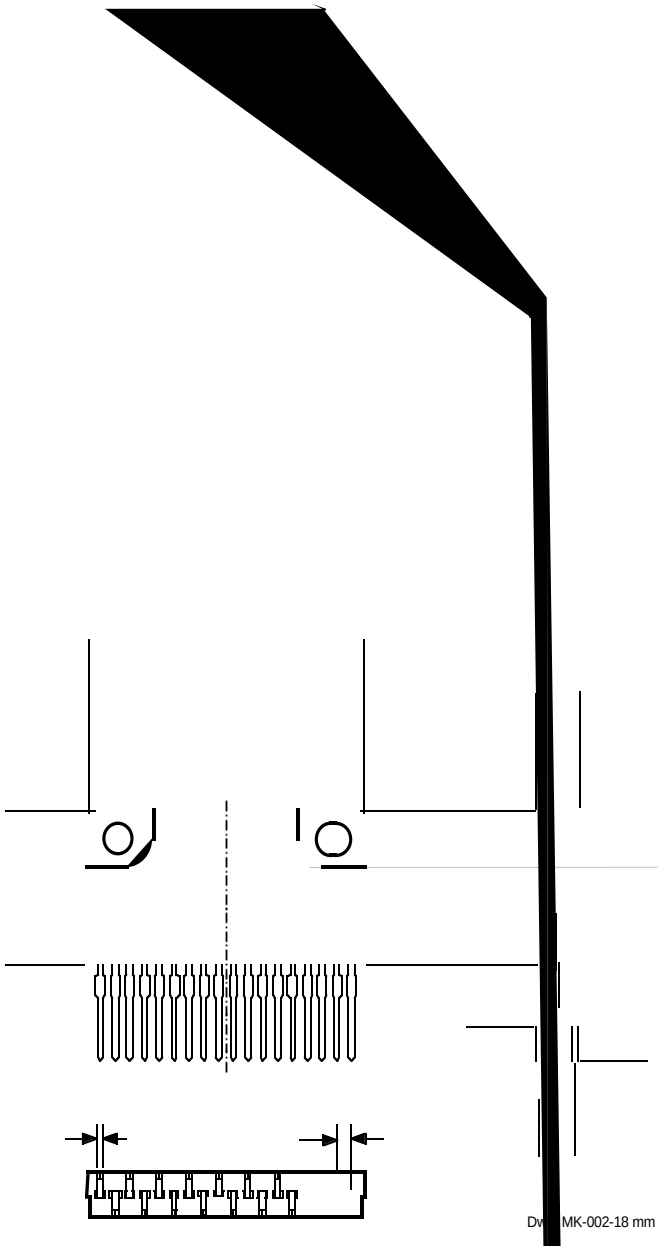


FIGURE 5. NORMALIZED ON RESISTANCE vs TEMPERATURE

The power MOSFET outputs of these devices are similar to the International Rectifier type IRL510 (SLA7042M) and IRL520 (SLA7044M). These devices feature an excellent combination of fast switching, ruggedized device design, low on-resistance, and cost effectiveness.

SLA7042M AND SLA7044M
MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS

Motor Drivers



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