FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16916-2E

32-bit Microcontrollers

CMOS

FR80 MB91665 Series

MB91F669/F668/V650

■ DESCRIPTION

The MB91665 series is a line of Fujitsu microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.
This series is based on the FR80* family CPU and is implemented as a single chip.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Semiconductor Limited.

■ FEATURES

- FR80 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - General-purpose registers : 32-bit × 16
  - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
  - Instructions suitable for embedded applications
    - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
    - Instruction support for high level languages
      Function entry and exit instructions, instructions for register multi-load and multi-store
    - Bit search instruction
      “1” detection, “0” detection, transition point detection
    - Branch instructions with delay slots
      Reduced overhead when processing branches
    - Register interlock functions
      Facilitate coding in assembly language
    - Built-in multiplier/instruction-level support
      - Signed 32-bit multiplication : 5 cycles
      - Signed 16-bit multiplication : 3 cycles
    - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
    - Harvard architecture allowing program access and data access to be executed simultaneously
    - The prefetch function for instructions using the 4-word instruction queue in the CPU

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For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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- Instruction compatible with FR family CPU
  - Additional bit search instructions
  - No resource instructions and coprocessor instructions

- Maximum operating frequency
  - CPU : 33 MHz
  - Resources : 33 MHz
  - External bus : 33 MHz

- External bus interface
  - Operating frequency : Max 33 MHz
  - MB91F669 (64 pins)
    24 addresses, 8/16-bit data I/O (multiplex bus)
    8 addresses, 8/16-bit data I/O (split bus)
  - MB91F668 (48 pins)*
    16 addresses, 8-bit data I/O (multiplex bus)
    No address, 8-bit data I/O (split bus)
    * There are no RDY, SYSCLK, $\overline{WR1}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$
  - 24 address lines, 8- or 16-bit data I/O (separate busses or multiplexed bus)
  - Programmable automatic wait cycle insertion for each area

- DMA controller (DMAC)
  - 4 channels
  - Address space : 32 bits (4 Gbytes)
  - Transfer modes : Block transfer/burst transfer/demand transfer
  - Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
  - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
  - Block size : 1 to 16
  - Number of transfers : 1 to 65535
  - Transfer requests
    - Requests from software
    - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
  - Reload functions : Reload can be specified on all channels
  - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
  - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.

- Multifunction serial interface
  - Operation mode is selectable from UART/CSIO/I^2C for each channel
  - UART
    - Full-duplex double buffer
    - Selectable parity on/off
    - Built-in dedicated baud rate generator
    - External clock can be used as a serial clock
    - Error detection function for parity, frame and overrun errors
  - CSIO
    - Full-duplex double buffer
    - Built-in dedicated baud rate generator
    - Overrun error detection function
  - I^2C
    - Supports both standard mode (Max 100 kbps) and Fast mode (Max 400 kbps)
    - Some channels are 5 V tolerant

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- Interrupts
  - Total of 16 external interrupts (some pins are 5 V tolerant)
  - Interrupts from peripheral resources
  - Programmable interrupt levels (16 levels)
  - Can be used to return from stop mode, sleep mode

- A/D converter
  - MB91F669 (64 pins): 12 channels, 1 unit
  - MB91F668 (48 pins): 10 channels, 1 unit
  - 10-bit resolution
  - Conversion time : approx. 1.2 μs (PCLK = 33 MHz)
  - Priority conversion (2 levels)
  - Conversion modes : Single-shot conversion mode, scan conversion mode
  - Activation sources : Software, external trigger, base timer
  - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)

- Base timer
  - 4 channels
  - Operation mode is selectable from the followings for each channel
    - 16/32-bit reload timer
    - 16-bit PWM timer
    - 16/32-bit PWC timer
    - 16-bit PPG timer
  - Cascading connection between 2 channels allows them to be used as one 32-bit timer
  - Multiple channels can be started simultaneously
  - Input/output select function

- 16-bit reload timer
  - 3 channels (including 1 channel for REALOS)
  - Interval timer function
  - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)

- Compare timer
  - 32-bit input capture : 8 channels
  - 32-bit output compare : 8 channels
  - 32-bit free-run timer : 2 channels

- Other interval timers
  - Up/down counter : 1 channel
  - Watch counter : 1 channel
  - Watchdog timer : 1 channel

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- USB function / HOST
  - 1 channel
  - USB2.0 Full-Speed supported
  - The USB function and USB HOST are the switch types (USB I/O multiplexed)
  - Support of DMA transfer

  [USB Function]
  - Support of up to four endpoints
    - Endpoint 0 is provided for the fixed use of control transfers
    - Bulk or interrupt transfer can be selected for endpoint 1 to 3
  - Double buffer structure for endpoint 1 to 3

  [USB HOST]
  - Support control transfer, bulk transfer, interrupt transfer, and isochronous transfer
  - Automatic detection of connection/disconnection of USB devices
  - Automatic processing of a handshake packet for IN/OUT token processing
  - Support of a maximum packet length of up to 256 bytes
  - Support for a wakeup function

- Main timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the main clock (MCLK)
  - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
  - Can be used as an interval timer while the main clock (MCLK) oscillations is stable

- Sub timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
  - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable

- Clock generation
  - Main clock (MCLK) oscillator
  - Sub clock (SBCLK) oscillator
  - PLL clock (PLLCLK) oscillator

- Low-power dissipation mode
  - Stop mode
  - Watch mode
  - Sleep mode
  - Doze mode
  - Clock division function

- Other features
  - I/O port
  - $\overline{\text{INIT}}$ pin is provided as a reset pin
  - Watchdog timer reset, software reset
  - Delay interrupt
  - Power supply

    Single power supply (When USB not used: 2.7 V to 3.6 V, When USB used: 3.0 V to 3.6 V)

■ PRODUCT LINEUP

Parameter \ Part number		MB91F669	MB91F668
Product type		Flash memory product	
Built-in program memory capacity		128 Kbytes (Flash)	
Built-in RAM capacity		16 Kbytes	
External bus interface	multi	Address: 24 bits Data: 16/8 bits	Address: 16 bits Data: 8 bits
	split	Address: 8 bits Data: 16/8 bits	No address Data: 8 bits
DMA controller (DMAC)		4 channels	
Base timer		4 channels (Reload timer/ PWM/ PPG/ PWC modes can be switched)	
Multifunction serial interface		4 channels (UART/ SPI/ I^2C modes can be switched)	
External interrupt		16	
10-bit A/D converter		12 channels (1 unit)	10 channels (1 unit)
16-bit reload timer		3 channels	
Compare timer		32-bit input capture: 8 channels 32-bit output compare: 8 channels 32-bit free-run timer: 2 channels	
Up/Down counter		1 channel	
Watch counter		1 channel	
I/O port		50	34
USB function/HOST		1 channel (function/ host modes can be switched)	
Main timer		1 channel	
Sub timer		1 channel	
Wild register		16 channels	
Debug function		—	

■ PACKAGES

Package \ Product name	MB91F669	MB91F668
FPT-64P-M24	○	—
FPT-48P-M26	—	○

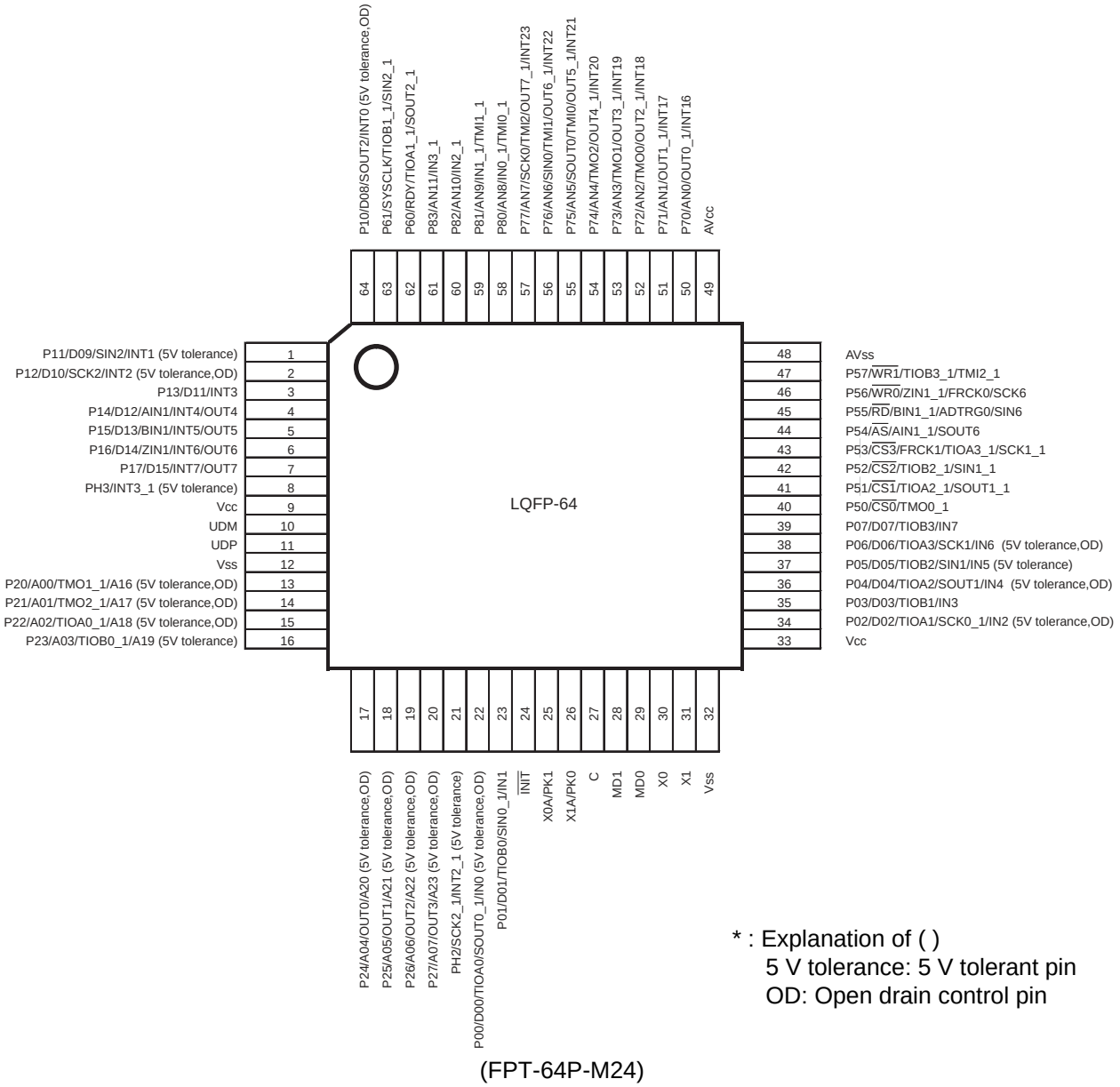
○ : Supported

Note: Refer to “■ PACKAGE DIMENSIONS” for detailed information on each package.

■ PIN ASSIGNMENT

• LQFP-64 (MB91F669)

(TOP VIEW)



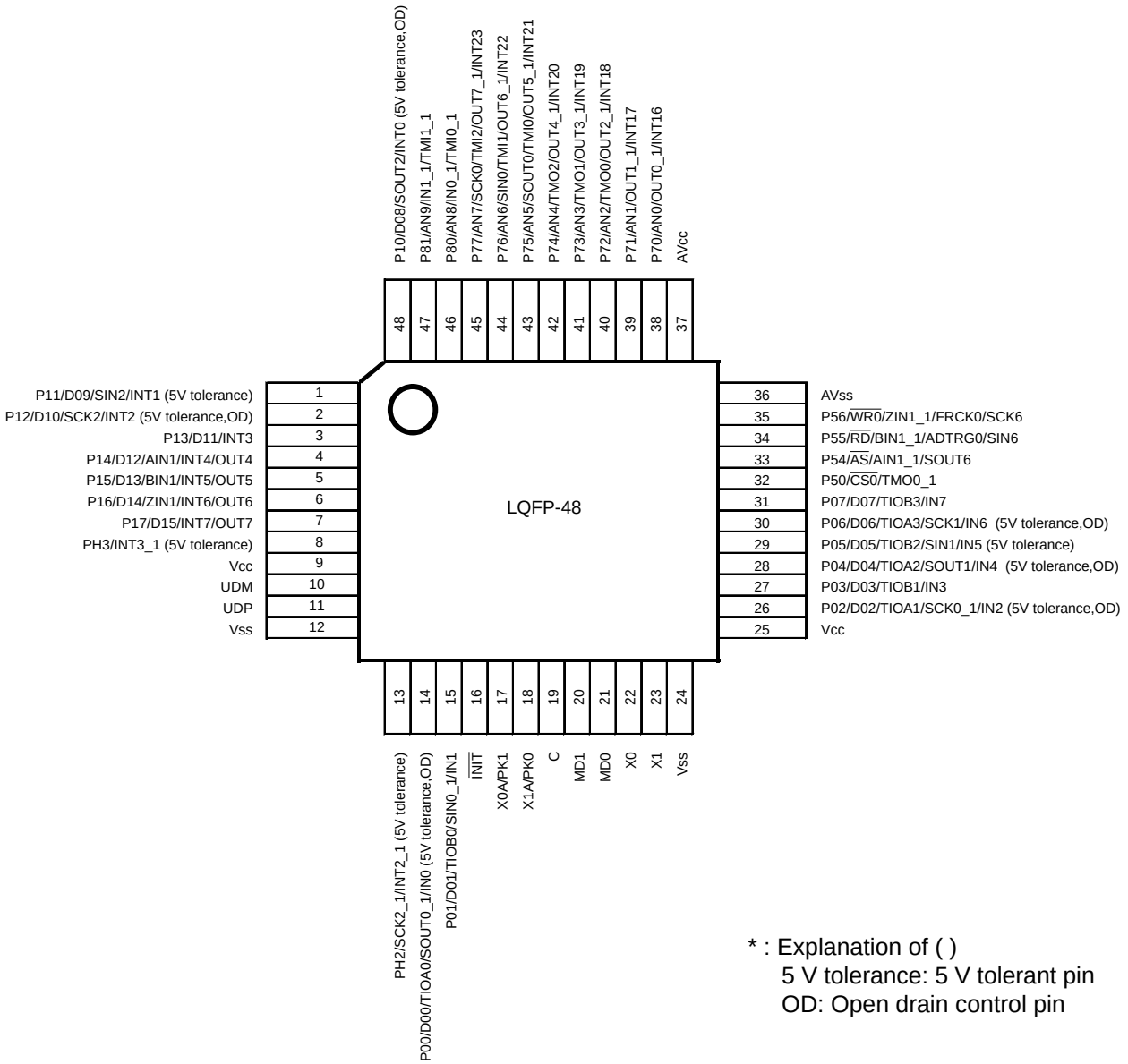
* : Explanation of ( )
5 V tolerance: 5 V tolerant pin
OD: Open drain control pin

(FPT-64P-M24)

Note : The number after the underscore (“_”) in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

• LQFP-48 (MB91F668)

(TOP VIEW)



* : Explanation of ( )
5 V tolerance: 5 V tolerant pin
OD: Open drain control pin

(FPT-48P-M26)

Note : The number after the underscore (“_”) in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin

Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
1	1	P11	Q*2	General-purpose I/O port	—	○
		D09		External bus interface data bus bit9	○	—
		SIN2		Multifunction serial interface ch.2 input pin	—	○
		INT1		External interrupt request 1 input pin	—	○
2	2	P12	Q*2	General-purpose I/O port	—	○
		D10		External bus interface data bus bit10	○	—
		SCK2 (SCL2)		Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I²C (operation mode 4).	—	○
		INT2		External interrupt request 2 input pin	—	○
3	3	P13	B	General-purpose I/O port	—	○
		D11		External bus interface data bus bit11	○	—
		INT3		External interrupt request 3 input pin	—	○
4	4	P14	B	General-purpose I/O port	—	○
		D12		External bus interface data bus bit12	○	—
		AIN1		Up/Down counter ch.1 AIN input pin	—	○
		INT4		External interrupt request 4 input pin	—	○
		OUT4		32-bit output compare ch.4 output pin	—	—
5	5	P15	B	General-purpose I/O port	—	○
		D13		External bus interface data bus bit13	○	—
		BIN1		Up/Down counter ch.1 BIN input pin	—	○
		INT5		External interrupt request 5 input pin	—	○
		OUT5		32-bit output compare ch.5 output pin	—	○
6	6	P16	B	General-purpose I/O port	—	○
		D14		External bus interface data bus bit14	○	—
		ZIN1		Up/Down counter ch.1 ZIN input pin	—	○
		INT6		External interrupt request 6 input pin	—	○
		OUT6		32-bit output compare ch.6 output pin	—	○

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Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
7	7	P17	B	General-purpose I/O port	—	○
		D15		External bus interface data bus bit15	○	—
		INT7		External interrupt request 7 input pin	—	○
		OUT7		32-bit output compare ch.7 output pin	—	○
8	8	PH3	D*2	General-purpose I/O port	—	○
		INT3_1		External interrupt request 3 input pin (Port 1)	—	○
9	9	V_{CC}	—	Power pin	—	—
10	10	UDM	USB	D− pin of USB function/HOST	—	—
11	11	UDP	USB	D+ pin of USB function/HOST	—	—
12	12	V_{SS}	—	GND pin	—	—
13	—	P20	Q*2	General-purpose I/O port	—	○
		A00		External bus interface address bus bit0	—	—
		TMO1_1		16-bit reload timer ch.1 output pin (Port 1)	—	○
		A16		External bus interface address bus bit16	—	—
14	—	P21	Q*2	General-purpose I/O port	—	○
		A01		External bus interface address bus bit1	—	—
		TMO2_1		16-bit reload timer ch.2 output pin (Port 1)	—	○
		A17		External bus interface address bus bit17	—	—
15	—	P22	Q*2	General-purpose I/O port	—	○
		A02		External bus interface address bus bit2	—	—
		TIOA0_1		Base timer ch.0 TIOA pin (Port 1)	—	○
		A18		External bus interface address bus bit18	—	—
16	—	P23	Q*2	General-purpose I/O port	—	○
		A03		External bus interface address bus bit3	—	—
		TIOB0_1		Base timer ch.0 TIOB pin (Port 1)	—	○
		A19		External bus interface address bus bit19	○	—
17	—	P24	Q*2	General-purpose I/O port	—	○
		A04		External bus interface address bus bit4	—	—
		OUT0		32-bit output compare ch.0 output pin	—	—
		A20		External bus interface address bus bit20	—	—

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Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
18	—	P25	Q*2	General-purpose I/O port	—	○
		A05		External bus interface address bus bit5	—	—
		OUT1		32-bit output compare ch.1 output pin	—	—
		A21		External bus interface address bus bit21	—	—
19	—	P26	Q*2	General-purpose I/O port	—	○
		A06		External bus interface address bus bit6	—	—
		OUT2		32-bit output compare ch.2 output pin	—	—
		A22		External bus interface address bus bit22	—	—
20	—	P27	Q*2	General-purpose I/O port	—	○
		A07		External bus interface address bus bit7	—	—
		OUT3		32-bit output compare ch.3 output pin	—	—
		A23		External bus interface address bus bit23	—	—
21	13	PH2	D*2	General-purpose I/O port	—	○
		SCK2_1 (SCL2_1)		Multifunction serial interface ch.2 clock I/O pin (Port 1). This pin operates as SCK2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2_1 when it is used in an I²C (operation mode 4).	—	○
		INT2_1		External interrupt request 2 input pin (Port 1)	—	○
22	14	P00	Q*2	General-purpose I/O port	—	○
		D00		External bus interface data bus bit0	○	—
		TIOA0		Base timer ch.0 TIOA pin	—	—
		SOUT0_1 (SDA0_1)		Multifunction serial interface ch.0 output pin (Port 1). This pin operates as SOUT0_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0_1 when it is used in an I²C (operation mode 4).	—	—
		IN0		32-bit input capture ch.0 input pin	—	○
23	15	P01	B	General-purpose I/O port	—	○
		D01		External bus interface data bus bit1	○	—
		TIOB0		Base timer ch.0 TIOB pin	—	○
		SIN0_1		Multifunction serial interface ch.0 input pin (Port 1)	—	○
		IN1		32-bit input capture ch.1 input pin	—	○

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Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
24	16	$\overline{INIT}$	P	External reset input pin. A reset is valid when $\overline{INIT}$ = L. The I/O circuit type for the flash memory products is P.	—	○
25	17	PK1	I	General-purpose I/O port	—	○
		X0A		Sub clock (oscillation) input pin	—	○
26	18	PK0	I	General-purpose I/O port	—	○
		X1A		Sub clock (oscillation) I/O pin	—	—
27	19	C	—	Power stabilization capacity pin	—	—
28	20	MD1	P	Mode 1 pin. Input must always be at the “L” level. The I/O circuit type for the flash memory products is P.	—	○
29	21	MD0	P	Mode 0 pin. The I/O circuit type for the flash memory products is P. During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	—	○
30	22	X0	A	Main clock (oscillation) input pin	—	○
31	23	X1	A	Main clock (oscillation) I/O pin	—	—
32	24	V_{SS}	—	GND pin	—	—
33	25	V_{CC}	—	Power pin	—	—
34	26	P02	Q*2	General-purpose I/O port	—	○
		D02		External bus interface data bus bit2	○	—
		TIOA1		Base timer ch.1 TIOA pin	—	○
		SCK0_1 (SCL0_1)		Multifunction serial interface ch.0 clock I/O pin (Port 1). This pin operates as SCK0_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0_1 when it is used in an I^2C (operation mode 4).	—	○
		IN2		32-bit input capture ch.2 input pin	—	○
35	27	P03	B	General-purpose I/O port	—	○
		D03		External bus interface data bus bit3	○	—
		TIOB1		Base timer ch.1 TIOB pin	—	○
		IN3		32-bit input capture ch.3 input pin	—	○

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Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
36	28	P04	Q*2	General-purpose I/O port	—	○
		D04		External bus interface data bus bit4	○	—
		TIOA2		Base timer ch.2 TIOA pin	—	—
		SOUT1 (SDA1)		Multifunction serial interface ch.1 output pin. This pin operates as SOUT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I²C (operation mode 4).	—	○
		IN4		32-bit input capture ch.4 input pin	—	○
37	29	P05	Q*2	General-purpose I/O port	—	○
		D05		External bus interface data bus bit5	○	—
		TIOB2		Base timer ch.2 TIOB pin	—	○
		SIN1		Multifunction serial interface ch.1 input pin	—	○
		IN5		32-bit input capture ch.5 input pin	—	○
38	30	P06	Q*2	General-purpose I/O port	—	○
		D06		External bus interface data bus bit6	○	—
		TIOA3		Base timer ch.3 TIOA pin	—	○
		SCK1 (SCL1)		Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I²C (operation mode 4).	—	○
		IN6		32-bit input capture ch.6 input pin	—	○
39	31	P07	B	General-purpose I/O port	—	○
		D07		External bus interface data bus bit7	○	—
		TIOB3		Base timer ch.3 TIOB pin	—	○
		IN7		32-bit input capture ch.7 input pin	—	○
40	32	P50	C	General-purpose I/O port	—	○
		$\overline{CS0}$		External bus interface chip select 0 output pin	—	—
		TMO0_1		16-bit reload timer ch.0 output pin (Port 1)	—	—

(Continued)

Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
41	—	P51	C	General-purpose I/O port	—	○
		$\overline{CS1}$		External bus interface chip select 1 output pin	—	—
		TIOA2_1		Base timer ch.2 TIOA pin (Port 1)	—	—
		SOUT1_1 (SDA1_1)		Multifunction serial interface ch.1 output pin (Port 1). This pin operates as SOUT1_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1_1 when it is used in an I²C (operation mode 4).	—	○
42	—	P52	C	General-purpose I/O port	—	○
		$\overline{CS2}$		External bus interface chip select 2 output pin	—	—
		TIOB2_1		Base timer ch.2 TIOB pin (Port 1)	—	○
		SIN1_1		Multifunction serial interface ch.1 input pin (Port 1)	—	○
43	—	P53	C	General-purpose I/O port	—	○
		$\overline{CS3}$		External bus interface chip select 3 output pin	—	—
		FRCK1		32-bit free-run timer ch.1 external clock input pin	—	○
		TIOA3_1		Base timer ch.3 TIOA pin (Port 1)	—	○
		SCK1_1 (SCL1_1)		Multifunction serial interface ch.1 clock I/O pin (Port 1). This pin operates as SCK1_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1_1 when it is used in an I²C (operation mode 4).	—	○
44	33	P54	C	General-purpose I/O port	—	○
		$\overline{AS}$		External bus interface address strobe output pin	—	—
		AIN1_1		Up/Down counter ch.1 AIN input pin (Port 1)	—	○
		SOUT6 (SDA6)		Multifunction serial interface ch.6 output pin. This pin operates as SOUT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I²C (operation mode 4).	—	○
45	34	P55	C	General-purpose I/O port	—	○
		$\overline{RD}$		External bus interface read strobe output pin	—	—
		BIN1_1		Up/Down counter ch.1 BIN input pin (Port 1)	—	○
		ADTRG0		10-bit A/D converter external trigger input pin	—	○
		SIN6		Multifunction serial interface ch.6 input pin	—	○

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Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
46	35	P56	C	General-purpose I/O port	—	○
		$\overline{WR0}$		External bus interface write strobe 0 output pin	—	—
		ZIN1_1		Up/Down counter ch.1 ZIN input pin (Port 1)	—	○
		FRCK0		32-bit free-run timer ch.0 external clock input pin	—	○
		SCK6 (SCL6)		Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I²C (operation mode 4).	—	○
47	—	P57	C	General-purpose I/O port	—	○
		$\overline{WR1}$		External bus interface write strobe 1 output pin	—	—
		TIOB3_1		Base timer ch.3 TIOB pin (Port 1)	—	○
		TMI2_1		16-bit reload timer ch.2 input pin (Port 1)	—	○
48	36	AV_{SS}	—	10-bit A/D converter GND pin	—	—
49	37	AV_{CC}	—	10-bit A/D converter analog power pin	—	—
50	38	P70	E	General-purpose I/O port	—	○
		AN0		10-bit A/D converter ch.0 analog input pin	—	—
		OUT0_1		32-bit output compare ch.0 output pin (Port 1)	—	—
		INT16		External interrupt request 16 input pin	—	○
51	39	P71	E	General-purpose I/O port	—	○
		AN1		10-bit A/D converter ch.1 analog input pin	—	—
		OUT1_1		32-bit output compare ch.1 output pin (Port 1)	—	—
		INT17		External interrupt request 17 input pin	—	○
52	40	P72	E	General-purpose I/O port	—	○
		AN2		10-bit A/D converter ch.2 analog input pin	—	—
		TMO0		16-bit reload timer ch.0 output pin	—	—
		OUT2_1		32-bit output compare ch.2 output pin (Port 1)	—	—
		INT18		External interrupt request 18 input pin	—	○
53	41	P73	E	General-purpose I/O port	—	○
		AN3		10-bit A/D converter ch.3 analog input pin	—	—
		TMO1		16-bit reload timer ch.1 output pin	—	—
		OUT3_1		32-bit output compare ch.3 output pin (Port 1)	—	—
		INT19		External interrupt request 19 input pin	—	○

(Continued)

Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
54	42	P74	E	General-purpose I/O port	—	○
		AN4		10-bit A/D converter ch.4 analog input pin	—	—
		TMO2		16-bit reload timer ch.2 output pin	—	—
		OUT4_1		32-bit output compare ch.4 output pin (Port 1)	—	—
		INT20		External interrupt request 20 input pin	—	○
55	43	P75	E	General-purpose I/O port	—	○
		AN5		10-bit A/D converter ch.5 analog input pin	—	—
		SOUT0 (SDA0)		Multifunction serial interface ch.0 output pin. This pin operates as SOUT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I²C (operation mode 4).	—	—
		TMI0		16-bit reload timer ch.0 input pin	—	○
		OUT5_1		32-bit output compare ch.5 output pin (Port 1)	—	—
		INT21		External interrupt request 21 input pin	—	○
56	44	P76	E	General-purpose I/O port	—	○
		AN6		10-bit A/D converter ch.6 analog input pin	—	—
		SIN0		Multifunction serial interface ch.0 input pin	—	○
		TMI1		16-bit reload timer ch.1 input pin	—	○
		OUT6_1		32-bit output compare ch.6 output pin (Port 1)	—	—
		INT22		External interrupt request 22 input pin	—	○
57	45	P77	E	General-purpose I/O port	—	○
		AN7		10-bit A/D converter ch.7 analog input pin	—	—
		SCK0 (SCL0)		Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I²C (operation mode 4).	—	○
		TMI2		16-bit reload timer ch.2 input pin	—	○
		OUT7_1		32-bit output compare ch.7 output pin (Port 1)	—	—
		INT23		External interrupt request 23 input pin	—	○
58	46	P80	E	General-purpose I/O port	—	○
		AN8		10-bit A/D converter ch.8 analog input pin	—	—
		IN0_1		32-bit input capture ch.0 input pin (Port 1)	—	○
		TMI0_1		16-bit reload timer ch.0 input pin (Port 1)	—	○

(Continued)

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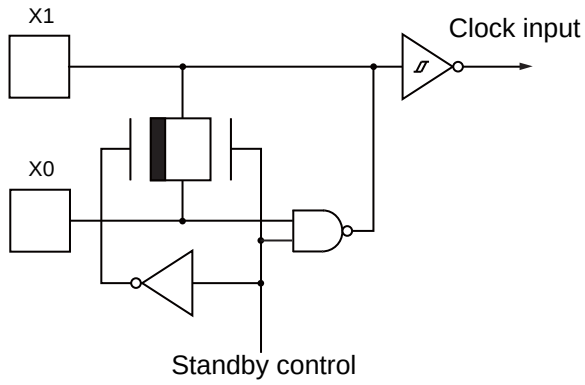
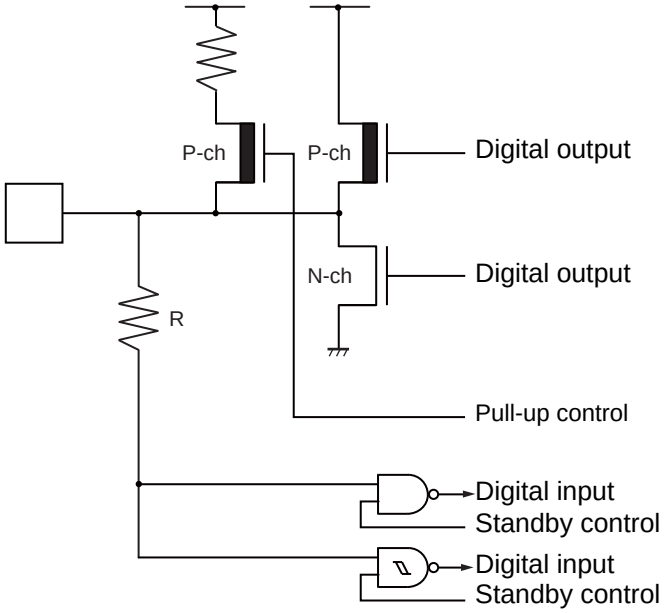
Pin Number		Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
64 pin	48 pin					
59	47	P81	E	General-purpose I/O port	—	○
		AN9		10-bit A/D converter ch.9 analog input pin	—	—
		IN1_1		32-bit input capture ch.1 input pin (Port 1)	—	○
		TMI1_1		16-bit reload timer ch.1 input pin (Port 1)	—	○
60	—	P82	E	General-purpose I/O port	—	○
		AN10		10-bit A/D converter ch.10 analog input pin	—	—
		IN2_1		32-bit input capture ch.2 input pin (Port 1)	—	○
61	—	P83	E	General-purpose I/O port	—	○
		AN11		10-bit A/D converter ch.11 analog input pin	—	—
		IN3_1		32-bit input capture ch.3 input pin (Port 1)	—	○
62	—	P60	B	General-purpose I/O port	—	○
		RDY		External bus interface ready input pin	○	—
		TIOA1_1		Base timer ch.1 TIOA pin (Port 1)	—	○
		SOUT2_1 (SDA2_1)		Multifunction serial interface ch.2 output pin (Port 1). This pin operates as SOUT2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2_1 when it is used in an I²C (operation mode 4).	—	○
63	—	P61	C	General-purpose I/O port	—	○
		SYSCLK		External bus interface bus clock output pin	—	—
		TIOB1_1		Base timer ch.1 TIOB pin (Port 1)	—	○
		SIN2_1		Multifunction serial interface ch.2 input pin (Port 1)	—	○
64	48	P10	Q	General-purpose I/O port	—	○
		D08		External bus interface data bus bit8	○	—
		SOUT2 (SDA2)		Multifunction serial interface ch.2 output pin. This pin operates as SOUT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I²C (operation mode 4).	—	○
		INT0		External interrupt request 0 input pin	—	○

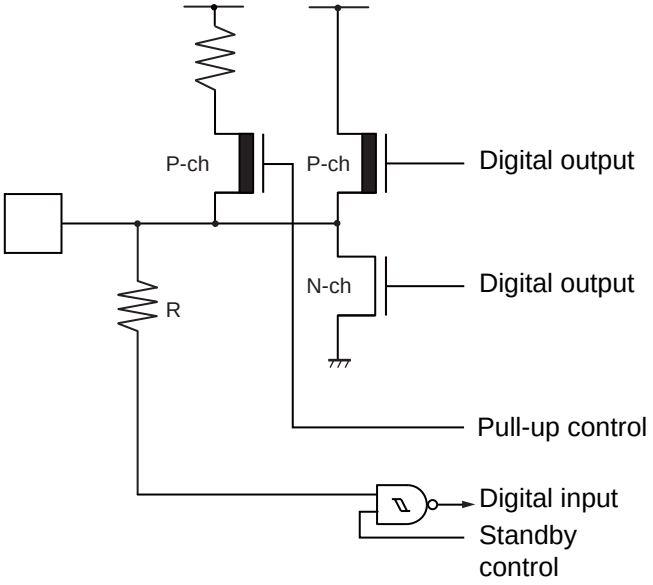
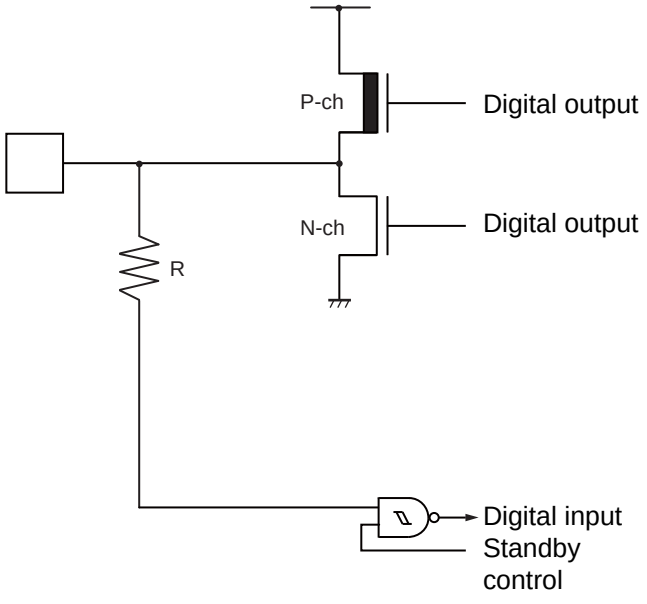
*1 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

*2 : 5 V tolerant pin.

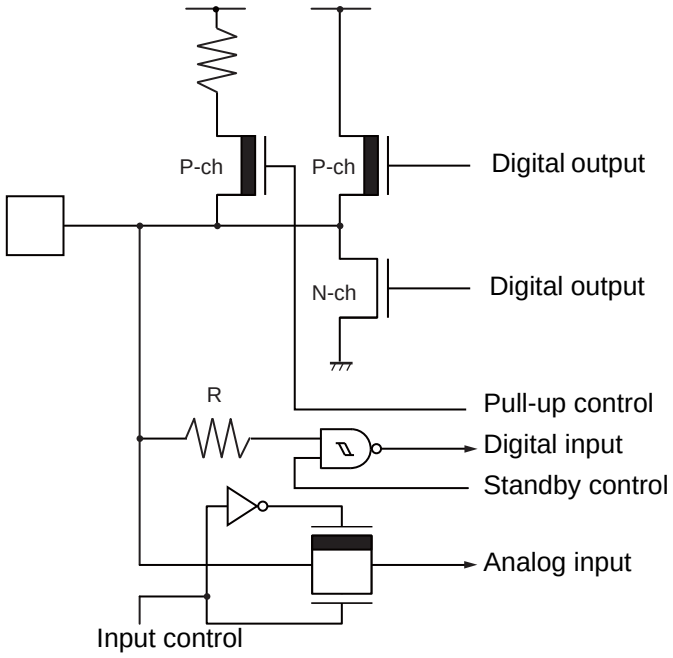
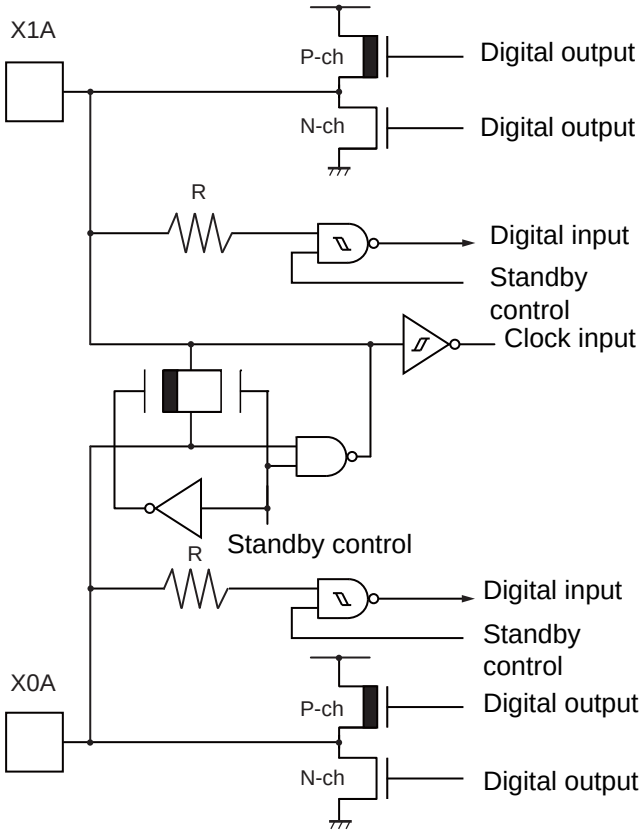
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance approx. 1 MΩ • With standby control
B		• CMOS level output • CMOS level input • CMOS level hysteresis input • With pull-up control • With standby control Notes: • CMOS level input when input data, RDY pin of external bus interface. Input other than above situations,CMOS level hysteresis input. • When this pin is used as an I²C pin, the digital output P-ch transistor is always off. • When this pin is used as a N-ch open drain control pin, the digital output P-ch transistor is always off.

(Continued)

Type	Circuit	Remarks
C		• CMOS level output • CMOS level hysteresis input • With pull-up control • With standby control Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
D		• CMOS level output • CMOS level hysteresis input • 5 V tolerant input • With standby control Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

(Continued)

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up control • With standby control Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
I		• Oscillation feedback resistance approx.10 MΩ • CMOS level output • CMOS level hysteresis input • With standby control

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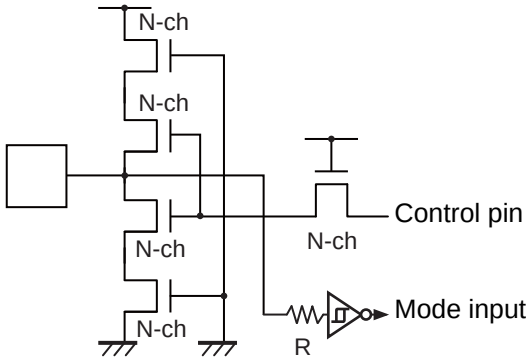
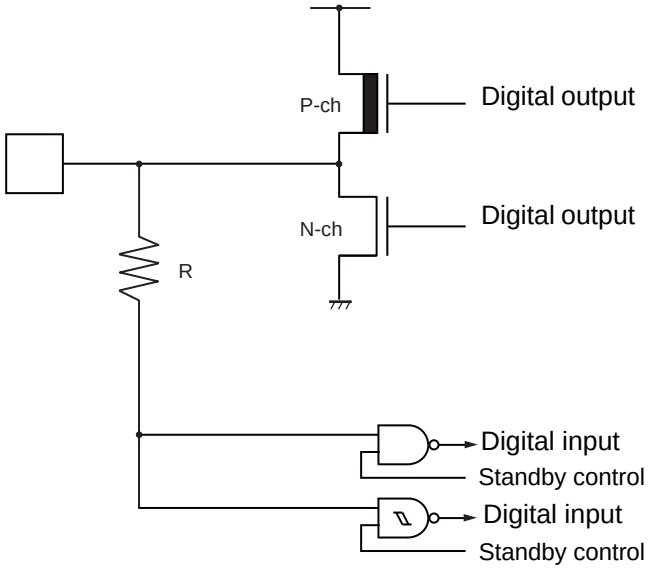
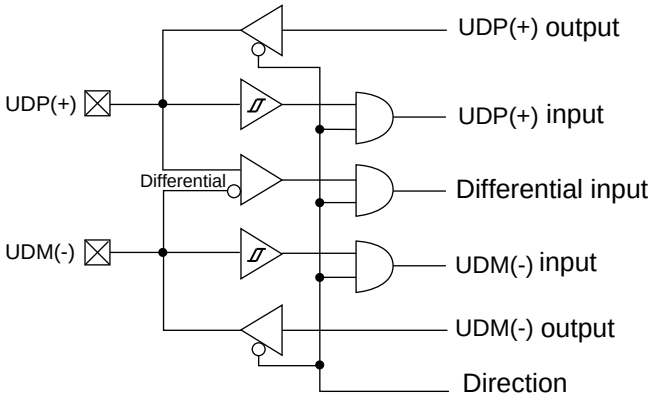
Type	Circuit	Remarks
P		• Flash memory product only • CMOS level hysteresis input • High voltage control for testing Flash memory
Q		• CMOS level output • CMOS level input • CMOS level hysteresis input • 5 V tolerant input • With standby control Note: When this pin is used as a N-ch open drain control pin, the digital output P-ch transistor is always off.
USB		USB I/O pin

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125 °C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

■ HANDLING DEVICES

• Power supply pins

In products with multiple V_{CC} and V_{SS} pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at low impedance.
It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between V_{CC} and V_{SS} near this device.

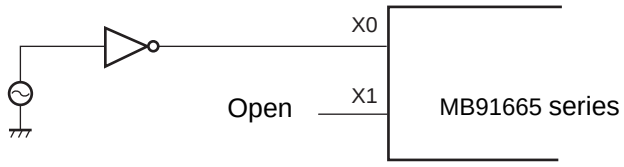
• Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.
It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.

• Using an external clock

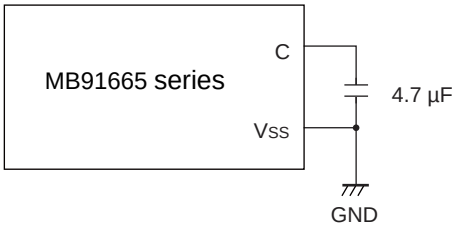
When using an external clock, the clock signal should be input to the X0 pin only and the X1 pin should be kept open.

• Example of Using an External Clock



• C Pin

As MB91660 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 μF to the C pin for use by the regulator.



- Mode pins (MD0, MD1)

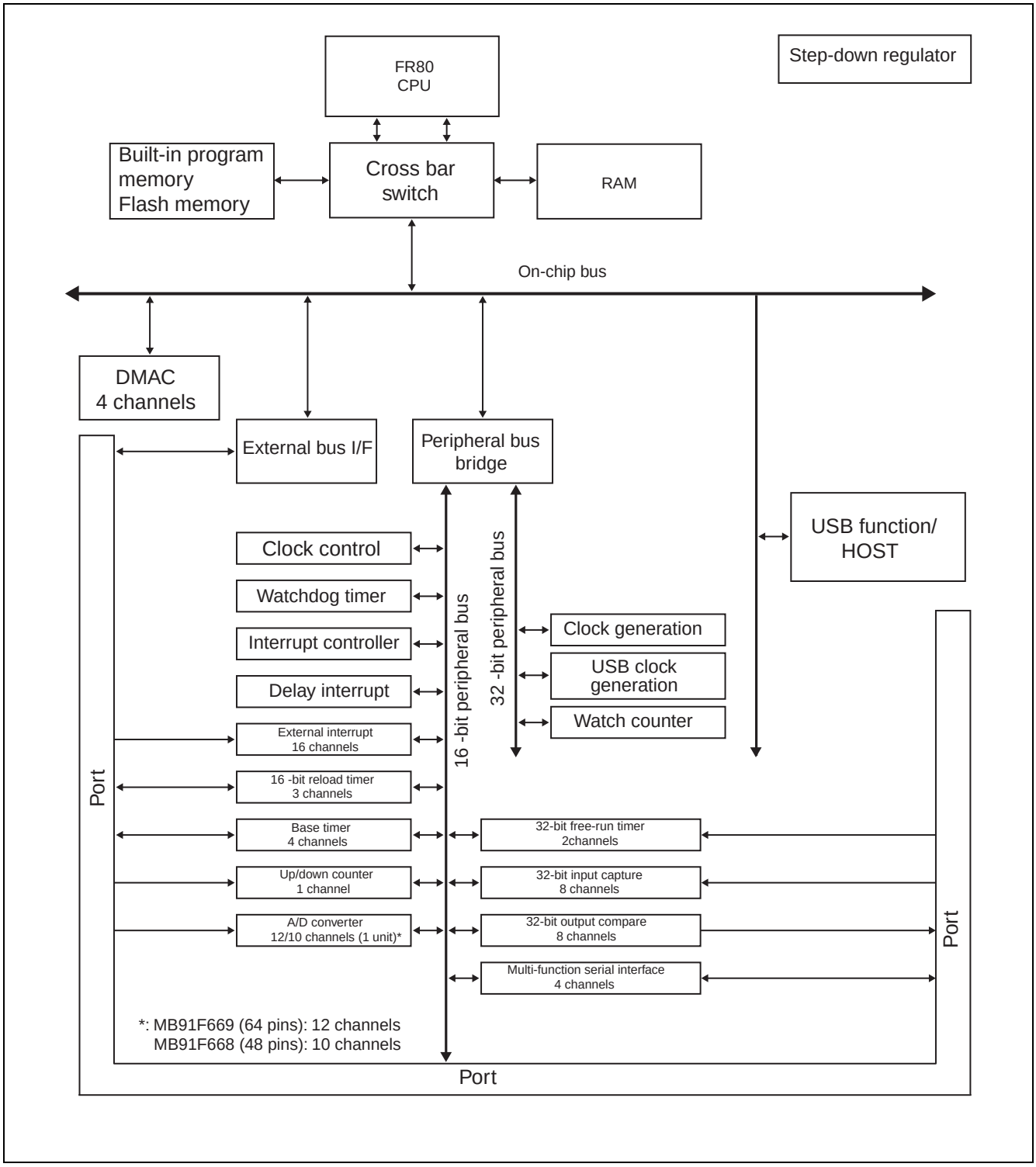
  Connect the MD pin (MD0, MD1) directly to V_{CC} or V_{SS} pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and V_{CC} pins or V_{SS} pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on
  - To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an “L” level input connected to the $\overline{INIT}$ pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.
  - Turn power on/off in the following order
    Turning on : $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$
    Turning off : $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$
  - Release the reset ($\overline{INIT}$ pin “L” level to “H” level) after the power supply has stabilized.

- Caution on operations during PLL clock mode

  On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.
  However, Fujitsu will not guarantee results of operations if such failure occurs.

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

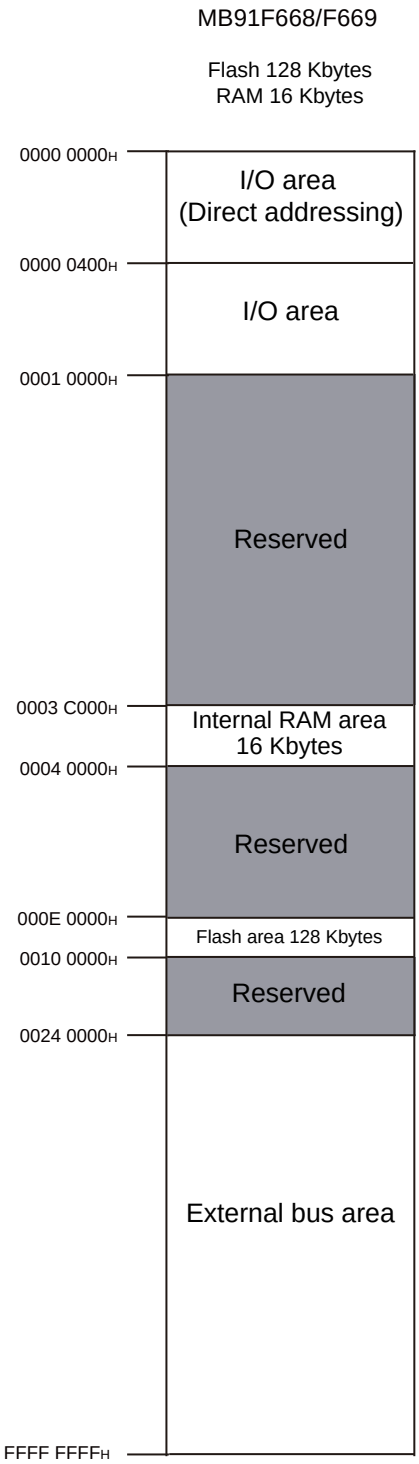
The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct Addressing Areas

The following areas in the address space are used as I/O areas.
These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000$_H$ to 0000 00FF$_H$
- Half word data access : 0000 0000$_H$ to 0000 01FF$_H$
- Word data access : 0000 0000$_H$ to 0000 03FF$_H$

2. Memory Map



Notes :
- Small sector area is related to flash products only. Please refer to the Flash Memory section of the Hardware Manual for more details.
- Do not access the reserved areas.

■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003CH	WDTCR0 [R/W] B, H - 0 - - 0000	WDTCPR0 [R/W] B, H 00000000	—		Watchdog timer
0000 0040H	EIRR0 [R/W] B, H, W 0000 0000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Initial value after reset
"1" : Initial value"1"
"0" : Initial value"0"
"X" : Initial value undefined
" - " : Reserved bit or undefined bit

— : Reserved area

Access unit
(B : byte, H : half word, W : word)

Read/write attribute
"R" : Indicates that there is a read only bit.
"R/W" : Indicates that there is a read/write bit.
"W" : Indicates that there is a write only bit.

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Notes : • When performing a data access, the addresses should be as below.
- Word access : Address should be multiples of 4 (least significant 2 bits should be "00B")
- Half word access : Address should be multiples of 2 (least significant bit should be "0B")
- Byte access : —

• Do not access the reserved areas.

Address	Registers				Block
	+0	+1	+2	+3	
0000 0000H	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	—	Port data register
0000 0004H	—	PDR5 [R/W] B,H XXXXXXXX	PDR6 [R/W] B,H XXXXXXXX	PDR7[R/W] B,H XXXXXXXX	
0000 0008H	PDR8 [R/W] B,H XXXXXXXX	—			
0000 000CH	—				
0000 0010H	—	PDRH [R/W] B,H ----XXXX	—		
0000 0014H	PDRK [R/W] B ----XXXX	—			
0000 0018H to 0000 001CH	—				
0000 0020H to 0000 0038H	—				Reserved
0000 003CH	WDTCR0[R/W] B,H - 0- - 0000	WDTCPR0[R/W] B,H 00000000	—		Watchdog timer
0000 0040H	EIRR0[R/W] B,H,W 00000000	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044H	DICR [R/W] B - - - - - - - 0	—			Delay interrupt
0000 0048H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004CH	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] H - - 000000 - - 000000		
0000 0050H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] H - - 000000 - - 000000		
0000 0058H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005CH	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] H - - 000000 - - 000000		

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0060H	SCR0[R/W] IBCR0[R,R/W] B,H,W*2 0 - - 00000	SMR0 [R/W] B,H,W 000 - 0000	SSR0 [R,R/W] B,H,W 0 - 000011	ESCR0[R/W] IBSR0[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.0
0000 0064H	RDR0[R]/TDR0[W] B,H,W*1 - - - - - - - 0 00000000		BGR10[R/W]H,W 00000000	BGR00[R/W] H,W 00000000	
0000 0068H	SCR1[R/W] IBCR1[R,R/W] B,H,W*2 0 - - 00000	SMR1 [R/W] B,H,W 000 - 0000	SSR1 [R,R/W] B,H,W 0 - 000011	ESCR1[R/W] IBSR1[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.1
0000 006CH	RDR1[R]/TDR1[W] B,H,W*1 - - - - - - - 0 00000000		BGR11[R/W] H,W 00000000	BGR01[R/W] H,W 00000000	
0000 0070H	ISMK1 [R/W] B,H*2 - - - - - - - -	ISBA1 [R/W] B,H*2 - - - - - - - -	—		
0000 0074H	SCR2[R/W] IBCR2[R,R/W] B,H,W*2 0 - - 00000	SMR2 [R/W] B,H,W 000 - 0000	SSR2 [R,R/W] B,H,W 0 - 000011	ESCR2[R/W] IBSR2 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.2
0000 0078H	RDR2[R]/TDR2[W] B,H,W*1 - - - - - - - 0 00000000		BGR12[R/W] H,W 00000000	BGR02[R/W] H,W 00000000	
0000 007CH	ISMK2 [R/W] B,H*2 - - - - - - - -	ISBA2 [R/W] B,H*2 - - - - - - - -	—		
0000 0080H to 0000 00A0H	—				Reserved
0000 00A4H	SCR6[R/W] IBCR6[R,R/W] B,H,W*2 0 - - 00000	SMR6 [R/W] B,H,W 000 - 0000	SSR6 [R,R/W] B,H,W 0 - 000011	ESCR6[R/W] IBSR6[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.6
0000 00A8H	RDR6[R]/TDR6[W] B,H,W*1 - - - - - - - 0 00000000		BGR16 [R/W] H,W 00000000	BGR06 [R/W] H,W 00000000	
0000 00ACH	ISMK6 [R/W] B,H*2 - - - - - - - -	ISBA6 [R/W] B,H*2 - - - - - - - -	—		
0000 00B0H to 0000 00B8H	—				Reserved

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 00BC$_H$	ISMK0 [R/W] B,H*2 - - - - - - - -	ISBA0 [R/W] B,H*2 - - - - - - - -	—		Multi-function serial interface ch.0
0000 00C0$_H$ to 0000 0110$_H$	—				Reserved
0000 0114$_H$	EIRR2[R/W] B,H,W 00000000	ENIR2[R/W] B,H,W 00000000	ELVR2[R/W] B,H,W 00000000 00000000		External interrupt 16 to 23
0000 0118$_H$ to 0000 011C$_H$	—				Reserved
0000 0120$_H$	ADCR0[R/W] B,H 000- 0000	ADSR0[R,R/W] B,H 00- - - 000	—		A/D converter
0000 0124$_H$	SCCR0[R,R/W] B,H 1000- 000	SFNS0[R/W] B,H - - - - 0000	SCFD0[R] B,H XXXXXXXX XX- XXXXX		
0000 0128$_H$	—	SCIS20[R/W] B 00000000	SCIS10[R/W] B,H 00000000	SCIS00[R/W] B,H 00000000	
0000 012C$_H$	PCCR0[R,R/W] B,H 1000- 000	PFNS0[R/W] B,H - - - - - - 00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130$_H$	PCIS0[R/W] B 00000000	—	CMPD0[R/W] B,H 00000000	CMPCR0[R/W] B,H 00000000	
0000 0134$_H$	—	ADSS20[R/W] B 00000000	ADSS10[R/W] B,H 00000000	ADSS00[R/W] B,H 00000000	
0000 0138$_H$	ADST00[R/W] B,H 00100000	ADST10[R/W] B,H 00100000	ADCT0[R/W] B - - - - - 111	—	
0000 013C$_H$	—				Reserved
0000 0140$_H$	BT0TMR[R]H 00000000 00000000		BT0TMCR[R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144$_H$	—	BT0STC[R/W]B 0000-000	—		
0000 0148$_H$	BT0PCSR/BT0PRLL[R/W]H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 014C$_H$	—				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0150H	BT1TMR[R]H 00000000 00000000		BT1TMCR[R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154H	—	BT1STC[R/W]B 0000-000	—		
0000 0158H	BT1PCSR/BT1PRLL[R/W]H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 015CH	—				
0000 0160H	BT2TMR[R]H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164H	—	BT2STC[R/W]B 0000-000	—		
0000 0168H	BT2PCSR/BT2PRLL[R/W]H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 016CH	—				
0000 0170H	BT3TMR[R]H 00000000 00000000		BT3TMCR[R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174H	—	BT3STC[R/W]B 0000-000	—		
0000 0178H	BT3PCSR/BT3PRLL[R/W]H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 017CH	BTSEL0123 [R/W] B 00000000	—			
0000 0180H to 0000 01A8H	—				Reserved
0000 01ACH	ADCHE [R/W] B,H,W -------- 111111-- ----1111 11111111				A/D channel enable
0000 01B0H	IRPR0H [R] B 000- - - - -	—			Interrupt request batch read function
0000 01B4H	—	IRPR2L [R] B,H,W 000- - - - -	IRPR3H [R] B,H,W 0000- - - -	IRPR3L [R] B,H,W 00000 - - -	
0000 01B8H	IRPR4H [R] B,H,W 0000- - - -	IRPR4L [R] B,H,W 000000- -	—		
0000 01BCH	—				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 01C0H to 0000 01CCH	—				Reserved
0000 01D0H	RCRH1 [W] H,W 00000000	RCRL1 [W] B,H,W 00000000	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/down counter ch.1
0000 01D4H	CCR1 [R,R/W] B,H 00000000 -0001000		—	CSR1 [R,R/W] B 00000000	
0000 01D8H	—				
0000 01DCH to 0000 01FCH	—				Reserved
0000 0200H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208H	TCCSH0 [R/W] B,H 0- - - - - 00	TCCSL0 [R/W] B,H - 1- 00000	—		
0000 020CH	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021CH	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	
0000 0220H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.4 to ch.7
0000 0224H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0228H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 022CH	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0230H	—	ICS45 [R/W] B 00000000	—	ICS67 [R/W] B 00000000	

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0234H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023CH	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244H	OCSH1 [R/W] B,H,W - - - 0- - 00	OCSL0 [R/W] B,H,W 0000- - 00	OCSH3 [R/W] B,H,W - - - 0- - 00	OCSL2 [R/W] B,H,W 0000- - 00	
0000 0248H	OCCP4 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.4 to ch.7
0000 024CH	OCCP5 [R/W] W 00000000 00000000 00000000 00000000				
0000 0250H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				
0000 0254H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
0000 0258H	OCSH5 [R/W] B,H,W - - - 0- - 00	OCSL4 [R/W] B,H,W 0000- - 00	OCSH7 [R/W] B,H,W - - - 0- - 00	OCSL6 [R/W] B,H,W 0000- - 00	
0000 025CH	FRTSEL [R/W] B - - - - - - 00	—			Free-run timer selector
0000 0260H	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.1
0000 0264H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
0000 0268H	TCCSH1 [R/W] B,H 0- - - - - 00	TCCSL1 [R/W] B,H - 1- 00000	—		
0000 026CH to 0000 031CH	—				Reserved
0000 0320H	FCTLR[R/W] H - 0- - 1011 - - - - - - - -		—	FSTR[R] B - - - - - - - 1	Flash memory control
0000 0324H to 0000 0334H	—				Reserved

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0338H	—		WREN[R/W] B,H 00000000 00000000		Wild register
0000 033CH	—				
0000 0340H to 0000 037CH	—				Reserved
0000 0380H	WRAR00[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				Wild register
0000 0384H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388H	WRAR01[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 038CH	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390H	WRAR02[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 0394H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398H	WRAR03[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 039CH	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0H	WRAR04[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03A4H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8H	WRAR05[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03ACH	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0H	WRAR06[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03B4H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B8H	WRAR07[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03BCH	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0H	WRAR08[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 03C4H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register
0000 03C8H	WRAR09[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03CCH	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D0H	WRAR10[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03D4H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8H	WRAR11[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03DCH	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0H	WRAR12[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03E4H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8H	WRAR13[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03ECH	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0H	WRAR14[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03F4H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8H	WRAR15[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03FCH	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0400H	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404H	DDR4 [R/W] B,H 00000000	DDR5 [R/W] B,H 00000000	DDR6 [R/W] B,H 00000000	DDR7[R/W] B,H 00000000	
0000 0408H	DDR8 [R/W] B 00000000	—	DDRA [R/W] B 00000000	—	
0000 040CH	—				
0000 0410H	DDRG [R/W] B,H 00000000	DDRH [R/W] B,H - - - - 0000	—		

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0414H	DDRK [R/W] B - - - - 0000	—			Data direction register
0000 0418H to 0000 041CH	—				
0000 0420H	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424H	—	PCR5 [R/W] B 00000000	PCR6 [R/W] B,H 00000000	PCR7[R/W] B,H 00000000	
0000 0428H	PCR8 [R/W] B,H 00000000	—			
0000 042CH to 0000 043CH	—				
0000 0440H	ICR00 [R,R/W] B,H,W - - - 11111	ICR01 [R,R/W] B,H,W - - - 11111	ICR02 [R,R/W] B,H,W - - - 11111	ICR03 [R,R/W] B,H,W - - - 11111	Interrupt control
0000 0444H	ICR04 [R,R/W] B,H,W - - - 11111	ICR05 [R,R/W] B,H,W - - - 11111	ICR06 [R,R/W] B,H,W - - - 11111	ICR07 [R,R/W] B,H,W - - - 11111	
0000 0448H	ICR08 [R,R/W] B,H,W - - - 11111	ICR09 [R,R/W] B,H,W - - - 11111	ICR10 [R,R/W] B,H,W - - - 11111	ICR11 [R,R/W] B,H,W - - - 11111	
0000 044CH	ICR12 [R,R/W] B,H,W - - - 11111	ICR13 [R,R/W] B,H,W - - - 11111	ICR14 [R,R/W] B,H,W - - - 11111	ICR15 [R,R/W] B,H,W - - - 11111	
0000 0450H	ICR16 [R,R/W] B,H,W - - - 11111	ICR17 [R,R/W] B,H,W - - - 11111	ICR18 [R,R/W] B,H,W - - - 11111	ICR19 [R,R/W] B,H,W - - - 11111	
0000 0454H	ICR20 [R,R/W] B,H,W - - - 11111	ICR21 [R,R/W] B,H,W - - - 11111	ICR22 [R,R/W] B,H,W - - - 11111	ICR23 [R,R/W] B,H,W - - - 11111	
0000 0458H	ICR24 [R,R/W] B,H,W - - - 11111	ICR25 [R,R/W] B,H,W - - - 11111	ICR26 [R,R/W] B,H,W - - - 11111	ICR27 [R,R/W] B,H,W - - - 11111	
0000 045CH	ICR28 [R,R/W] B,H,W - - - 11111	ICR29 [R,R/W] B,H,W - - - 11111	ICR30 [R,R/W] B,H,W - - - 11111	ICR31 [R,R/W] B,H,W - - - 11111	

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0460H	ICR32 [R,R/W] B,H,W - - - 11111	ICR33 [R,R/W] B,H,W - - - 11111	ICR34 [R,R/W] B,H,W - - - 11111	ICR35 [R,R/W] B,H,W - - - 11111	Interrupt control
0000 0464H	ICR36 [R,R/W] B,H,W - - - 11111	ICR37 [R,R/W] B,H,W - - - 11111	ICR38 [R,R/W] B,H,W - - - 11111	ICR39 [R,R/W] B,H,W - - - 11111	
0000 0468H	ICR40 [R,R/W] B,H,W - - - 11111	ICR41 [R,R/W] B,H,W - - - 11111	ICR42 [R,R/W] B,H,W - - - 11111	ICR43 [R,R/W] B,H,W - - - 11111	
0000 046CH	ICR44 [R,R/W] B,H,W - - - 11111	ICR45 [R,R/W] B,H,W - - - 11111	ICR46 [R,R/W] B,H,W - - - 11111	ICR47 [R,R/W] B,H,W - - - 11111	
0000 0470H to 0000 047CH	—				Reserved
0000 0480H	RSTRR [R] B,H,W 11-X- - - X*3	RSTCR [R/W] B,H,W 000- - - - 0	STBCR [R/W] B,H,W 0000- - 11	SLPRR [R/W] B,H,W 00000000	Reset control/ Power consumption control
0000 0484H	—				
0000 0488H	DIVR0 [R/W] B,H 000- - - - -	DIVR1 [R/W] B,H 0001- - - -	DIVR2 [R/W] B 0011- - - -	—	Clock division control
0000 048CH	—				
0000 0490H	IORR0 [R/W] B,H,W - 0000000	IORR1 [R/W] B,H,W - 0000000	IORR2 [R/W] B,H,W - 0000000	IORR3 [R/W] B,H,W - 0000000	Peripheral DMA transmission request control
0000 0494H to 0000 049CH	—				Reserved
0000 04A0H	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4H	PFR4 [R/W] B,H 00000000	PFR5 [R/W] B,H 00000000	PFR6 [R/W] B,H 00- 00- 0-	PFR7[R/W] B,H 00000000	
0000 04A8H	PFR8 [R/W] B 00000000	—	PFRA [R/W] B 00-00000	—	
0000 04ACH	—				
0000 04B0H	PFRG [R/W] B,H - 000- 000	PFRH [R/W] B,H - - - - - 0- 0	—		
0000 04B4H	—				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 04B8H	EPFR0 [R/W] B,H - - 000000	EPFR1 [R/W] B,H - - 000000	EPFR2 [R/W] B,H - - 000000	EPFR3 [R/W] B,H - - 000000	Extended port function register
0000 04BCH	EPFR4 [R/W] B,H 00000000	EPFR5 [R/W] B,H 00000000	EPFR6 [R/W] B,H 00000000	EPFR7 [R/W] B,H - - - 00000	
0000 04C0H	EPFR8 [R/W] B,H - - - 00000	EPFR9 [R/W] B,H - - - 00000	EPFR10 [R/W] B,H - - - 00000	EPFR11 [R/W] B,H - - - 00000	
0000 04C4H	EPFR12 [R/W] B,H - - - 00000	EPFR13 [R/W] B,H - - - 00000	EPFR14 [R/W] B,H - - - 00000	EPFR15 [R/W] B,H - - - 00000	
0000 04C8H	EPFR16 [R/W] B,H - - - 00000	EPFR17 [R/W] B,H - - - 00000	EPFR18 [R/W] B,H 00000000	EPFR19 [R/W] B,H - - - - 0001	
0000 04CCH	EPFR20 [R/W] B,H - - 000000	EPFR21 [R/W] B,H - - 000000	EPFR22 [R/W] B,H - - 000000	EPFR23 [R/W] B,H - - 000000	
0000 04D0H	EPFR24 [R/W] B,H - - 000000	EPFR25 [R/W] B,H - - 000000	EPFR26 [R/W] B,H - - 000000	EPFR27 [R/W] B,H - - 000000	
0000 04D4H	EPFR28 [R/W] B,H 00000000	EPFR29 [R/W] B,H 00000000	EPFR30 [R/W] B,H - - - - 0000	EPFR31 [R/W] B,H - 0000000	
0000 04D8H	EPFR32 [R/W] B,H 00000000	EPFR33 [R/W] B,H - - 000000	EPFR34 [R/W] B,H - 0000000	EPFR35 [R/W] B,H - - - - - - 00	
0000 04DCH	NDE0 [R/W] B,H 00000000	NDE1 [R/W] B,H 00000000	EXBS [R/W] B - - - - - - - 0	—	
0000 04E0H to 0000 04ECH	—				Reserved
0000 04F0H	ICSEL0[R/W] B,H,W - - - - - 000	—	ICSEL2[R/W] B,H,W - - - - - 000	—	DMA start request clear select function
0000 04F4H	ICSEL4[R/W] B,H,W - - - - - - 00	—	ICSEL6[R/W] B,H,W - - - - - - 00	ICSEL7[R/W] B,H,W - - - - - - - 0	
0000 04F8H	ICSEL8[R/W] B,H,W - - - - - - 00	ICSEL9[R/W] B,H,W - - - - - 000	ICSEL10[R/W] B,H,W - - - - 0000	—	
0000 04FCH	—				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0500H	—				Reserved
0000 0504H	FRID [R] W For the initial value, see the I/O Ports section of the Hardware Manual.				FR80ID
0000 0508H to 0000 050CH	—				Reserved
0000 0510H	CSELR [R/W] B,H,W 001- - - 00	CMONR [R] B,H,W 001- - - 00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000- 111	Clock generation/ Main timer/ Sub timer
0000 0514H	PLLCR [R/W] B,H - - 000000 11110000		CSTBR [R/W] B - 0000000	—	
0000 0518H	WCRD [R] B,H - - 000000	WCRL [R/W] B,H - - 000000	WCCR [R,R/W] B 00- - 0000	—	Clock counter
0000 051CH	UCCR [R/W] B - - - - - 001	—			USB clock generation
0000 0520H to 0000 05FCH	—				Reserved
0000 0600H	ASR0 [R/W] W 00000000 00000000 - - - - - - - - 1111- 001				External bus I/F
0000 0604H	ASR1 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 0608H	ASR2 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 060CH	ASR3 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 0610H to 0000 063CH	—				
0000 0640H	ACR0[R/W] W - 00- - 00- 0				
0000 0644H	ACR1[R/W] W - XX- - XX- X				
0000 0648H	ACR2[R/W] W - XX- - XX- X				
0000 064CH	ACR3[R/W] W - XX- - XX- X				
0000 0650H to 0000 067CH	—				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0680H	AWR0 [R/W] W - - - - 1111 00000000 11110000 00000- 0-				External bus I/F
0000 0684H	AWR1 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				
0000 0688H	AWR2 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				
0000 068CH	AWR3 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				
0000 0690H to 0000 06BCH	—				
0000 06C0H to 0000 0BFCH	—				Reserved
0000 0C00H	DCCR0 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				DMAC
0000 0C04H	DCSR0 [R, R/W] H 0- - - - - - - - - - - - - 000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0CH	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10H	DCCR1 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C14H	DCSR1 [R, R/W] H 0- - - - - - - - - - - - - 000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1CH	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C20H	DCCR2 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C24H	DCSR2 [R, R/W] H 0- - - - - - - - - - - - - 000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2CH	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30H	DCCR3 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 0C34H	DCSR3 [R, R/W] H 0- - - - - - - - - - - - - 000		DTCR3 [R/W] H 00000000 00000000		DMAC
0000 0C38H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C3CH	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40H to 0000 0DF0H	—				
0000 0DF4H	—			DILVR [R,R/W] B - - - 11111	
0000 0DF8H	DMACR [R/W] W 0- - - - - - - - - - - - - - - - 0- - - - - - - - - - - - - - - -				
0000 0DFCH to 0000 20FCH	—				Reserved
0000 2100H	HCNT1[R/W] B,H - - - - - 001	HCNT0[R/W] B,H 00000000	—		USB function/ HOST
0000 2104H	HERR[R/W] B,H 00000011	HIRQ[R/W] B,H 0- 000000	—		
0000 2108H	HFCOMP[R/W] B,H 00000000	HSTATE[R,R/W] B,H - - - 10010	—		
0000 210CH	HRTIMER1[R/W] B,H 00000000	HRTIMER0[R/W] B,H 00000000	—		
0000 2110H	HADR[R/W] B,H - 0000000	HRTIMER2[R/W] B,H - - - - - - 00	—		
0000 2114H	HEOF1[R/W] B,H - - 000000	HEOF0[R/W] B,H 00000000	—		
0000 2118H	HFRAME1[R/W] B,H - - - - - 000	HFRAME0[R/W] B,H 00000000	—		
0000 211CH	—	HTOKEN[R/W] B 00000000	—		

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 2120H	—	UDCC[R/W] B 1010- - 00	—		USB function/ HOST
0000 2124H	EP0C[R/W] H - - - - - - 0- - 1000000		—		
0000 2128H	EP1C[R/W] H 01100001 00000000		—		
0000 212CH	EP2C[R/W] H 0110000- - 1000000		—		
0000 2130H	EP3C[R/W] H 0110000- - 1000000		—		
0000 2134H to 0000 2138H	—				
0000 213CH	TMSP[R] H - - - - - 000 00000000		—		
0000 2140H	UDCIE[R,R/W] B,H - - 000000	UDCS[R/W] B,H - - 000000	—		
0000 2144H	EP0IS[R/W] H 10- - - 1- - - - - - - - -		—		
0000 2148H	EP00S[R,R/W] H 100- - 00- - XXXXXXX		—		
0000 214CH	EP1S[R,R/W] H 100- 000X XXXXXXXX		—		
0000 2150H	EP2S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 2154H	EP3S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 2158H to 0000 215CH	—				
0000 2160H	EP0DTH [R/W] B,H XXXXXXXX	EP0DTL [R/W] B,H XXXXXXXX	—		
0000 2164H	EP1DTH [R/W] B,H XXXXXXXX	EP1DTL [R/W] B,H XXXXXXXX	—		
0000 2168H	EP2DTH [R/W] B,H XXXXXXXX	EP2DTL [R/W] B,H XXXXXXXX	—		
0000 216CH	EP3DTH [R/W] B,H XXXXXXXX	EP3DTL [R/W] B,H XXXXXXXX	—		

(Continued)

(Continued)

Address	Registers				Block
	+0	+1	+2	+3	
0000 2170H to 0000 217CH	—				USB function/ HOST
0000 2180H to 0000 21A0H	—				Reserved
0000 21A4H	DREQSEL [R/W] B,H 00111011	USBSEL [R/W] B,H - - - - - - - 0	USBEN [R/W] B - - - - - - - 0	—	DMA transfer request selector/ USB enable
0000 21A8H to 0000 FFFCH	—				Reserved

*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

*2 : The register of I^2C can not be read immediate after reset.

*3 : Value just after reset by $\overline{INIT}$ pin.
Do not access the reserved areas.

■ VECTOR TABLE

Interrupt Source (Peripheral Function)	Interrupt Number		Interrupt level setting registers	Offset	TBR Initial address
	Dec.	Hex.			
Reset	0	00	—	3FC$_H$	000F FFFC$_H$
Reserved for system	1	01	—	3F8$_H$	000F FFF8$_H$
Reserved for system	2	02	—	3F4$_H$	000F FFF4$_H$
Reserved for system	3	03	—	3F0$_H$	000F FFF0$_H$
Reserved for system	4	04	—	3EC$_H$	000F FFEC$_H$
Reserved for system	5	05	—	3E8$_H$	000F FFE8$_H$
Reserved for system	6	06	—	3E4$_H$	000F FFE4$_H$
Reserved for system	7	07	—	3E0$_H$	000F FFE0$_H$
Reserved for system	8	08	—	3DC$_H$	000F FFDC$_H$
INTE instruction	9	09	—	3D8$_H$	000F FFD8$_H$
Reserved for system	10	0A	—	3D4$_H$	000F FFD4$_H$
Reserved for system	11	0B	—	3D0$_H$	000F FFD0$_H$
Step trace trap	12	0C	—	3CC$_H$	000F FFCC$_H$
Reserved for system	13	0D	—	3C8$_H$	000F FFC8$_H$
Undefined instruction exception	14	0E	—	3C4$_H$	000F FFC4$_H$
—	15	0F	Always 15(F$_H$)	3C0$_H$	000F FFC0$_H$
External interrupt request ch.0 to ch.7	16	10	ICR00	3BC$_H$	000F FFBC$_H$
Reserved	17	11	ICR01	3B8$_H$	000F FFB8$_H$
External interrupt request ch.16 to ch.23	18	12	ICR02	3B4$_H$	000F FFB4$_H$
Reserved	19	13	ICR03	3B0$_H$	000F FFB0$_H$
16-bit reload timer ch.0 to ch.2	20	14	ICR04	3AC$_H$	000F FFAC$_H$
Reception interrupt request from UART/CSIO/I^{2}C ch.0	21	15	ICR05	3A8$_H$	000F FFA8$_H$
Transmission interrupt request from UART/CSIO/I^{2}C ch.0 Transmission bus idle interrupt request from UART/CSIO ch.0	22	16	ICR06	3A4$_H$	000F FFA4$_H$
Reception interrupt request from UART/CSIO/I^{2}C ch.1	23	17	ICR07	3A0$_H$	000F FFA0$_H$
Transmission interrupt request from UART/CSIO/I^{2}C ch.1 Transmission bus idle interrupt request from UART/CSIO ch.1	24	18	ICR08	39C$_H$	000F FF9C$_H$
Status interrupt request from I^{2}C ch.1	25	19	ICR09	398$_H$	000F FF98$_H$
Reception interrupt request from UART/CSIO/I^{2}C ch.2	26	1A	ICR10	394$_H$	000F FF94$_H$

(Continued)

Interrupt Source (Peripheral Function)	Interrupt Number		Interrupt level setting registers	Offset	TBR Initial address
	Dec.	Hex.			
Transmission interrupt request from UART/CSIO/ I²C ch.2 Transmission bus idle interrupt request from UART/CSIO ch.2	27	1B	ICR11	390H	000F FF90H
Status interrupt request from I²C ch.2	28	1C	ICR12	38CH	000F FF8CH
Reserved	29	1D	ICR13	388H	000F FF88H
Reserved	30	1E	ICR14	384H	000F FF84H
Reserved	31	1F	ICR15	380H	000F FF80H
Reserved	32	20	ICR16	37CH	000F FF7CH
Reserved	33	21	ICR17	378H	000F FF78H
Reserved	34	22	ICR18	374H	000F FF74H
Reception interrupt request from UART/CSIO/I²C ch.6	35	23	ICR19	370H	000F FF70H
Transmission interrupt request from UART/CSIO/ I²C ch.6 Transmission bus idle interrupt request from UART/CSIO ch.6 Status interrupt request from I²C ch.6	36	24	ICR20	36CH	000F FF6CH
32-bit input capture ch.4 to ch.7	37	25	ICR21	368H	000F FF68H
32-bit output compare ch.4 to ch.7	38	26	ICR22	364H	000F FF64H
Reserved	39	27	ICR23	360H	000F FF60H
16-bit up/down counter ch.0	40	28	ICR24	35CH	000F FF5CH
Main timer/sub timer/watch counter	41	29	ICR25	358H	000F FF58H
10-bit A/D converter - Scanning conversion interrupt request - Priority conversion interrupt request - FIFO overrun interrupt request - Conversion result comparison interrupt request	42	2A	ICR26	354H	000F FF54H
32-bit free-run timer ch.0, ch.1	43	2B	ICR27	350H	000F FF50H
32-bit input capture ch.0 to ch.3	44	2C	ICR28	34CH	000F FF4CH
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348H	000F FF48H
Base timer ch.0	46	2E	ICR30	344H	000F FF44H
Base timer ch.1	47	2F	ICR31	340H	000F FF40H
Base timer ch.2	48	30	ICR32	33CH	000F FF3CH
Base timer ch.3	49	31	ICR33	338H	000F FF38H
Reserved	50	32	ICR34	334H	000F FF34H
Reserved	51	33	ICR35	330H	000F FF30H

(Continued)

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Interrupt Source (Peripheral Function)	Interrupt Number		Interrupt level setting registers	Offset	TBR Initial address
	Dec.	Hex.			
Reserved	52	34	ICR36	$32C_H$	000F FF2C$_H$
Reserved	53	35	ICR37	328_H	000F FF28$_H$
USB function (End point 1 to 3 for DRQ)	54	36	ICR38	324_H	000F FF24$_H$
USB function (End point 0 for DRQI, DRQO and each status)/USB HOST (each status)	55	37	ICR39	320_H	000F FF20$_H$
Reserved	56	38	ICR40	$31C_H$	000F FF1C$_H$
DMA Controller (DMAC) ch.0	57	39	ICR41	318_H	000F FF18$_H$
DMA Controller (DMAC) ch.1	58	3A	ICR42	314_H	000F FF14$_H$
DMA Controller (DMAC) ch.2	59	3B	ICR43	310_H	000F FF10$_H$
DMA Controller (DMAC) ch.3	60	3C	ICR44	$30C_H$	000F FF0C$_H$
Reserved	61	3D	ICR45	308_H	000F FF08$_H$
System reserved	62	3E	ICR46	304_H	000F FF04$_H$
Delay interrupt	63	3F	ICR47	300_H	000F FF00$_H$
Reserved for system (used by REALOS)	64	40	—	$2FC_H$	000F FEFC$_H$
Reserved for system (used by REALOS)	65	41	—	$2F8_H$	000F FEF8$_H$
Used by the INT instruction	66 to 255	42 to FF	—	$2F4_H$ to 000_H	000F FEF4$_H$ to 000F FC00$_H$

* : USB interrupt source

Interrupt Number		USB interrupt source	Details
Decimal	Hexadecimal		
54	36	USB function (DRQ of End Point 1 to 3)	DRQ (End Point1 to 3)
55	37	USB function (DRQI, DRQO of End Point 0 and each status)	DRQI, DRQO, SPK, SUSP, SOF, BRST, CONF, WKUP
		USB HOST (Each status)	DIRQ, URIRQ, RWKIRQ, CNNIRQ, SOFIRQ, CMPIRQ

■ PIN STATUS IN EACH CPU STATE

- When $\overline{\text{INIT}}$ = “L”

This is the period when the $\overline{\text{INIT}}$ pin is the “L” level.

- When $\overline{\text{INIT}}$ = “H”

The status immediately after the $\overline{\text{INIT}}$ pin changes from the “L” level to the “H” level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR).

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

- Internal input fixed at “0”

The input gate connected to the pin is disconnected from the external input and internally connected to “0”.

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin Name	Function Name	During initialization		Sleep Mode	Standby Mode	
		$\overline{INIT}$ = "L" Period	$\overline{INIT}$ = "H" Period		SLVL1 = 0	SLVL1 = 1
$\overline{INIT}$	$\overline{INIT}$	—	—	Input enabled	Input enabled	Input enabled
X0	X0	Input enabled	Input enabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1	X1	Input enabled	Input enabled		"H" output or Input enabled	"H"output or Input enabled
X0A	X0A (When $\overline{INIT}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1A	X1A (When $\overline{INIT}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled		"H"output or Input enabled	"H"output or Input enabled
MD0	MD0	Input enabled	Input enabled		Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled			
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P01	P01/D01/TIOB0/SIN0_1/IN1					
P02	P02/D02/TIOA1/SCK0_1/IN2					
P03	P03/D03/TIOB1/IN3					
P04	P04/D04/TIOA2/SOUT1/IN4					
P05	P05/D05/TIOB2/SIN1/IN5					
P06	P06/D06/TIOA3/SCK1/IN6					
P07	P07/D07/TIOB3/IN7					
P10	P10/D08/SOUT2/INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P11	P11/D09/SIN2/INT1					
P12	P12/D10/SCK2/INT2					
P13	P13/D11/INT3					
P14	P14/D12/AIN1/INT4/OUT4					
P15	P15/D13/BIN1/INT5/OUT5					
P16	P16/D14//ZIN1/INT6/OUT6					
P17	P17/D15/INT7/OUT7					

(Continued)

Pin Name	Function Name	During initialization		Sleep Mode	Standby Mode	
		$\overline{INIT}$ = "L" Period	$\overline{INIT}$ = "H" Period		SLVL1 = 0	SLVL1 = 1
P20	P20/A00/TMO1_1/A16	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P21	P21/A01/TMO2_1/A17					
P22	P22/A02/TIOA0_1/A18					
P23	P23/A03/TIOB0_1/A19					
P24	P24/A04/OUT0/A20					
P25	P25/A05/OUT1/A21					
P26	P26/A06/OUT2/A22					
P27	P27/A07/OUT3/A23					
P50	P50/$\overline{CS0}$/TMO0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P51	P51/$\overline{CS1}$/TIOA2_1/SOUT1_1					
P52	P52/$\overline{CS2}$/TIOB2_1/SIN1_1					
P53	P53/$\overline{CS3}$/FRCK1/TIOA3_1/ SCK_1					
P54	P54/$\overline{AS}$/SOUT6/AIN1_1					
P55	P55/$\overline{RD}$/SIN6/BIN1_1/ADTRG0					
P56	P56/$\overline{WR0}$/SCK6/ZIN1_1/FRCK0					
P57	P57/$\overline{WR1}$/TIOB3_1/TMI2_1					
P60	P60/RDY/TIOA1_1/SOUT2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P61	P61/SYSCLK/TIOB1_1/SIN2_1					
P70	P70/AN0/OUT0_1/INT16	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P71	P71/AN1/OUT1_1/INT17					
P72	P72/AN2/TMO0/OUT2_1/INT18					
P73	P73/AN3/TMO1/OUT3_1/INT19					
P74	P74/AN4/TMO2/OUT4_1/INT20					
P75	P75/AN5/SOUT0/TMI0/OUT5_1/ INT21					
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22					
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23					

(Continued)

(Continued)

Pin Name	Function Name	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}}$ = "L" Period	$\overline{\text{INIT}}$ = "H" Period		SLVL1 = 0	SLVL1 = 1
P80	P80/AN8/IN0_1/TMI0_1	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P81	P81/AN9/IN1_1/TMI1_1					
P82	P82/AN10/IN2_1					
P83	P83/AN11/IN3_1					
PH2	PH2/SCK2_1/INT2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
PH3	PH3/INT3_1					
PK0	PK0	Output Hi-Z	Output Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PK1	PK1					
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z/Input enabled	Maintain previous state/Input enabled	Maintain previous state	Maintain previous state
UDM	UDM (USB)					

• List of pin status (serial write mode)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"	
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P01	P01/D01/TIOB0/SIN0_1/IN1			
P02	P02/D02/TIOA1/SCK0_1/IN2			
P03	P03/D03/TIOB1/IN3			
P04	P04/D04/TIOA2/SOUT1/IN4			
P05	P05/D05/TIOB2/SIN1/IN5			
P06	P06/D06/TIOA3/SCK1/IN6			
P07	P07/D07/TIOB3/IN7			
P10	P10/D08/SOUT2/INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P11	P11/D09/SIN2/INT1			
P12	P12/D10/SCK2/INT2			
P13	P13/D11/INT3			
P14	P14/D12/AIN1/INT4/OUT4			
P15	P15/D13/BIN1/INT5/OUT5			
P16	P16/D14//ZIN1/INT6/OUT6			
P17	P17/D15/INT7/OUT7			

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
P20	P20/A00/TMO1_1/A16	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P21	P21/A01/TMO2_1/A17			
P22	P22/A02/TIOA0_1/A18			
P23	P23/A03/TIOB0_1/A19			
P24	P24/A04/OUT0/A20			
P25	P25/A05/OUT1/A21			
P26	P26/A06/OUT2/A22			
P27	P27/A07/OUT3/A23			
P50	P50/$\overline{CS0}$/TMO0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P51	P51/$\overline{CS1}$/TIOA2_1/SOUT1_1			
P52	P52/$\overline{CS2}$/TIOB2_1/SIN1_1			
P53	P53/$\overline{CS3}$/FRCK1/TIOA3_1/ SCK_1			
P54	P54/$\overline{AS}$/SOUT6/AIN1_1			
P55	P55/$\overline{RD}$/SIN6/BIN1_1/ADTRG0			
P56	P56/$\overline{WR0}$/SCK6/ZIN1_1/FRCK0			
P57	P57/$\overline{WR1}$/TIOB3_1/TMI2_1			
P60	P60/RDY/TIOA1_1/SOUT2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P61	P61/SYSCLK/TIOB1_1/SIN2_1			
P70	P70/AN0/OUT0_1/INT16	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P71	P71/AN1/OUT1_1/INT17			
P72	P72/AN2/TMO0/OUT2_1/INT18			
P73	P73/AN3/TMO1/OUT3_1/INT19			
P74	P74/AN4/TMO2/OUT4_1/INT20			
P75	P75/AN5/SOUT0/TMI0/OUT5_1/ INT21	Output Hi-Z/ Input enabled	Output	Output
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23		Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled
P80	P80/AN8/IN0_1/TMI0_1	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P81	P81/AN9/IN1_1/TMI1_1			
P82	P82/AN10/IN2_1			
P83	P83/AN11/IN3_1			

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Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"	
PH2	PH2/SCK2_1/INT2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PH3	PH3/INT3_1			
PK0	PK0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PK1	PK1			
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
UDM	UDM (USB)			

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	Vss − 0.3	Vss + 4.0	V	
Analog power supply voltage*1, *3	AV_{CC}	Vss − 0.3	Vss + 4.0	V	
Analog reference voltage*1, *3	AVRH	Vss − 0.3	Vss + 4.0	V	
Input voltage*1	V_I	Vss − 0.3	V_{CC} + 0.3 (≤ 4.0)	V	*7
		Vss − 0.3	Vss + 6.0	V	5 V tolerant
		Vss − 0.5	V_{CC} + 0.5 (≤ 4.0)	V	USB I/O
Analog pin input voltage*1	V_{IA}	Vss − 0.3	Vss + 4.0	V	
Output voltage*1	V_O	Vss − 0.3	Vcc + 0.3	V	
		Vss − 0.5	V_{CC} + 0.5 (≤ 4.0)	V	USB I/O
Maximum clamp current	I_{CLAMP}	− 4	+ 4	mA	*8
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*8
“L” level maximum output current*4	I_{OL}	—	10	mA	
		—	43	mA	USB I/O
“L” level average output current*5	I_{OLAV}	—	4	mA	
		—	15	mA	USB I/O
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*4	I_{OH}	—	− 10	mA	
		—	− 43	mA	USB I/O
“H” level average output current*5	I_{OHAV}	—	− 4	mA	
		—	− 15	mA	USB I/O
“H” level total maximum output current*6	ΣI_{OH}	—	− 100	mA	
“H” level total average output current	ΣI_{OHAV}	—	− 50	mA	
Power consumption	P_D	—	500	mW	
Operating temperature	Ta	− 40	+ 85	°C	
Storage temperature	T_{STG}	− 55	+ 125	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : V_{CC} must not drop below $V_{SS} − 0.3$ V.

*3 : Be careful not to exceed $V_{CC} + 0.3$ V, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

(Continued)

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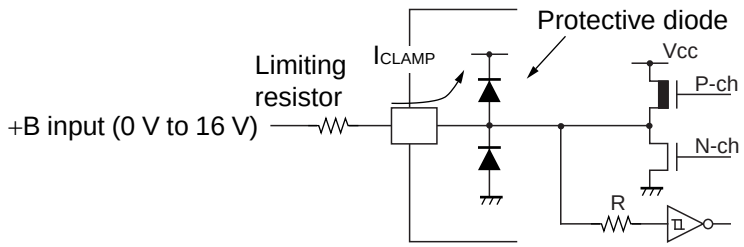
*6 : The total average output current is the average current for all pins over a period of 100 ms.

*7 : If the input current or the maximum input current are limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*8 :
- Corresponding pins:P01, P03, P13 to P17,P50 to P57, P60, P61
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Do not leave +B input pins open.
- Sample recommended circuit

•Input/output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	Not using USB
		3.0	3.6	V	Using USB
Analog power supply voltage	AV_{CC}	2.7	3.6	V	Not using USB AV_{CC} = V_{CC}
		3.0	3.6	V	Using USB AV_{CC} = V_{CC}
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	− 40	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	V_{CC}	Normal operation	—	35	45	mA	CPU : 33 MHz, Peripheral : 33 MHz, Not using USB*1, *3
				—	45	60	mA	CPU : 32 MHz, Peripheral : 32 MHz, Using USB*1, *3
	I_{CCS}		SLEEP mode	—	10	20	mA	Peripheral : 33 MHz, Not using USB*1, *3
				—	20	30	mA	Peripheral : 32 MHz Using USB*1, *3
	I_{CCL}		Sub operation	—	100	300	µA	CPU : 32 kHz, Peripheral : 32 kHz*1, *2, *4
	I_{CCT}		Watch mode	—	70	200	µA	*1, *2, *4
	I_{CCH}		STOP mode	—	45	100	µA	*1, *2
“H” level input voltage	V_{IH}	P00 to P07*5, P10 to P17*6, P22 to P27, P60*7 P72 to P77, P80 to P83	—	$V_{CC} \times 0.7$	—	Vcc + 0.3	V	
“L” level input voltage	V_{IL}	P00 to P07*5, P10 to P17*6, P22 to P27, P60*7 P72 to P77, P80 to P83	—	$V_{SS} - 0.3$	—	$V_{CC} \times 0.3$	V	
“H” level input voltage (hysteresis input)	V_{IHS}	P00 to P07*8, P10 to P17*9, P50 to P57, P60*10, P61, P70, P71, P72 to P77, P80 to P83, PK0, PK1, $\overline{INIT}$, MD0, MD1	—	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
		P20, P21, P22 to P27, PH2, PH3	—	$V_{CC} \times 0.8$	—	$V_{SS} + 5.5$	V	5 V tolerant

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L"level input voltage (hysteresis input)	V_{ILS}	P00 to P07*8, P10 to P17*9, P20, P21, P22 to P27, P50 to P57, P60*10, P61, P70, P71, P72 to P77, P80 to P83, PH2, PH3, PK0, PK1, $\overline{INIT}$, MD0, MD1	—	Vss − 0.3	—	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P50 to P57, P60, P61, P70 to P77, P80 to P83, PH2, PH3, PK0, PK1	V_{CC} = 3.0 V I_{OH} = − 4 mA	V_{CC} − 0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}		V_{CC} = 3.0 V I_{OL} = 4 mA	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	—	—	− 5	—	+ 5	μA	Digital pin
				− 10	—	+ 10	μA	Analog pin
Pull-up resistance value	R_{PU}	Pull-up pin	—	16.6	33	66	kΩ	
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, AVRH	—	—	10	15	pF	

*1 : When opened, all ports are fixed to output

*2 : Ta = + 25 °C and V_{CC} = 3.3 V

*3 : X0 = 8.3 MHz, CPU clock = 33 MHz and X0A = when stopped

*4 : X0 = STOP and X0A = at 32 kHz

*5 : When using as D00 to D07 pin

*6 : When using as D08 to D15 pin

*7 : When using as RDY input

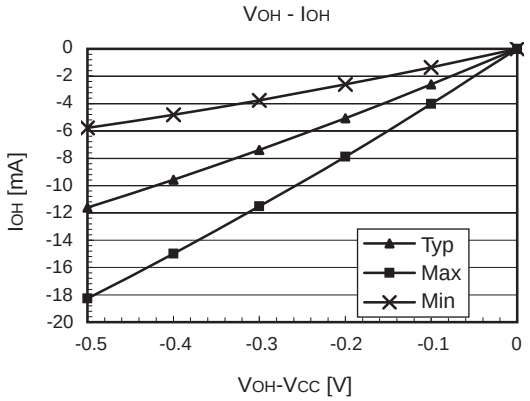
*8 : When using other than D00 to D07 pin

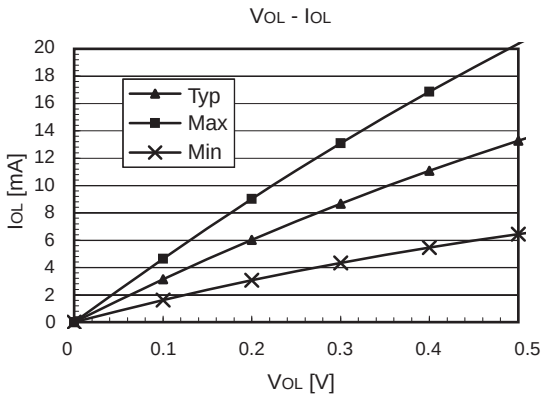
*9 : When using other than D08 to D15 pin

*10 : When using other than RDY input

- **V-I characteristics**

Conditions
Min : Process = Slow, Ta = + 85 °C, V_{CC} = 2.7 V
Typ : Process = Typical, Ta = + 25 °C, V_{CC} = 3.3 V
Max : Process = Fast, Ta = − 40 °C, V_{CC} = 3.6 V





4. AC Characteristics

(1) Main Clock (MCLK) Input Standard

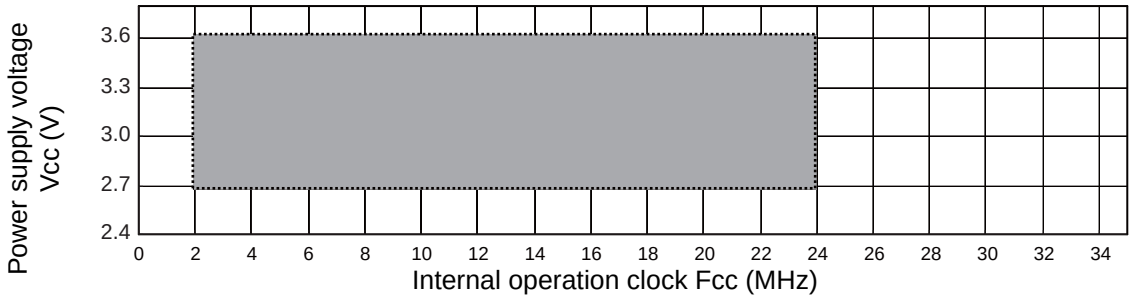
Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

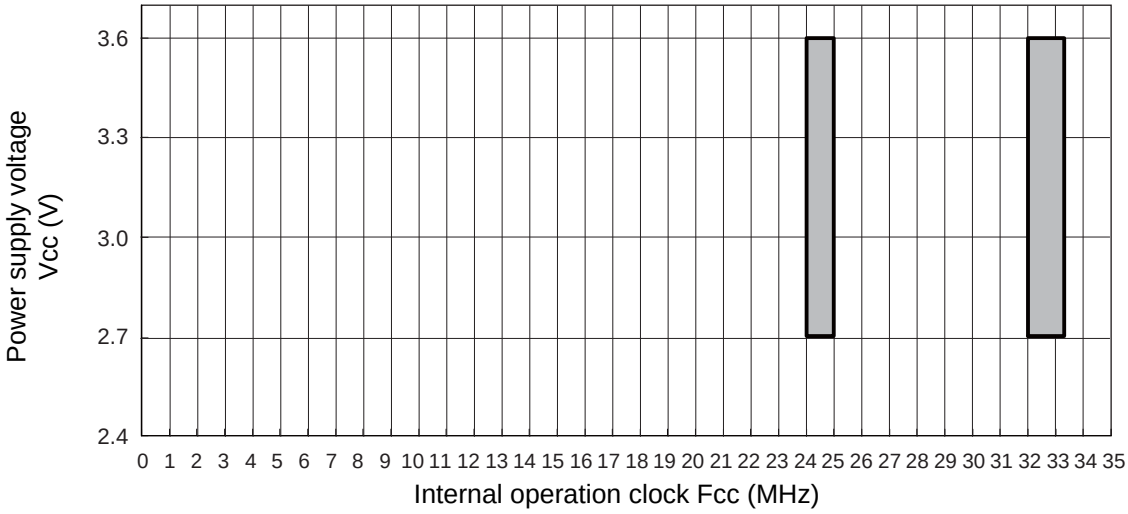
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	—	4	48	MHz	When crystal oscillator is connected
			—	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		—	20.83	250	ns	When using external clock
Input clock pulse width	—		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		—	—	5	ns	When using external clock
Internal operating clock frequency	F_{CS}	—	—	—	33	MHz	Source clock
	F_{CC}	—	—	—	33	MHz	CPU clock
	F_{CP}	—	—	—	33	MHz	Peripheral bus clock
	F_{CT}	—	—	—	33	MHz	External bus clock
Internal operating clock cycle time	t_{CYCS}	—	—	30	—	ns	Source clock
	t_{CYCC}	—	—	30	—	ns	CPU clock
	t_{CYCP}	—	—	30	—	ns	Peripheral bus clock
	t_{CYCT}	—	—	30	—	ns	External bus clock

• Operating guaranteed range (Not using USB)

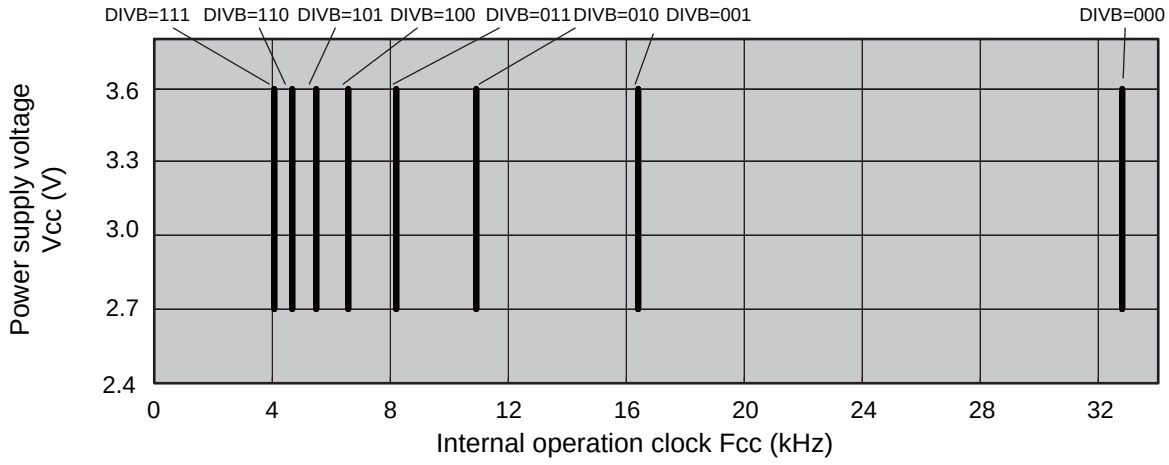
• When the main clock is selected (DIVB=000)



• When the PLL clock is selected (DIVB=000)

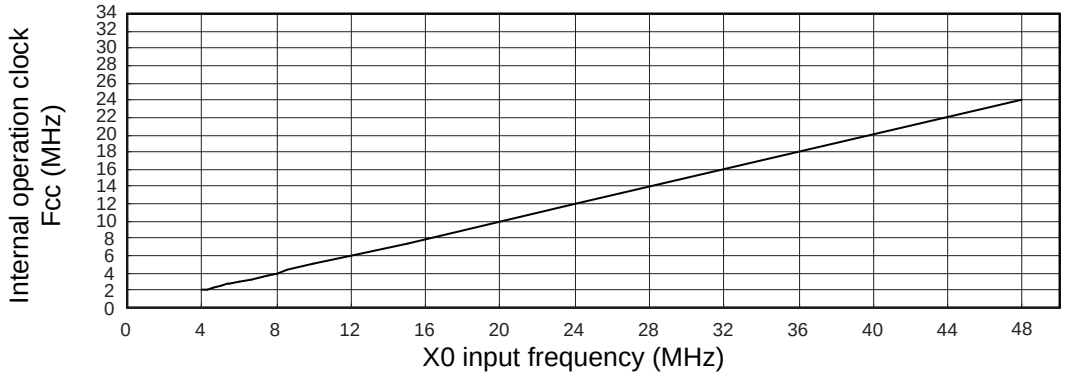


• When the sub clock is selected (F_{CL} = 32.768 kHz)

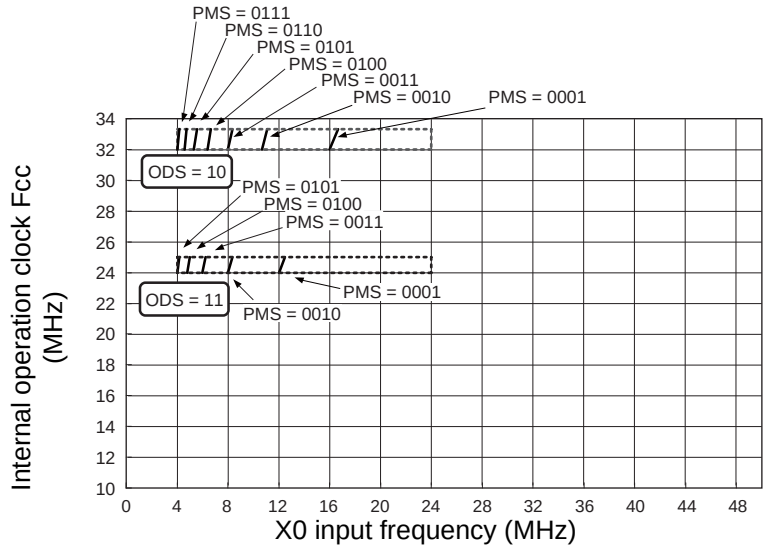


• Example of configuration (Not using USB)

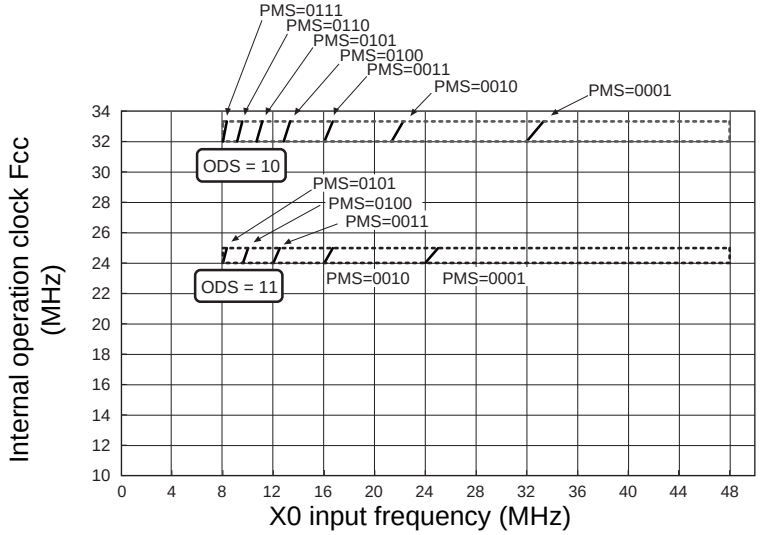
• When the main clock is selected (DIVB=000*1)



• When the PLL clock is selected (DIVB=000*1, PDS=0000*2)

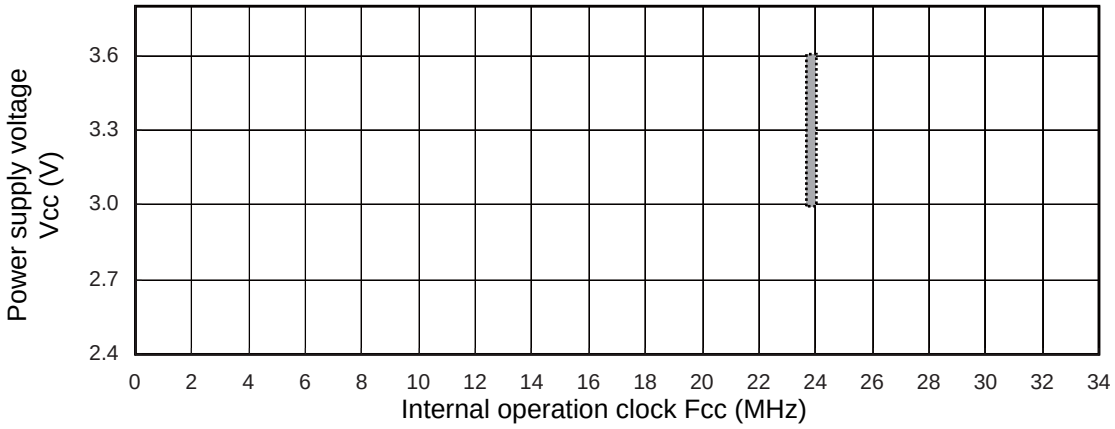


• When the PLL clock is selected (DIVB=000*1, PDS=0001*2)

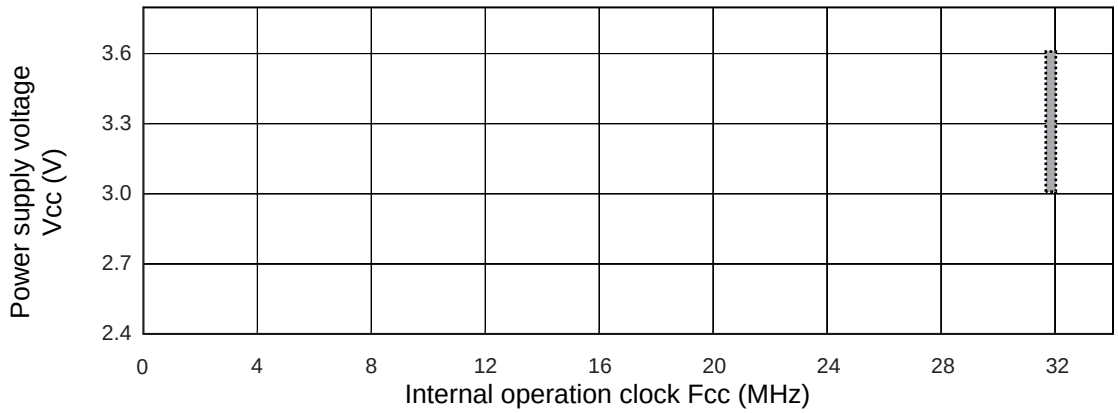


• Operating guaranteed range (at using USB)

• When the main clock is selected (DIVB = 000*1)



• When the PLL clock is selected (DIVB = 000*1, ODS = 10*3, PMS = 0111*4, PDS=0000*2, X0 = 4 MHz or DIVB = 000*1, ODS = 10*3, PMS = 0001*4, PDS = 0010*2, X0 = 48 MHz)



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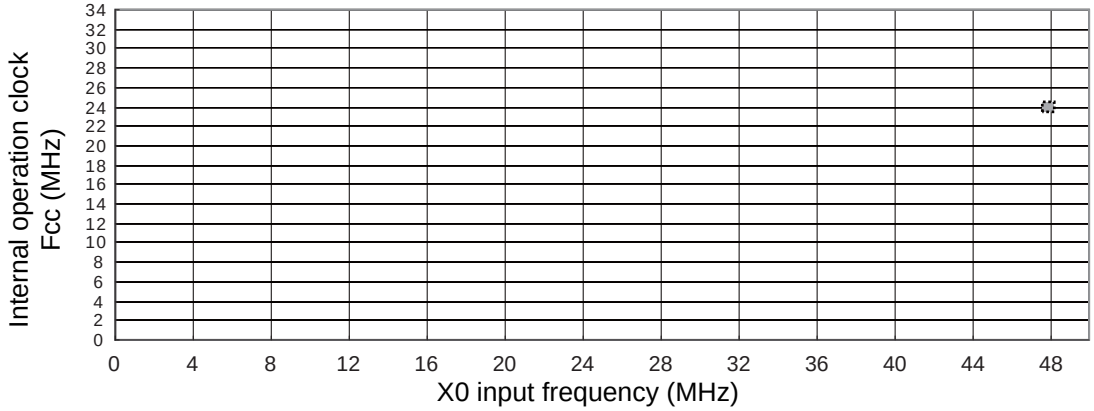
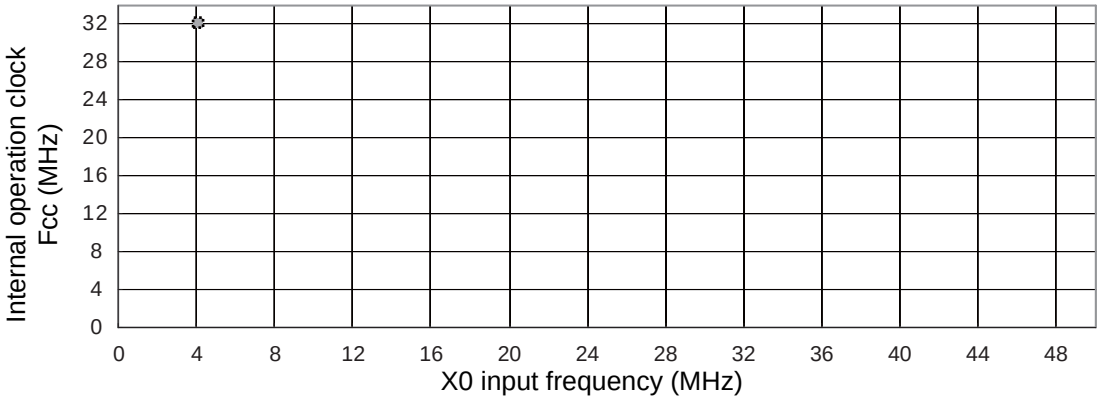
• Example of configuration (at using USB)

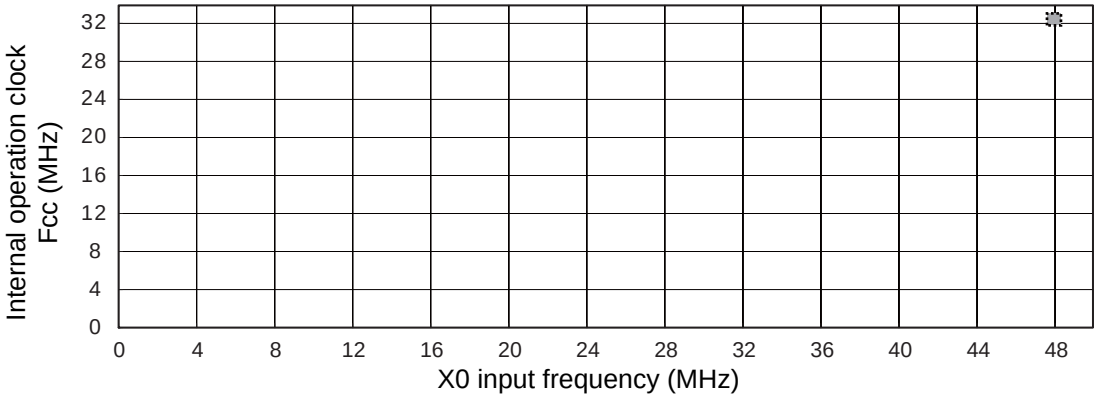
• When the main clock is selected (DIVB = 000*1)



• When the PLL clock is selected (DIVB = 000*1, ODS = 10*3, PMS = 0111*4, PDS = 0000*2)



• When the PLL clock is selected (DIVB=000*1, ODS=10*3, PMS=0001*4, PDS=0010*2)



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*1: The values other than DIVB = 000 are omitted.

*2: The values other than PDS = 0000, 0001,0010 are omitted.

*3: The values other than ODS = 10 are omitted.

*4: The values other than PMS = 0001,0111 are omitted.

Note: DIVB: Base clock division configuration bit
ODS : PLL macro oscillation clock division rate select bit
PDS : PLL input clock division select bit
PMS : PLL clock multiple rate select bit

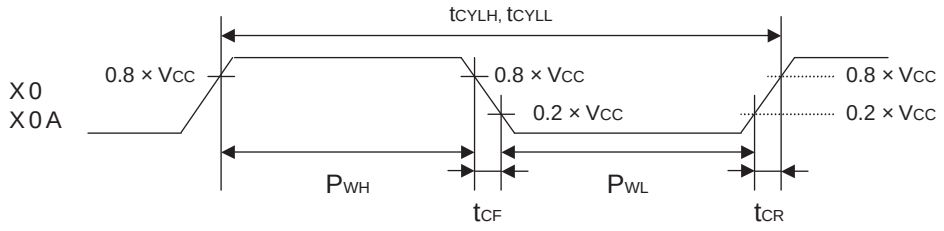
(2) Sub Clock (SBCLK) Input Standard

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When crystal oscillator is connected
			—	—	32.768	—	kHz	When using external clock
Input clock cycle	t_{CYLL}		—	—	30.518	—	µs	When using external clock
Input clock pulse width	—		P_{WH} / t_{CYLL} P_{WL} / t_{CYLL}	45	—	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		—	—	—	200	ns	When using external clock

<When external clock input>



(3) Conditions of PLL

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	600	—	—	µs	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	4	—	24	MHz	
PLL multiple rate	—	4	—	24	multiplied by	ODS × PMS
PLL macro oscillation clock frequency	f_{PLLO}	96	—	100	MHz	

(4) Regulator Voltage Stabilization Wait Time

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Regulator voltage stabilization wait time	t_{REG}	50	—	µs	Time taken for the regulator voltage to stabilize

Notes: • This is the time from when the external power supply stabilizes (after reaching 2.7 V) when USB is not used.
• This is the time from when the external power supply stabilizes (after reaching 3.0 V) when USB is used.

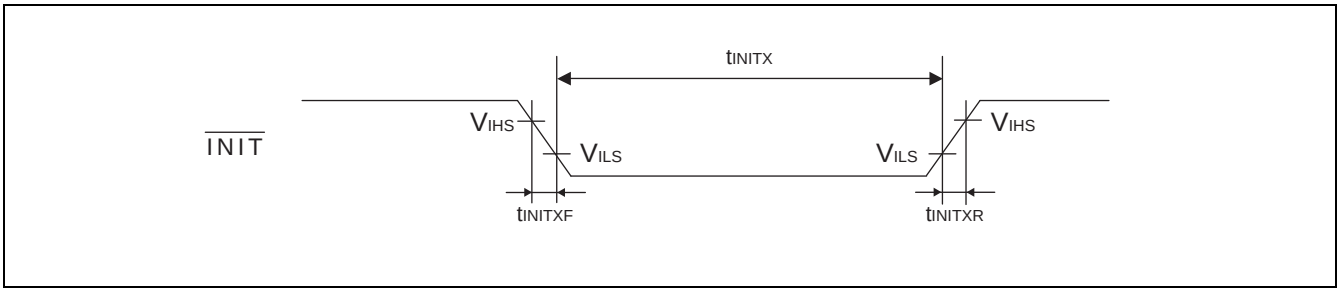
(5) Reset Input Standards

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	t_{INITX}	$\overline{INIT}$	—	Oscillation time of oscillator + 10 t_{CYLH}	—	ns	*
Reset input time (At other times)				10 t_{CYLH}	—	ns	
Reset input rise time and fall time	t_{INITXF}, t_{INITXR}			—	10	ms	

* : After the supply voltage has stabilized, it takes a further 50 μs until the internal supply stabilizes. Hold the input to the $\overline{INIT}$ pin during that period.
- At power-on
- When in stop mode
- When in sub mode and sub watch mode when the main oscillation is stopped.



(6) Clock Output Timing

• t_{CHCL} : t_{CLCH} = 1 : 1 (divided by 1, 2, 4, 6, 8)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK*	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			t_{CYC} / 2 − 5	t_{CYC} / 2 + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			t_{CYC} / 2 − 5	t_{CYC} / 2 + 5	ns

* : This pin is not existed in MB91F668.

Notes: • t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

• When DIVT = 000, be sure to set as DIVB = 000.

• t_{CHCL} : t_{CLCH} = 1 : 2 (divided by 3)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK*	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			1 / 3 t_{CYC} − 5	1 / 3 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			2 / 3 t_{CYC} − 5	2 / 3 t_{CYC} + 5	ns

* : This pin is not existed in MB91F668.

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

• t_{CHCL} : t_{CLCH} = 2 : 3 (divided by 5)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK*	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			2 / 5 t_{CYC} − 5	2 / 5 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			3 / 5 t_{CYC} − 5	3 / 5 t_{CYC} + 5	ns

* : This pin is not existed in MB91F668.

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

• t_{CHCL} : t_{CLCH} = 3 : 4 (divided by 7)

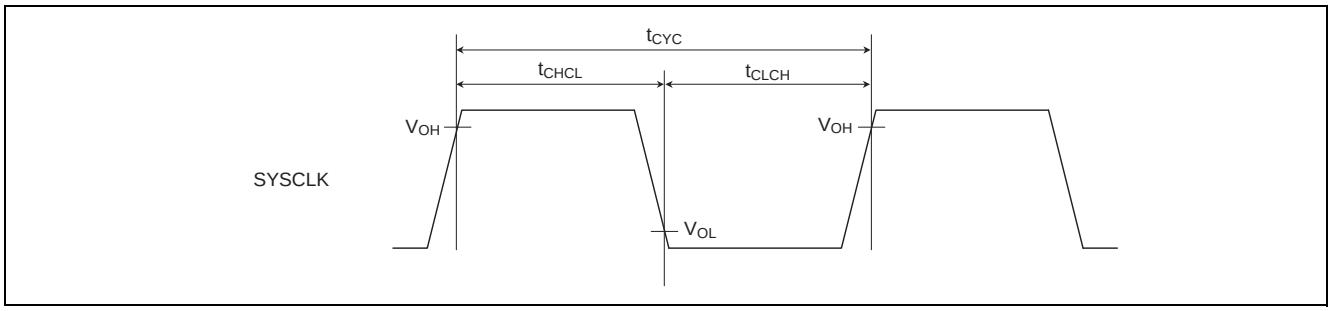
Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK*	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			3 / 7 t_{CYC} − 5	3 / 7 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			4 / 7 t_{CYC} − 5	4 / 7 t_{CYC} + 5	ns

* : This pin is not existed in MB91F668.

Note: t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.



(7) External Bus Access Read/Write Operation

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

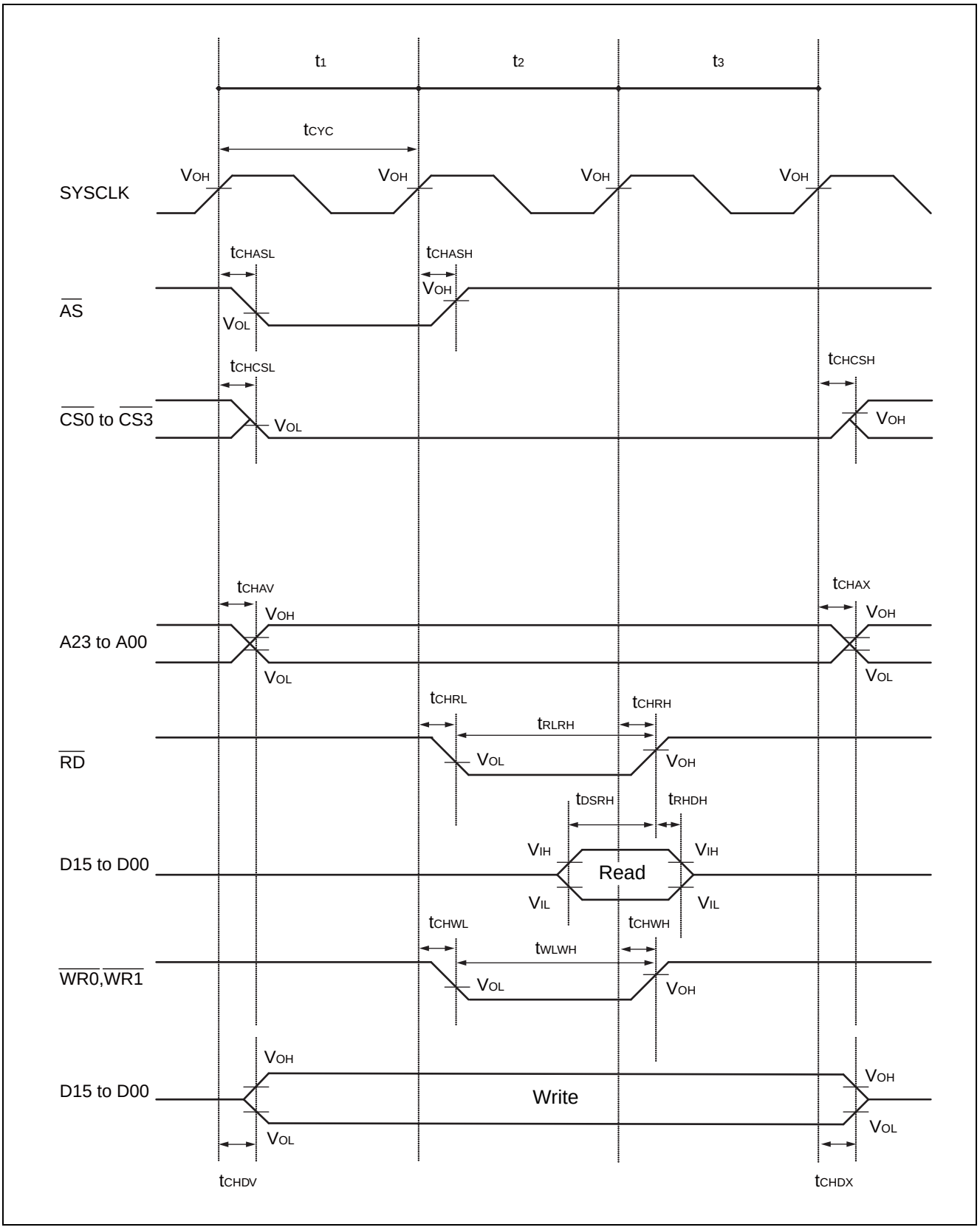
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
$\overline{AS}$ delay time	t_{CHASL}	SYSCLK*2, $\overline{AS}$	—	0.6	10	ns	
	t_{CHASH}						
$\overline{CS0}$ to $\overline{CS3}$ delay time	t_{CHCSL}	SYSCLK*2, $\overline{CS0}$ to $\overline{CS3}$*2		0.6	10	ns	
	t_{CHCSH}						
Address delay time	t_{CHAV}	SYSCLK*2, A23 to A00		0.6	10	ns	
	t_{CHAX}						
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK*2, $\overline{RD}$		0.6	10	ns	
	t_{CHRH}						
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} − 10	—	ns	*1
Data setup → $\overline{RD}$↑ time	t_{DSRH}	$\overline{RD}$, D15 to D00		18	—	ns	
$\overline{RD}$↑→ data hold time	t_{RHDH}			0	—	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK*2, $\overline{WR0}$, $\overline{WR1}$*2		0.6	10	ns	
	t_{CHWH}						
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$*2		t_{CYC} − 10	—	ns	*1
SYSCLK↑→ Data output time	t_{CHDV}	SYSCLK*2, D15 to D00		0.6	15	ns	
SYSCLK↑→ Data hold time	t_{CHDX}			0.6	15	ns	

*1 : When the bus timing is delayed by an automatic wait insertion or RDY input, add the time (t_{CYC} × the number of delay cycles added) to this rating.

*2 : This pin is not existed in MB91F668.

Note: When the external load capacitance C = 50 pF.


t1
t2
t3
tCYC
SYSCLK
VOH
VOH
VOH
VOH
tCHASL
tCHASH
AS
VOH
VOL
tCHCSL
tCHCSH
CS0 to CS3
VOL
VOH
tCHAV
tCHAX
A23 to A00
VOH
VOH
VOL
VOL
tCHRL
tCHRH
tRLRH
RD
VOL
VOH
tDSRH
tRHDH
D15 to D00
VIH
VIH
Read
VIL
VIL
tCHWL
tCHWH
tWLWH
WR0,WR1
VOL
VOH
D15 to D00
VOH
VOH
Write
VOL
VOL
tCHDV
tCHDX

(8) Multiplexed Bus Access Read/Write Operation

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

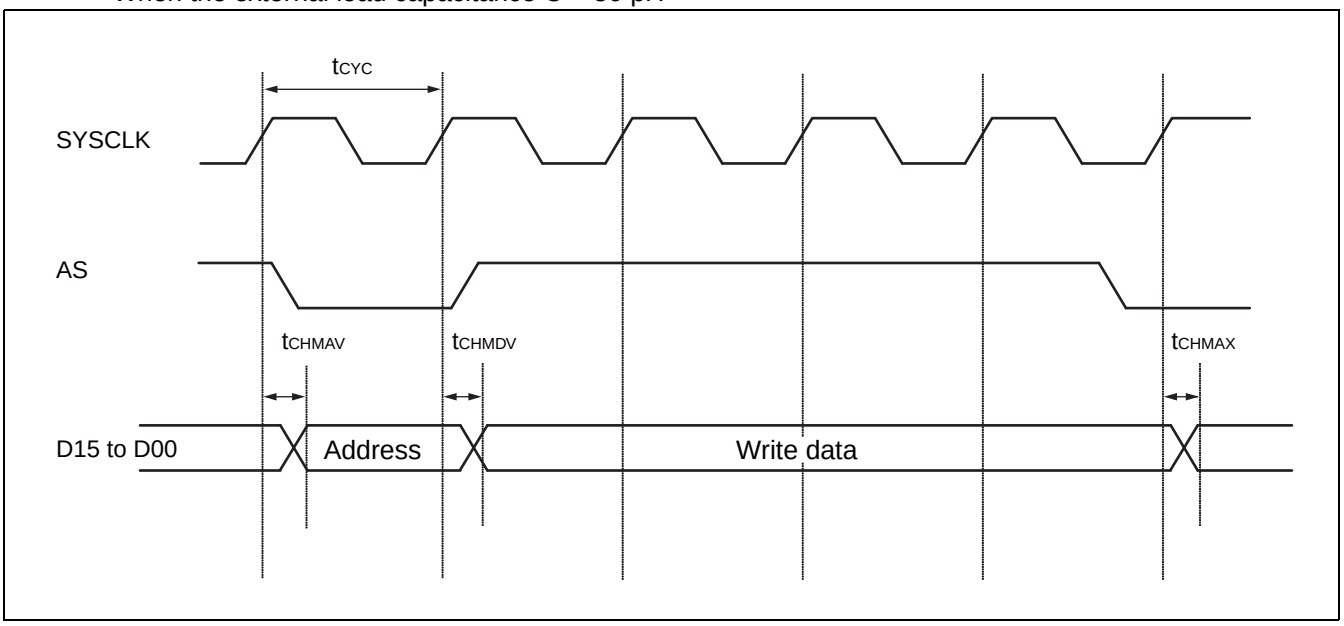
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
SYSCLK↑ → D15 to D00 address delay time	t_{CHMAV}, t_{CHMAX}	SYSCLK*, D15 to D00 (address)	—	0.6	15	ns
SYSCLK↑ → D15 to D00 data delay time	t_{CHMDV}			0.6	15	ns

*: This pin is not existed in MB91F668.

Notes: • The ratings not listed here are the same as the normal bus interface.

• When the external load capacitance C = 50 pF.

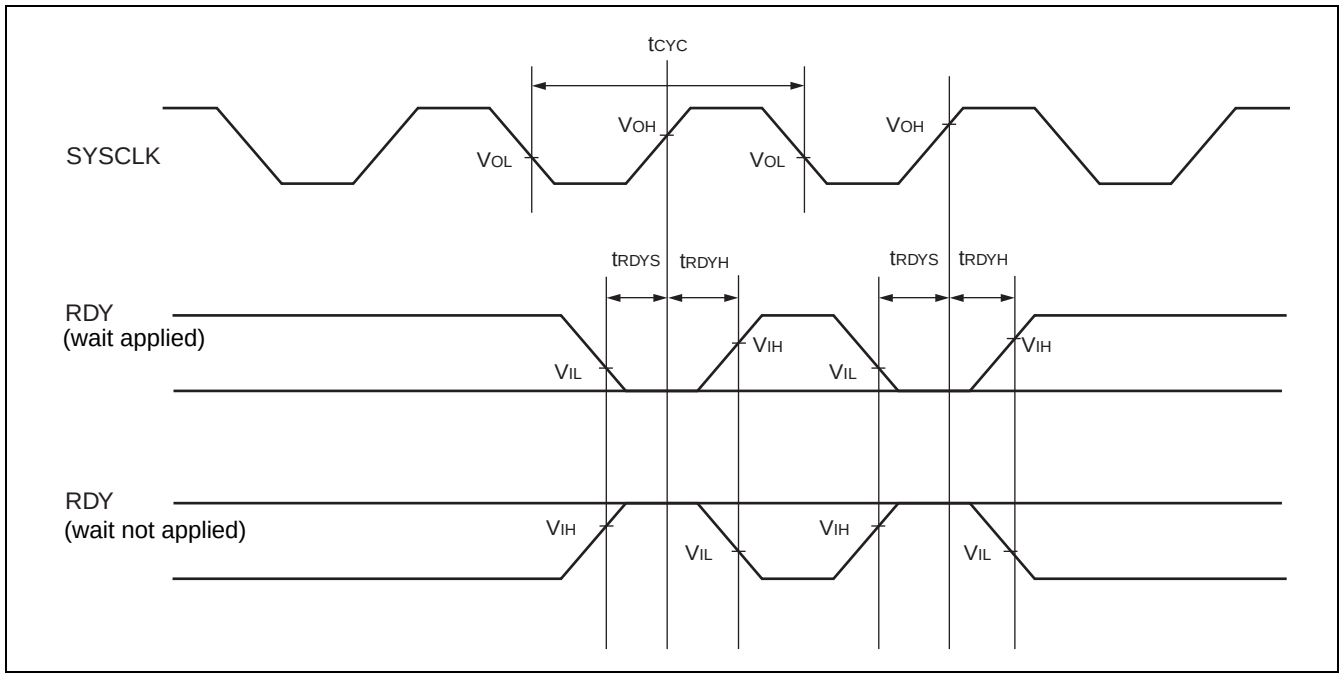


(9) Ready Input Timing (MB91F669 only)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK, RDY	—	18	—	ns
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK, RDY		0	—	ns



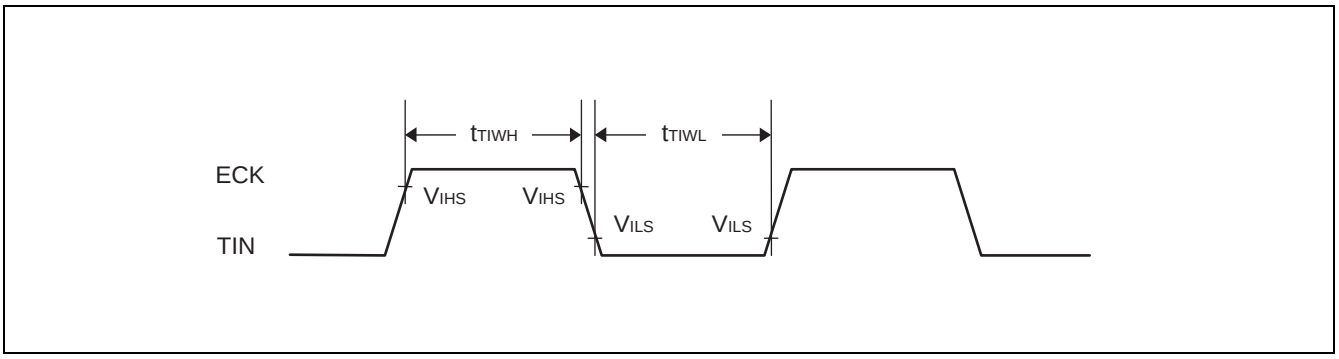
(10) Base Timer Input Timing

• Timer input timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (When used as ECK, TIN)	—	2 t_{CYCP}	—	ns

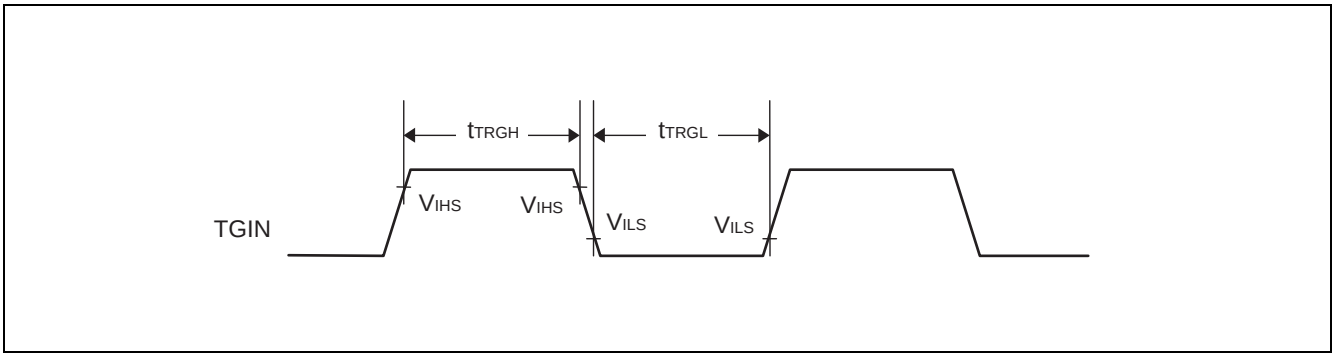


• Trigger Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (When used as TGIN)	—	2 t_{CYCP}	—	ns



(11) Synchronous serial (CSIO) timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

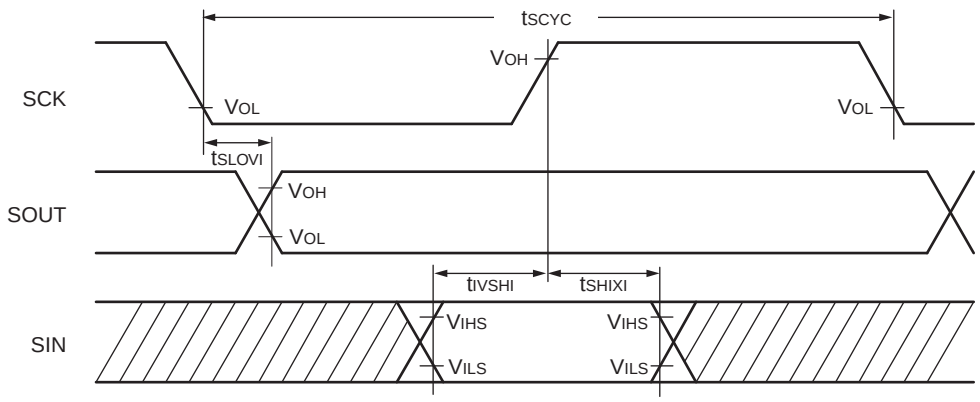
• Synchronous serial (SPI = 0, SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn, SOUTn		− 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn, SOUTn		—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

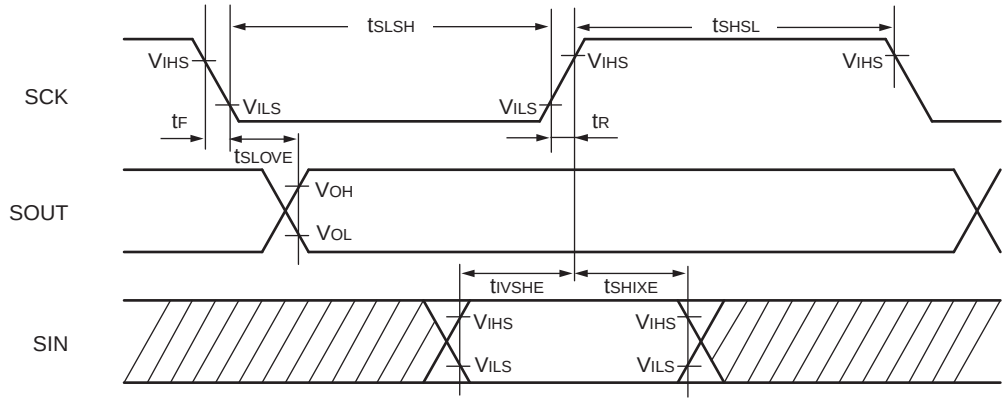
Notes: • The above standards apply to CLK synchronous mode.

• t_{CYCP} indicates the peripheral clock cycle time.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

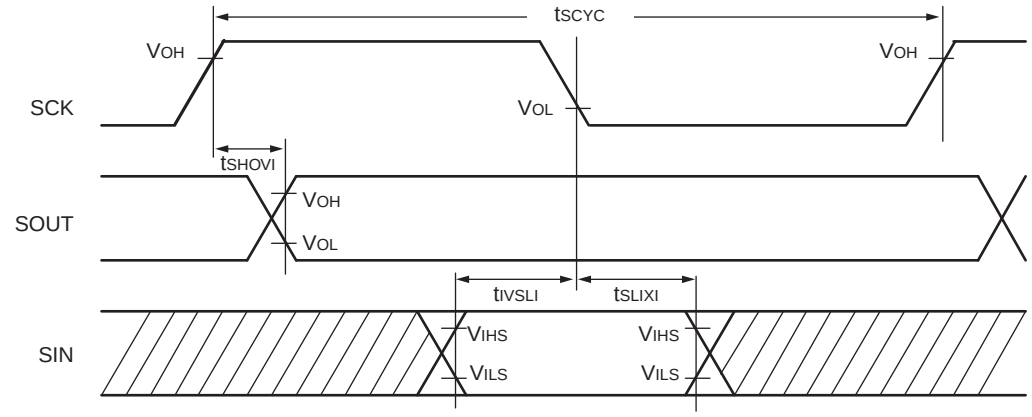
• Synchronous serial (SPI = 0, SCINV = 1)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn, SOUTn		− 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn, SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn, SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn, SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn, SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

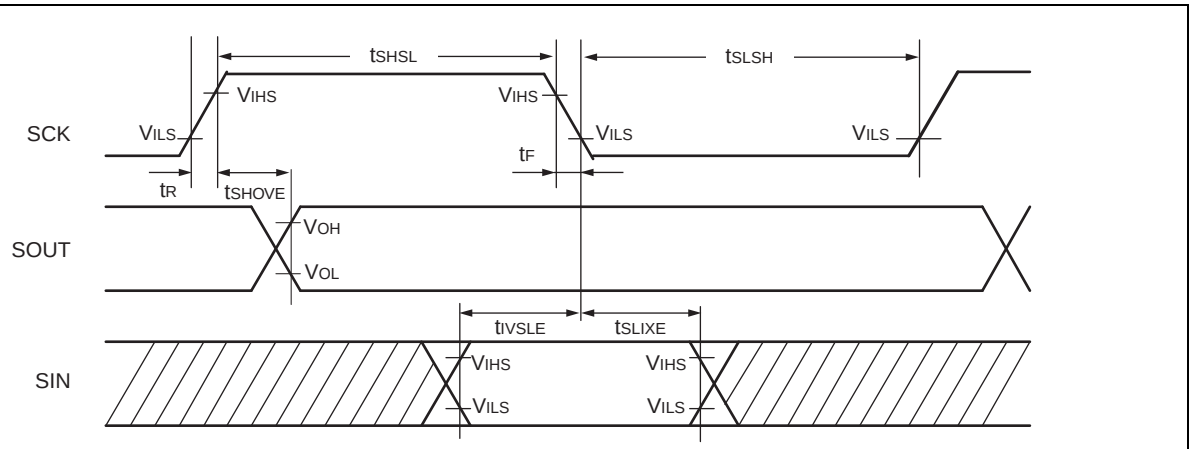
Notes: • The above standards apply to CLK synchronous mode.

• t_{CYCP} indicates the peripheral clock cycle time.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

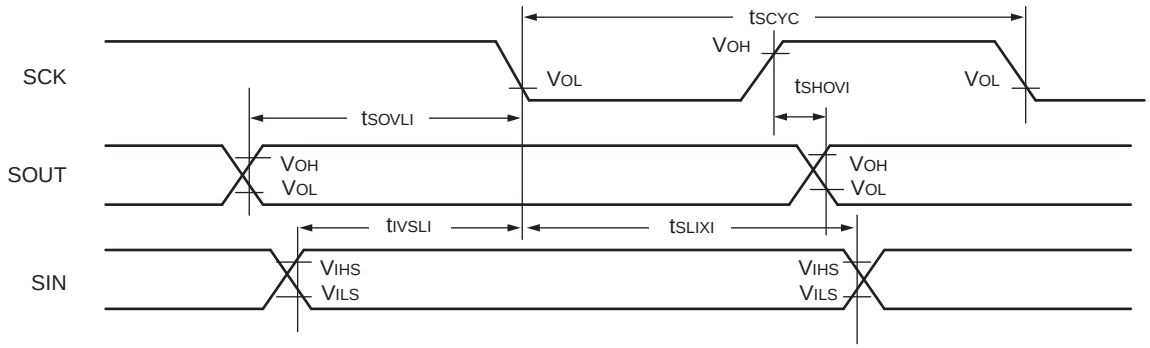
• Synchronous serial (SPI = 1,SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn, SOUTn		− 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn, SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
SOUT → SCK ↓ delay time	t_{SOVLI}	SCKn, SOUTn		$2t_{CYCP}$ − 30	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn, SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn, SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn, SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

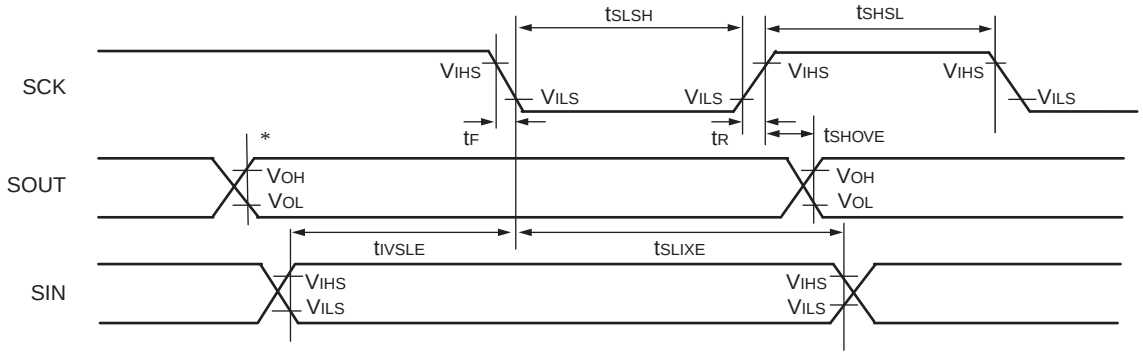
Notes: • The above standards apply to CLK synchronous mode.

• t_{CYCP} indicates the peripheral clock cycle time.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

* : Changes when writing to TDR register

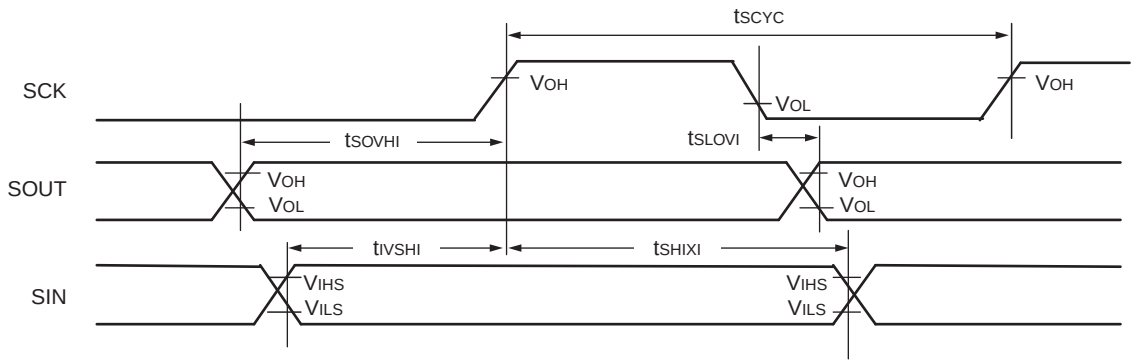
• Synchronous serial (SPI = 1, SCINV = 1)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn, SOUTn		− 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	ns
SOUT → SCK ↑ delay time	t_{SOVHI}	SCKn, SOUTn		$2t_{CYCP}$ − 30	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn, SOUTn		—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

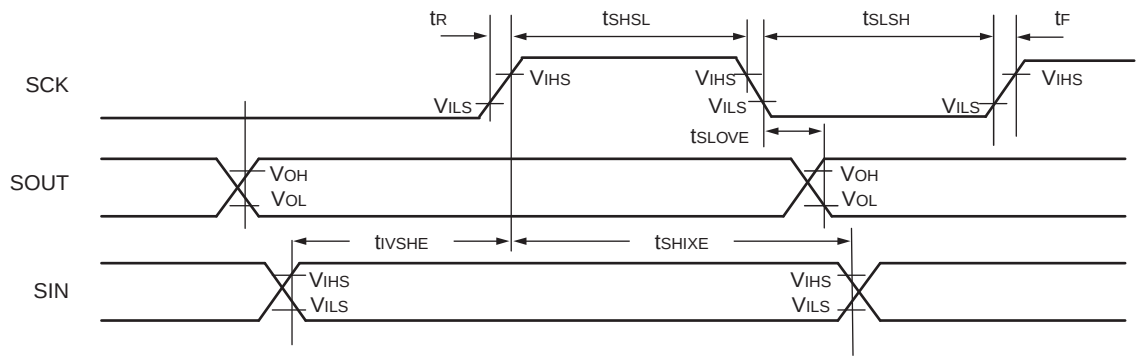
Notes: • The above standards apply to CLK synchronous mode.

• t_{CYCP} indicates the peripheral clock cycle time.

• When the external load capacitance C = 50 pF.



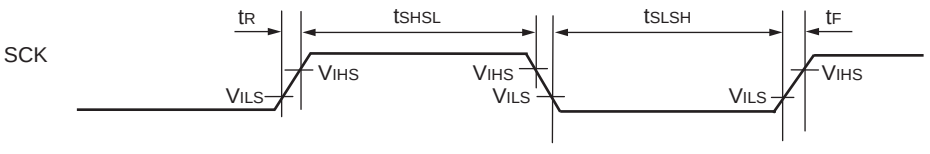
MS bit = 0



MS bit = 1

• External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock “L” pulse width	t_{SLSH}	C_L = 50 pF	t_{CYCP} + 10	—	ns
Serial clock “H” pulse width	t_{SHSL}		t_{CYCP} + 10	—	ns
SCK fall time	t_F		—	5	ns
SCK rise time	t_R		—	5	ns



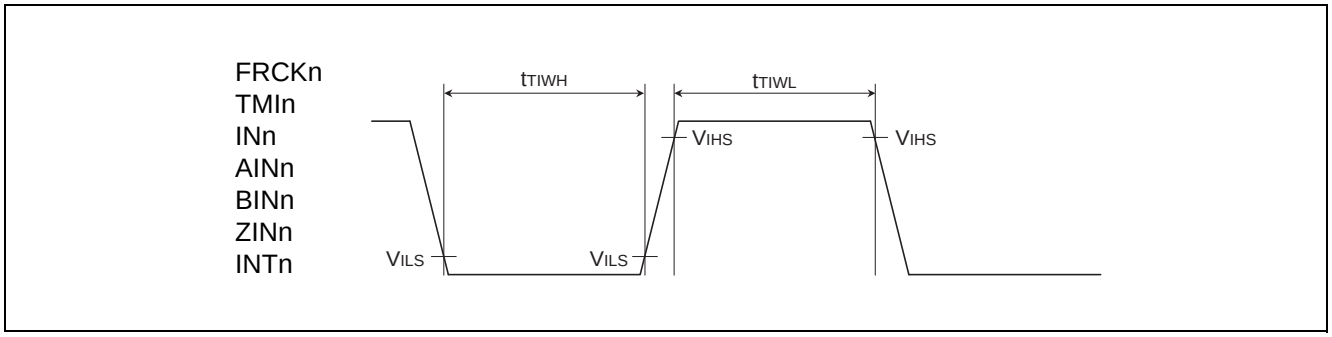
(12) Free-run Timer Clock, Reload Timer Event Input, Up/down Counter Input, Input Capture Input, Interrupt Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	FRCKn, TMIn, INn, AINn, BINn, ZINn	—	2 t_{CYCP}	—	ns	*1
		INTn	—	3 t_{CYCP}	—	ns	*1
			—	1.0	—	µs	*2

*1 : t_{CYCP} indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.

*2 : When in stop mode, in main timer mode, or in watch mode.

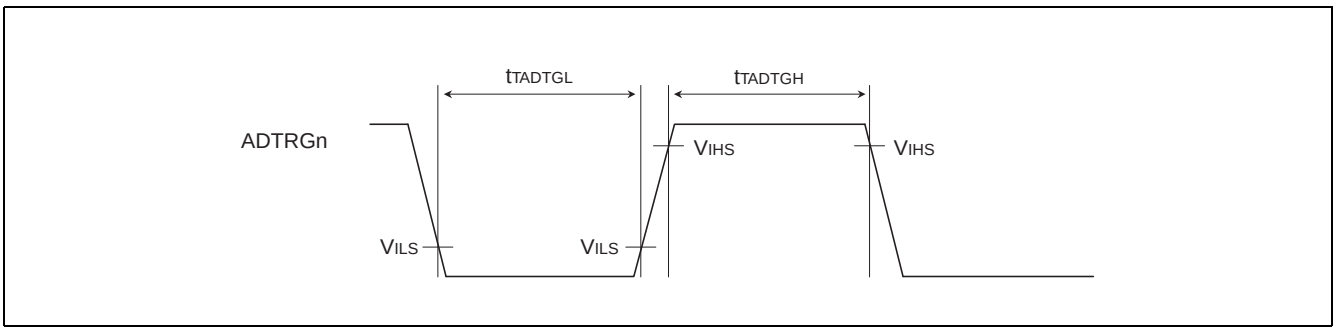


(13) A/D Converter Trigger Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	t_{TADTGL}, t_{TADTGH}	ADTRGn	—	2 t_{CYCP}	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.



(14) I²C Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

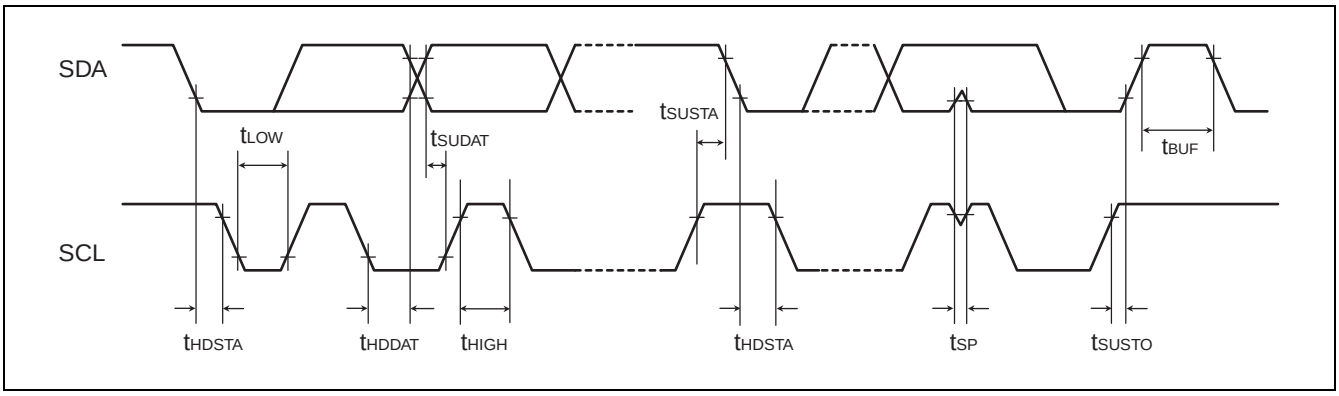
Parameter	Symbol	Pin name	Condi-tions	Typical mode		High-speed mode*3		Unit
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCKn (SCLn)	C_L = 50 pF, R = (Vp/I_{OL}) *1	0	100	0	400	kHz
"(Repeated) START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOUTn (SDAn) , SCKn (SCLn)		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCKn (SCLn)		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCKn (SCLn)		4.0	—	0.6	—	µs
"Repeated START condition" setup time SCL ↑→ SDA ↓	t_{SUSTA}	SCKn (SCLn)		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOUTn (SDAn) , SCKn (SCLn)		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑→ SCL↑	t_{SUDAT}	SOUTn (SDAn) , SCKn (SCLn)		250	—	100	—	ns
"STOP condition" setup time SCL↑→ SDA↑	t_{SUSTO}	SOUTn (SDAn) , SCKn (SCLn)		4.0	—	0.6	—	µs
Bus free time between "STOP condition" and "START condition"	t_{BUF}	—		4.7	—	1.3	—	µs
Noise filter	t_{SP}	—	—	2 t_{CYCP} *4	—	2 t_{CYCP} *4	—	ns

*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4 : t_{CYCP} is the peripheral clock cycle time. To use I²C, set the peripheral bus clock at 8 MHz or more.


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

5. Electrical Characteristics for the A/D Converter

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	− 5	—	+ 5	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V
Linearity error	—	− 3.5	—	+ 3.5	LSB	
Differential linearity error	—	− 3	—	+ 3	LSB	
Zero transition voltage	AN0 to AN11*4	− 1.5	+ 0.5	+ 4	LSB	
Full transition voltage	AN0 to AN11*4	AVRH − 4	AVRH − 1.5	AVRH + 0.5	LSB	
Compare time	—	0.72*3	—	—	µs	PCLK = 33 MHz
Conversion time	—	1.2*1	—	—	µs	PCLK = 33 MHz
Power supply current (analog + digital)	AV_{CC}	—	—	3.5	mA	D/A stopped
		—	—	11	µA	At power-down*2
Reference power supply current (between AVRH and AV_{SS})	AVRH	—	—	0.6	mA	AVRH = 3.0 V
		—	—	5	µA	At power-down*2
Analog input capacity	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN11*4	—	—	10	µA	
Analog input voltage	AN0 to AN11*4	AV_{SS}	—	AVRH	V	
Standard voltage	AVRH	AV_{SS}	—	AV_{CC}	V	

*1 : Depending on the clock cycle supplied to peripheral resources.
Ensure that it satisfies the value; PCLK cycle × more than 4 + the value calculated from (Equation 1).
The condition of the minimum conversion time is when PCLK = 33 MHz, the value of sampling time: 0.424 µs, external impedance: 1.4 kΩ or less and compare time: 0.72 µs.

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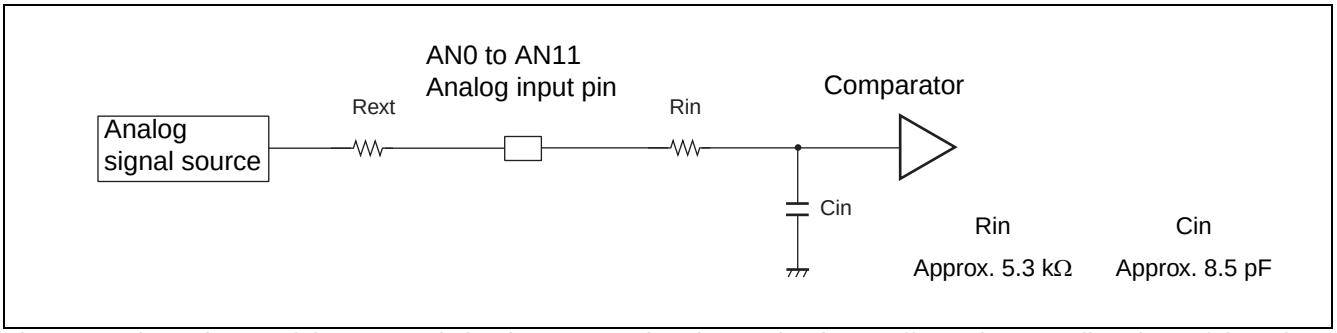
*2 : The current when the CPU is in stop mode and the A/D converter is not operating.

*3 : Compare time = {(CT + 1) × 10 + 4} × peripheral clock (PCLK) period. (CT indicates compare time setting bits.)
The condition of the minimum compare time is when CT = 1 and PCLK = 33 MHz.

*4 : There are no AN10 and AN11 in MB91F668.



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of T_S calculated from the following equation.

(Equation 1) $Ts = (Rin + Rext) \times Cin \times 7$

Ts : Sampling time
Rin : Input resistance of A/D = 5.3 kΩ
Cin : Input capacitance of A/D = 8.5 pF
Rext : Output impedance of external circuit

If the sampling time is set as 600 ns,

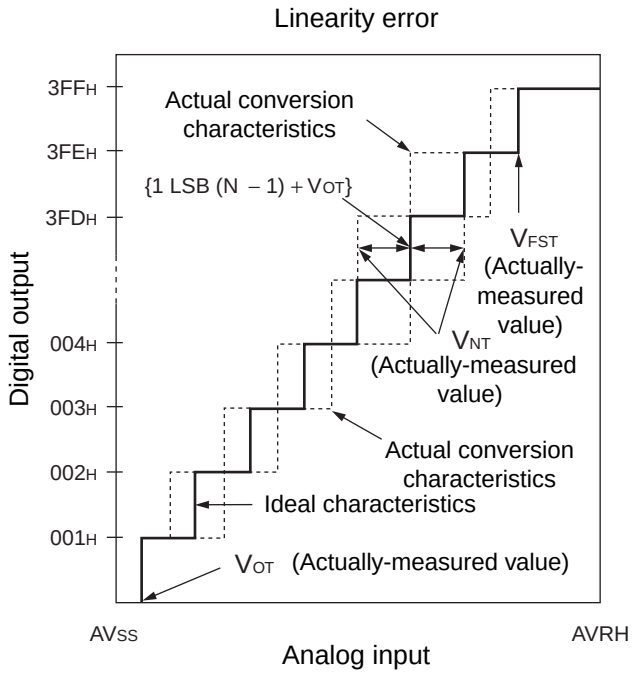
$600\ ns \geq (5.3\ k\Omega + Rext) \times 8.5\ pF \times 7$

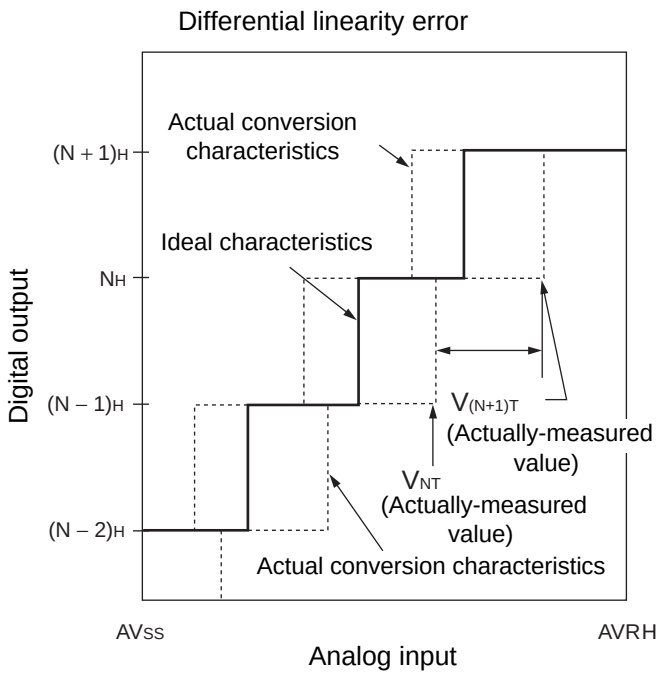
$\therefore Rext \leq 4.8\ k\Omega$

And the impedance of the external circuit therefore needs to be 4.8 kΩ or less.

• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0000000000←→0000000001) and the full-scale transition point (1111111110←→1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.





$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.
V_{NT} : Voltage at which the digital output changes from $(N - 1)_H$ to N_H.

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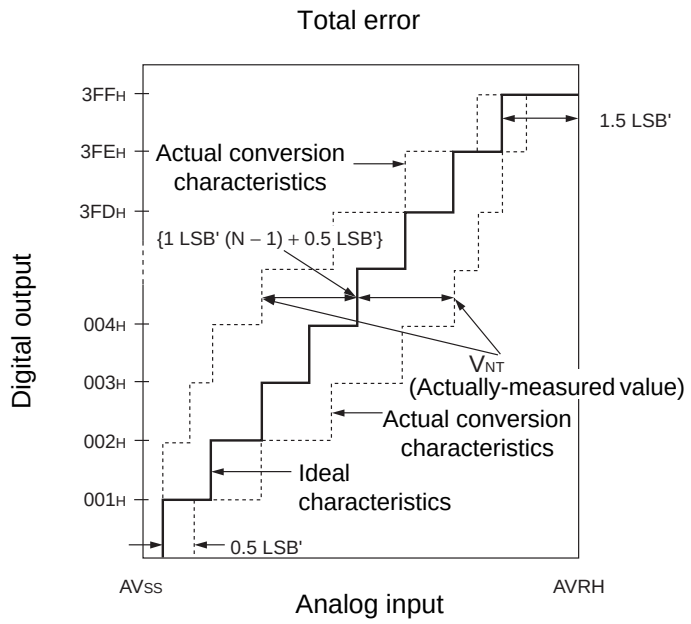

$$1\ \text{LSB' (Ideal value)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (\text{N} - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB [V]

6. USB Characteristics

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter		Sym-bol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input High level voltage	V_{IH}	UDP, UDM	—	2.0	V_{CC} + 0.3	V	*1
	Input Low level voltage	V_{IL}		—	V_{SS} − 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		—	0.2	—	V	*2
	Differential common mode input voltage	V_{CM}		—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		—	1.3	2.0	V	*4
	Rise time	t_{FR}		—	4	20	nS	*5
	Fall time	t_{FF}		—	4	20	nS	*5
	Rise/fall time matching	t_{RFM}		—	90	111.11	%	*5
	Output impedance	Z_{DRV}		—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C_{EDGE}		—	—	75	pF	*6
Series resistance		R_S		—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 [V], V_{IH} (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

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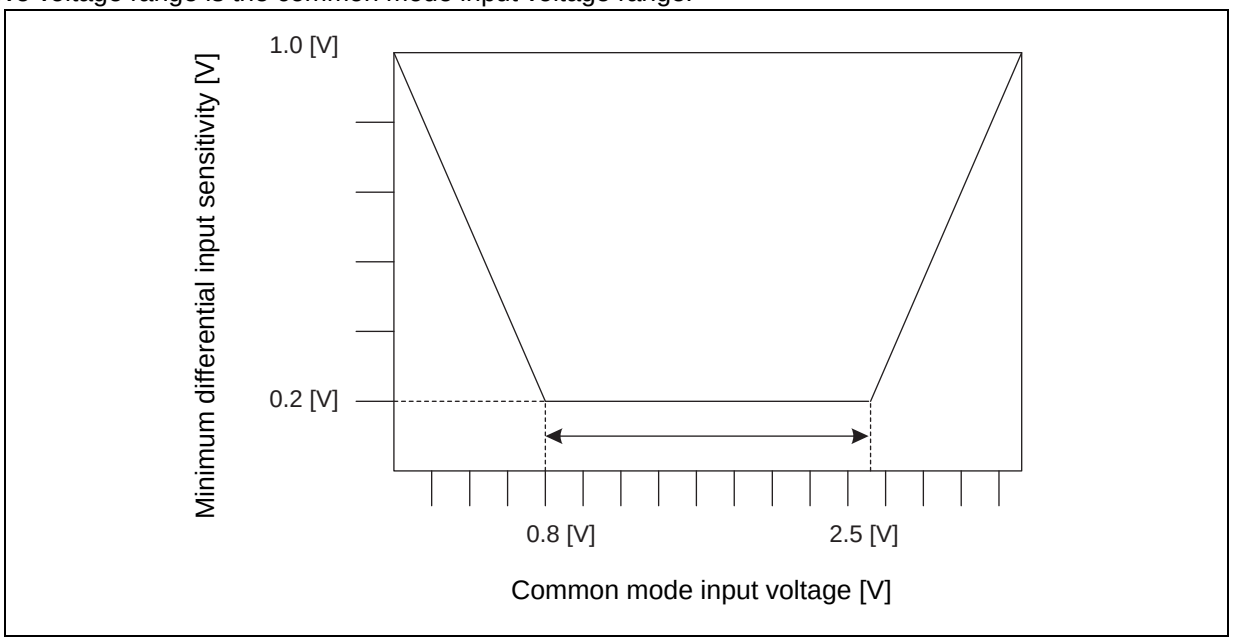
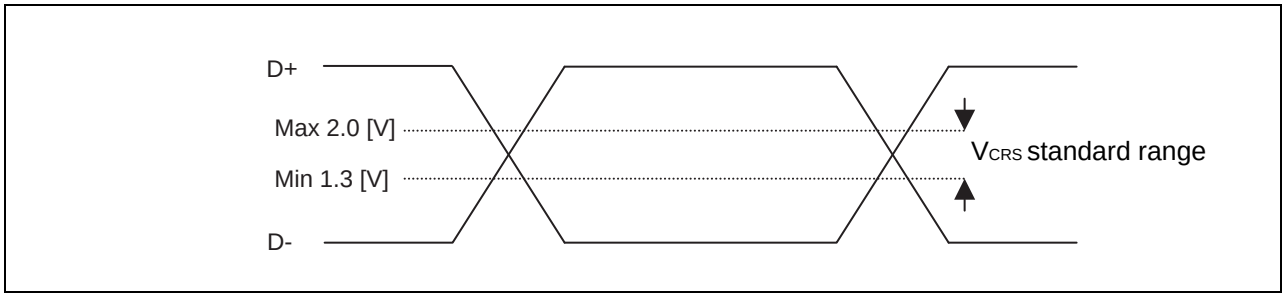
*2 : Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 [mV] of differential input sensitivity when the differential data input is within 0.8 [V] to 2.5 [V] to the local ground reference level.
Above voltage range is the common mode input voltage range.

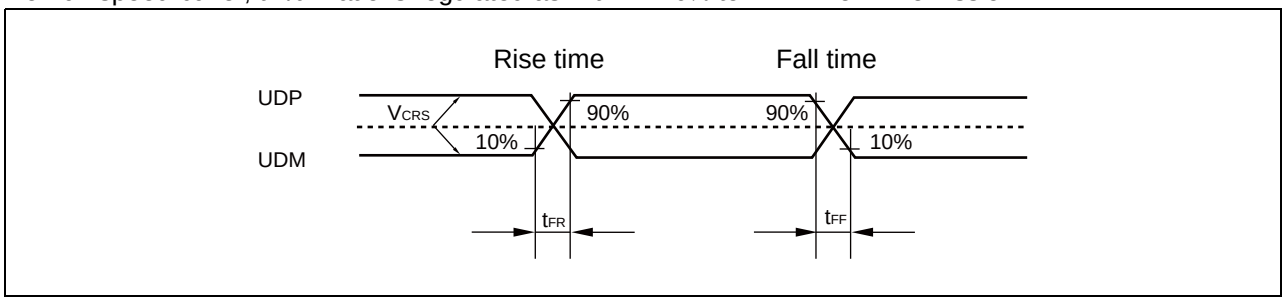


*3 : The output drive capability of the driver is below 0.3 [V] at Low-State (V_{OL}) (to 3.6 [V] and 1.5 kΩ load), and 2.8 [V] or above (to the V_{SS} and 15 kΩ load) at High-State (V_{OH}).

*4 : The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 [V] to 2.0 [V].



*5 : Regarding t_{FR}, t_{FF}, t_{RFM}
They indicate rise time (Trise) and fall time (Tfall) of the differential data signal.
They are defined by the time between 10% to 90% of the output signal voltage.
For full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ±10% to minimize RFI emission.



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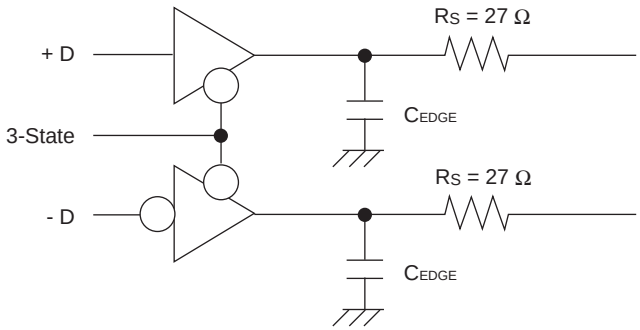
*6 : The place to connect transceiver edge rate control capacitance C_{EDGE}
For this USB I/O, it is recommended to use C_{EDGE} control capacitor.
For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 to 50 [pF] (recommended value : 47 [pF] ≒ 50[pF]) to D + and D − lines when implementing on the board.



Driver output impedance 3 Ω to 19 Ω
Rs serial resistance value 25 Ω to 30 Ω
Please apply 27 Ω of serial resistance value as a recommended value.

7. Flash Memory Write/Erase Characteristics

(V_{CC} = 3.3 V, Ta = + 25 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes write time prior to internal erase
Half word (16bits) write time	—	23	370	μs	Not including system-level overhead time.
Chip erase time*1	—	10.8	43.2	s	Excludes write time prior to internal erase
Erase/write cycles	10000	—	—	cycle	Average Ta ≤ + 85 °C
Flash memory data hold time	10*2	—	—	year	Average Ta ≤ + 85 °C

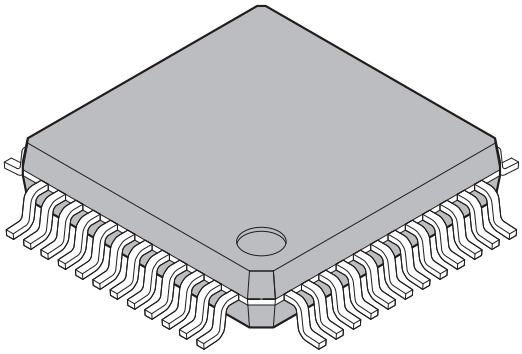
*1 : The chip erase time is the sector erase time multiplied across all sectors.

*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ ORDERING INFORMATION

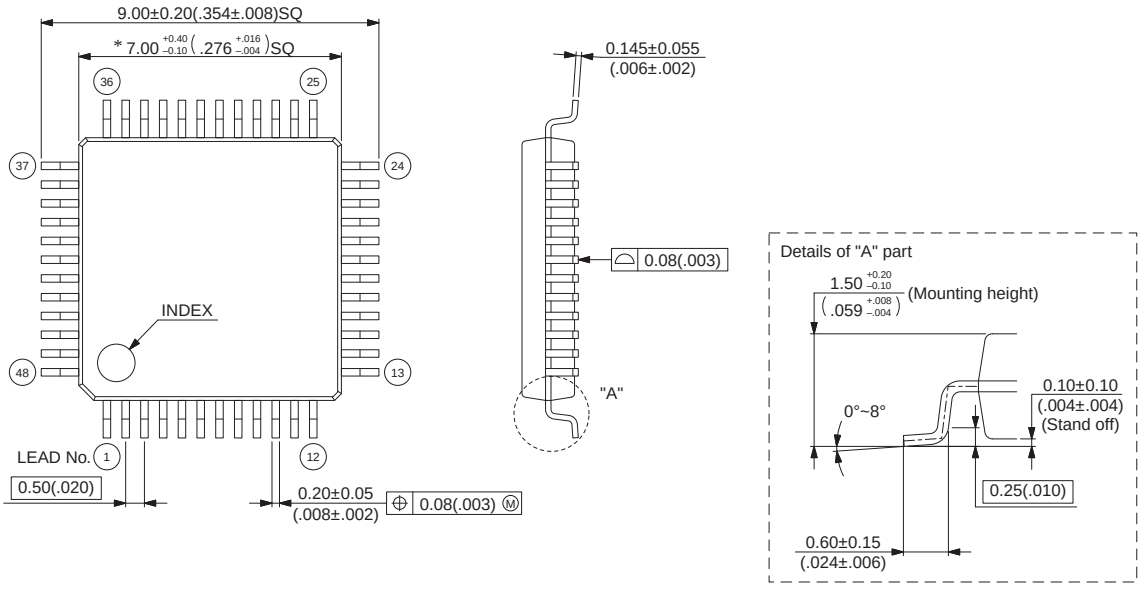
Part number	Package
MB91F669PMC	64-pin plastic LQFP (FPT-64P-M24)
MB91F668PMC	48-pin plastic LQFP (FPT-48P-M26)

■ PACKAGE DIMENSION

48-pin plastic LQFP		
 (FPT-48P-M26)	Lead pitch	0.50 mm
	Package width × package length	7 mm × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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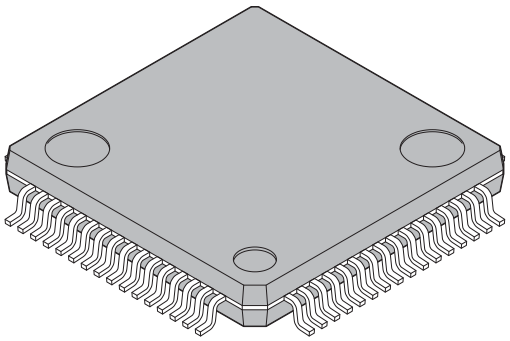
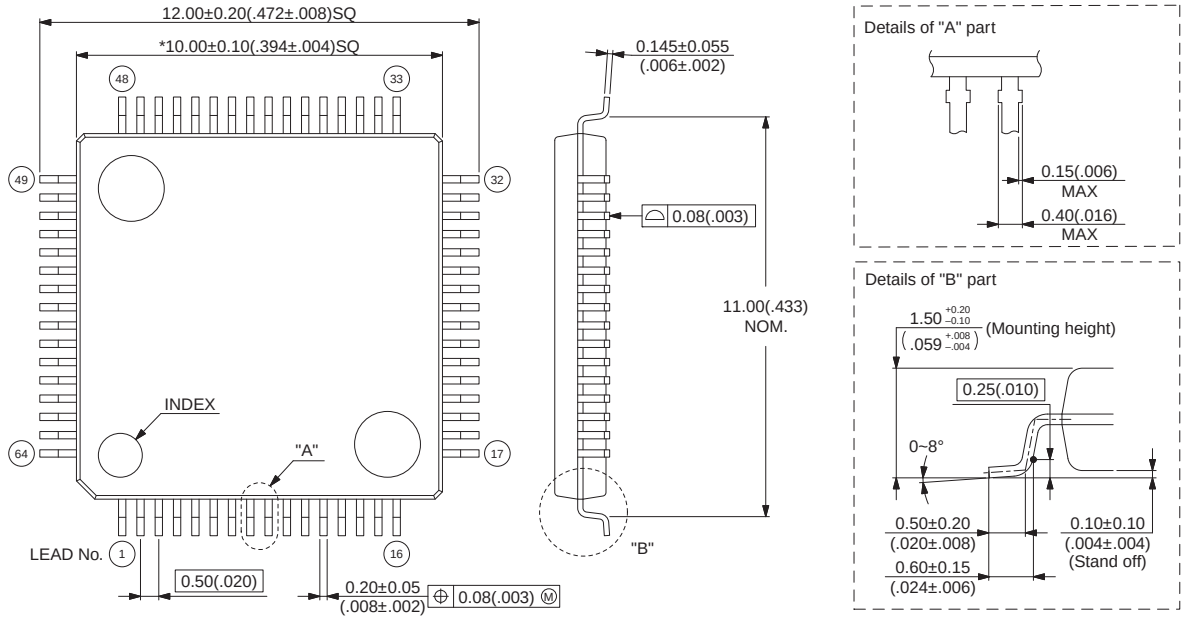
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 mm × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Code (Reference)	P-LFQFP64-10×10-0.50
(FPT-64P-M24)		

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
4	■ FEATURES	Changed the explanation of “USB function / HOST”. (Supports Full-Speed only → USB2.0 Full-Speed supported)
34	■ I/O MAP	Corrected “Initial value after reset”. (ADCHE: -------- -------- ----1111 11111111→ -------- 111111-- ----1111 11111111)"
61	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Changed “Value” for “Power supply current”.

The vertical lines marked in the left side of the page show the changes.

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