1165913

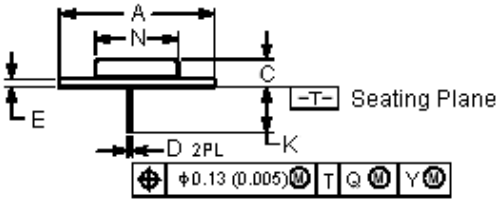
Complementary silicon power transistors.

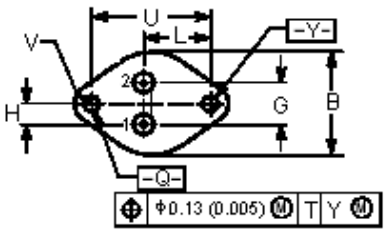
The 2N6609 powerbase™ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, DC-DC converters or inverters.

Features:

- Pb-free packages.
- High safe operating area (100% tested) 150W at 100V.
- Completely characterized for linear operation.
- High DC current gain and low saturation voltage
  h_{FE} = 15 (minimum) at 8.0A, 4.0V
  V_{CE} (sat) = 1.4V (maximum) at I_C = 8.0A, I_B = 0.8A.
- For low distortion complementary designs.

(TO-3)



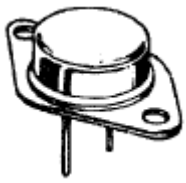


Style 1:
Pin 1. Base
2. Emitter
Collector (Case)

Dimensions	Minimum	Maximum
A	1.550 (39.37) Reference	
B	-	1.050 (26.67)
C	0.250 (6.35)	0.335 (8.51)
D	0.038 (0.97)	0.043 (1.09)
E	0.055 (1.40)	0.070 (1.77)
G	0.430 (10.92) BSC	
H	0.215 (5.46) BSC	
K	0.440 (11.18)	0.480 (12.19)
L	0.665 (16.89) BSC	
N	-	0.830 (21.08)
Q	0.151 (3.84)	0.165 (4.19)
U	1.187 (30.15) BSC	
V	0.131 (3.33)	0.188 (4.77)

Dimensions : Inches (Millimetres)

16A Complementary Power Transistors 140V, 150W



TO-3
Case 1-07

Maximum Ratings (Note 1)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	V dc
Collector-Emitter Voltage	V_{CEX}	160	
Collector-Base Voltage	V_{CBO}		
Emitter-Base Voltage	V_{EBO}	7	
Collector Current - Continuous - Peak (Note 2)	I_C	16 30	A dc
Base Current - Continuous - Peak (Note 2)	I_B	4 15	
Total Power Dissipation at T_A = 25°C Derate above 25°C	P_D	150 0.855	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. Indicates JEDEC Registered Data.
2. Pulse Test: Pulse Width = 5ms, Duty Cycle ≤10%.

Thermal Characteristics

Characteristics	Symbol	Maximum	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.17	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

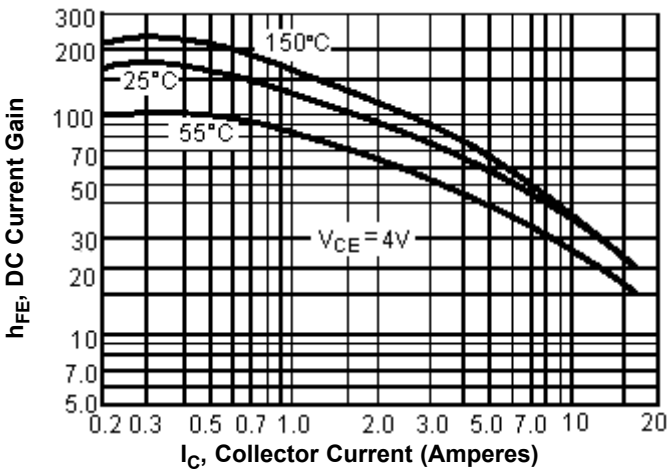
Characteristic	Symbol	Minimum	Maximum	Unit
Off Characteristics (Note 3)				
Collector-Emitter Breakdown Voltage (Note 4) (I_C = 0.2A dc, I_B = 0)	$V_{EO\ (sus)}$	140	-	V dc
Collector-Emitter Sustaining Voltage (Note 4) (I_C = 0.1A dc, $V_{BE\ (off)}$ = 1.5V dc, R_{BE} = 100Ω)	$V_{CEX\ (sus)}$	160	-	
Collector-Emitter Sustaining Voltage (I_C = 0.2A dc, R_{BE} = 100Ω)	$V_{CER\ (sus)}$	150	-	
Collector Cut off Current (Note 4) (V_{CE} = 120V dc, I_B = 0)	I_{CEO}	-	10	mA dc
Collector Cut off Current (Note 4) (V_{CE} = 140V dc $V_{BE\ (off)}$ = 1.5V dc) (V_{CE} = 140V dc $V_{BE\ (off)}$ = 1.5V dc, T_C = 150°C)	I_{CEX}	-	2 10	
Collector Cut off Current (V_{CB} = 140V dc, I_E = 0)	I_{CBO}	-	2	
Emitter Cut off Current (Note 4) (V_{BE} = 7V dc, I_C = 0)	I_{EBO}	-	5	

Electrical Characteristics (T_C = 25°C unless otherwise noted)

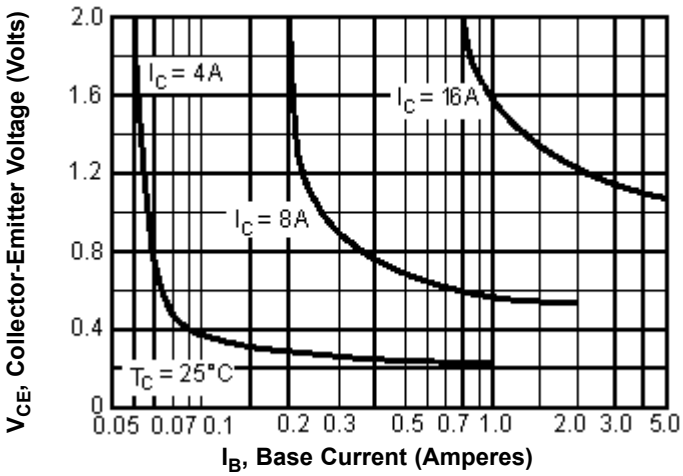
On Characteristic (Note 3)				
DC Current Gain (I_C = 8A dc, V_{CE} = 4V dc) (Note 4) (I_C = 16A dc, V_{CE} = 4V dc)	h_{FE}	15 5	60 -	-
Collector-Emitter Saturation Voltage (I_C = 8A dc, I_B = 800mA dc) (Note 4) (I_C = 16A dc, I_B = 3.2A dc)	$V_{CE\ (sat)}$	-	1.4 4	V dc
Base-Emitter On Voltage (Note 4) (I_C = 8A dc, V_{CE} = 4V dc)	$V_{BE\ (on)}$	-	2.2	
Dynamic Characteristics				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1A, f = 50kHz)	$\lvert h_{fe} \rvert$	4	-	-
Small-Signal Current Gain (Note 4) (I_C = 1A dc, V_{CE} = 4V dc, f = 1kHz)	h_{fe}	40	-	-
Second Breakdown Characteristics				
Second Breakdown Collector Current with Base Forward Biased t = 1s (non-repetitive), V_{CE} = 100V	$I_{S/b}$	1.5	-	A dc

3. Pulse Test : Pulse Width = 300μs, Duty Cycle ≤2.0%.
4. Indicates JEDEC Registered Data.

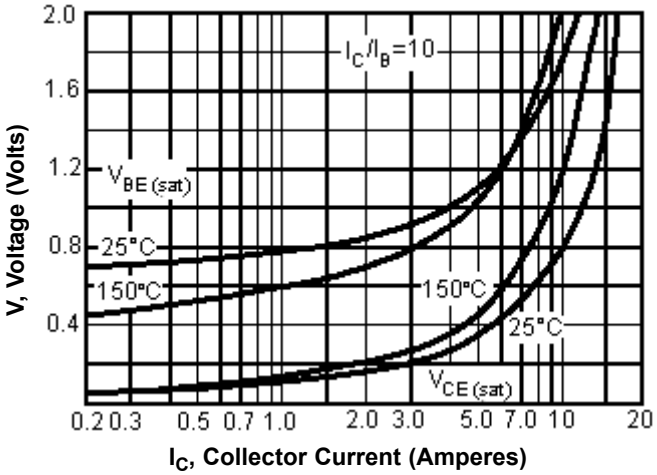
DC Current Gain



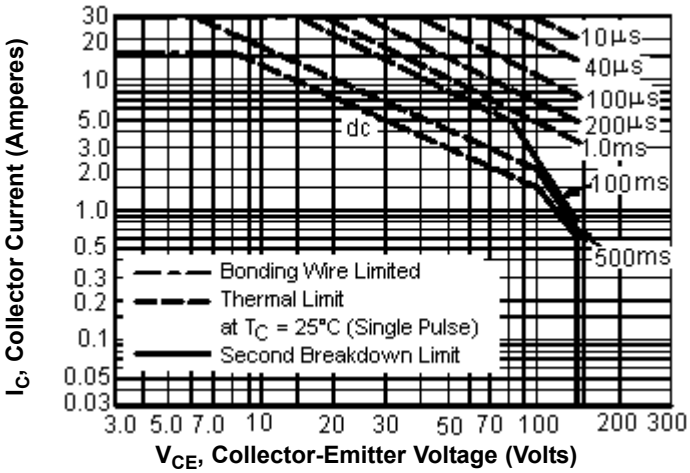
Collector Saturation Region



"On" Voltage

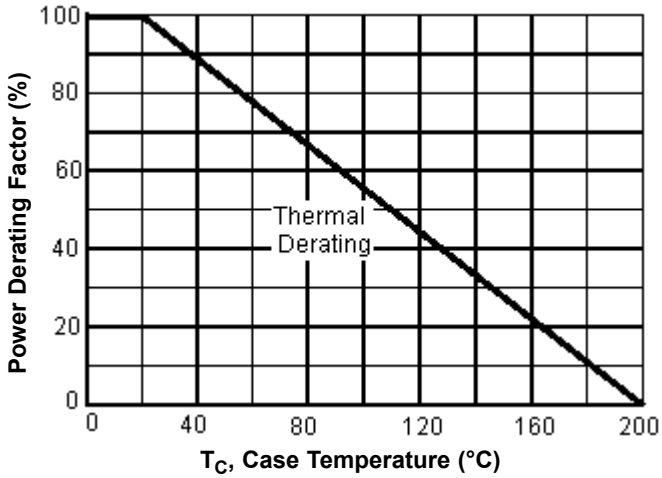


Forward Bias Safe Operating Area



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data is based on $T_{J\,(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J\,(pk)}$ <200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Power Derating



Part Number Table

Description	Part Number
Transistor, PNP, TO-3	MJ2955