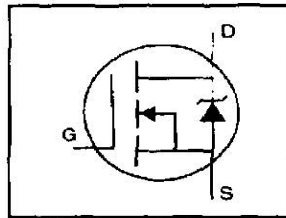


# IRF740LCPbF

## HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V<sub>GS</sub> Rating
- Reduced C<sub>iss</sub>, C<sub>oss</sub>, C<sub>rss</sub>
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead-Free



$$V_{DSS} = 400V$$

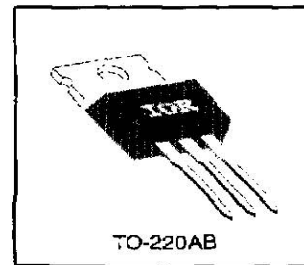
$$R_{DS(on)} = 0.55\Omega$$

$$I_D = 10A$$

### Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



### Absolute Maximum Ratings

| Parameter                         | Max.   | Units                 |
|-----------------------------------|--|-----------------------|
| $I_D$ @ $T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS} @ 10\text{ V}$ | 10                    |
| $I_D$ @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{ V}$ | 6.3                   |
| $I_{DM}$                          | Pulsed Drain Current ①                           | 32                    |
| $P_D$ @ $T_C = 25^\circ\text{C}$  | Power Dissipation                                | 125                   |
|                                   | Linear Derating Factor                           | 1.0                   |
| $V_{GS}$                          | Gate-to-Source Voltage                           | $\pm 30$              |
| $E_{AS}$                          | Single Pulse Avalanche Energy ②                  | 520                   |
| $I_{AR}$                          | Avalanche Current ③                              | 10                    |
| $E_{AR}$                          | Repetitive Avalanche Energy ④                    | 13                    |
| $dv/dt$                           | Peak Diode Recovery $dv/dt$ ⑤                    | 4.0                   |
| $T_J$                             | Operating Junction and                           | -55 to +150           |
| $T_{STG}$                         | Storage Temperature Range                        |                       |
|                                   | Soldering Temperature, for 10 seconds            | 300 (1.6mm from case) |
|                                   | Mounting Torque, 6-32 or M3 screw                | 10 lbf·in (1.1 N·m)   |

### Thermal Resistance

| Parameter       | Parameter                           | Min. | Typ. | Max. | Units              |
|-----------------|-------------------------------------|------|------|------|--------------------|
| $R_{\theta JC}$ | Junction-to-Case                    | —    | —    | 1.0  |                    |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | —    | 0.50 | —    | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Junction-to-Ambient                 | —    | —    | 62   |                    |

### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

| Parameter                              | Min. | Typ. | Max. | Units | Test Conditions   |
|--|------|------|------|-------|---|
| V <sub>(BR)DSS</sub>                   | 400  | —    | —    | V     | V <sub>GS</sub> =0V, I <sub>D</sub> =250μA                          |
| ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub> | —    | 0.76 | —    | V/°C  | Reference to 25°C, I <sub>D</sub> =1mA                              |
| R <sub>D(on)</sub>                     | —    | —    | 0.55 | Ω     | V <sub>GS</sub> =10V, I <sub>D</sub> =6.0A ①                        |
| V <sub>GS(th)</sub>                    | 2.0  | —    | 4.0  | V     | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA            |
| g <sub>fs</sub>                        | 3.0  | —    | —    | S     | V <sub>DS</sub> =50V, I <sub>D</sub> =6.0A ①                        |
| I <sub>DSS</sub>                       | —    | —    | 25   | μA    | V <sub>DS</sub> =400V, V <sub>GS</sub> =0V                          |
| I <sub>DSS</sub>                       | —    | —    | 250  | μA    | V <sub>DS</sub> =320V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C   |
| I <sub>GSS</sub>                       | —    | —    | 100  | nA    | V <sub>GS</sub> =20V  |
| I <sub>GSS</sub>                       | —    | —    | -100 | nA    | V <sub>GS</sub> =-20V   |
| Q <sub>G</sub>                         | —    | —    | 39   | nC    | I <sub>D</sub> =10A   |
| Q <sub>GS</sub>                        | —    | —    | 10   | nC    | V <sub>DS</sub> =320V   |
| Q <sub>GD</sub>                        | —    | —    | 19   | nC    | V <sub>GS</sub> =10V See Fig. 6 and 13 ①                            |
| t <sub>d(on)</sub>                     | —    | 11   | —    | ns    | V <sub>DD</sub> =200V   |
| t <sub>r</sub>                         | —    | 31   | —    | ns    | I <sub>D</sub> =10A   |
| t <sub>d(off)</sub>                    | —    | 25   | —    | ns    | R <sub>G</sub> =9.1Ω  |
| t <sub>f</sub>                         | —    | 20   | —    | ns    | R <sub>D</sub> =20Ω See Figure 10 ①                                 |
| L <sub>D</sub>                         | —    | 4.5  | —    | nH    | Between lead, 6 mm (0.25in.) from package and center of die contact |
| L <sub>S</sub>                         | —    | 7.5  | —    | nH    |   |
| C <sub>iss</sub>                       | —    | 1100 | —    | pF    | V <sub>DS</sub> =0V   |
| C <sub>oss</sub>                       | —    | 190  | —    | pF    | V <sub>DS</sub> =25V  |
| C <sub>rss</sub>                       | —    | 18   | —    | pF    | f=1.0MHz See Figure 5   |

### Source-Drain Ratings and Characteristics

| Parameter       | Min.   | Typ. | Max. | Units | Test Conditions  |
|-----------------|--|------|------|-------|--|
| I <sub>S</sub>  | —  | —    | 10   | A     | MOSFET symbol showing the integral reverse p-n junction diode.   |
| I <sub>SM</sub> | —  | —    | 32   | A     |  |
| V <sub>SD</sub> | —  | —    | 2.0  | V     | T <sub>J</sub> =25°C, I <sub>S</sub> =10A, V <sub>GS</sub> =0V ① |
| t <sub>rr</sub> | —  | 380  | 570  | ns    | T <sub>J</sub> =25°C, I <sub>F</sub> =10A                        |
| Q <sub>rr</sub> | —  | 2.8  | 4.2  | μC    | di/dt=100A/μs ①  |
| t <sub>or</sub> | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> ) |      |      |       |  |

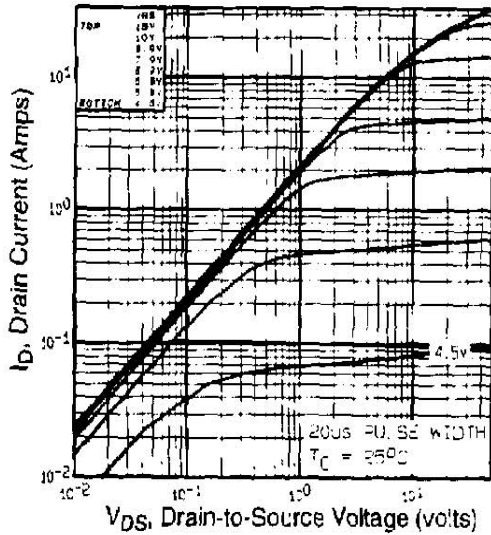
#### Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

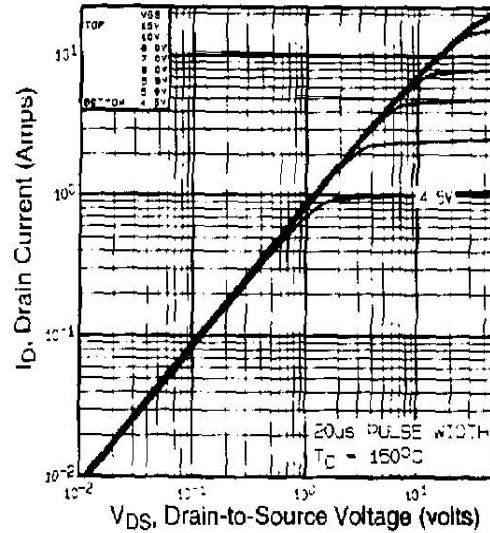
② I<sub>SD</sub>≤10A, di/dts120A/μs, V<sub>DS</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C

③ V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=9.1mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=10A (See Figure 12)

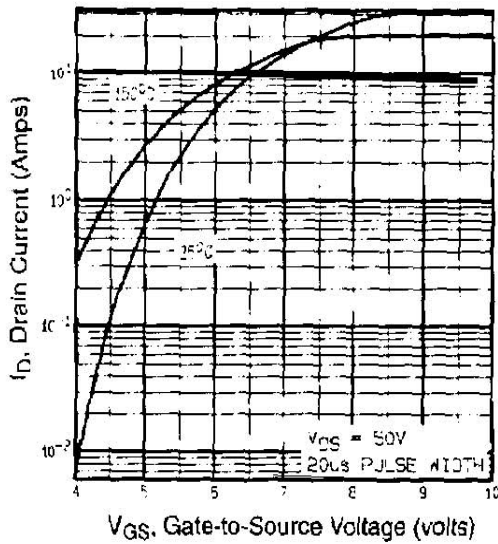
④ Pulse width ≤ 300 μs; duty cycle ≤2%.



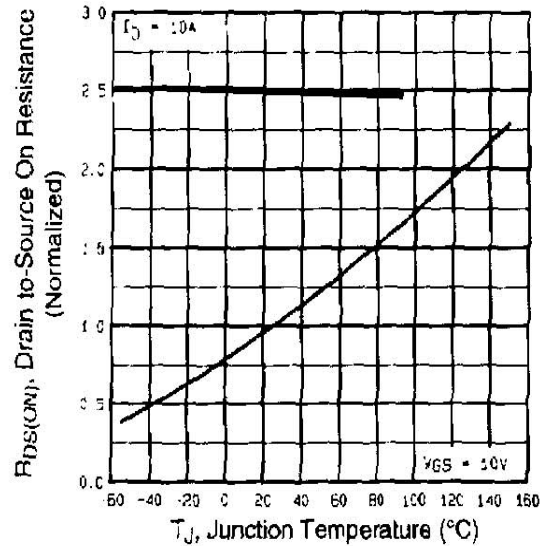
**Fig 1.** Typical Output Characteristics,  
 $T_c=25^\circ\text{C}$



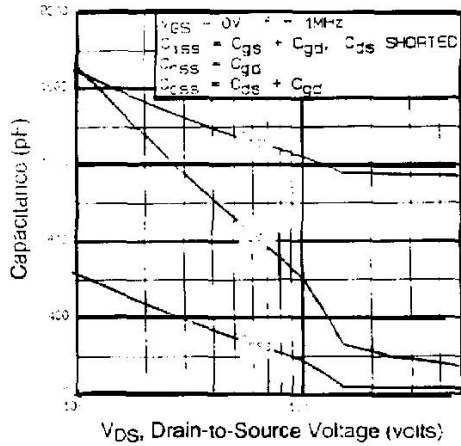
**Fig 2.** Typical Output Characteristics,  
 $T_c=150^\circ\text{C}$



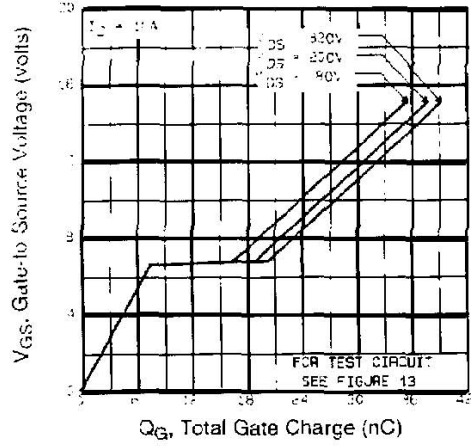
**Fig 3.** Typical Transfer Characteristics



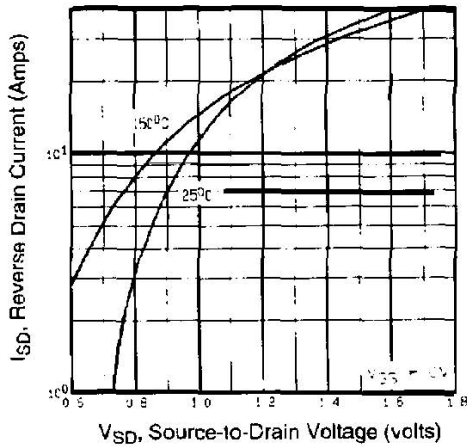
**Fig 4.** Normalized On-Resistance  
 Vs. Temperature



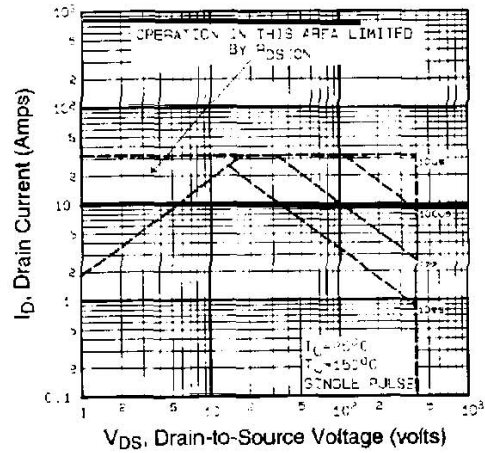
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



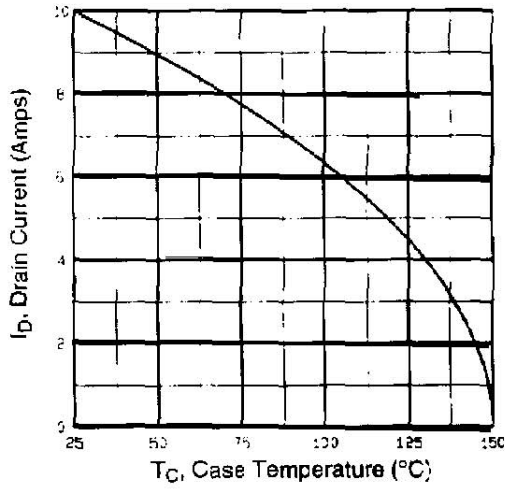
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



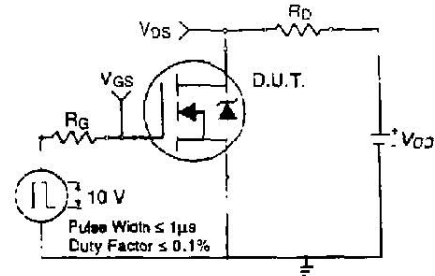
**Fig 7.** Typical Source-Drain Diode Forward Voltage



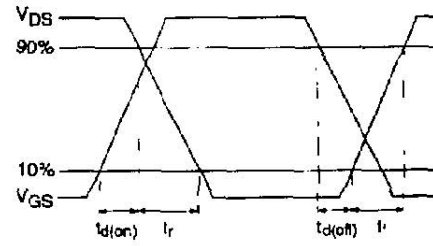
**Fig 8.** Maximum Safe Operating Area



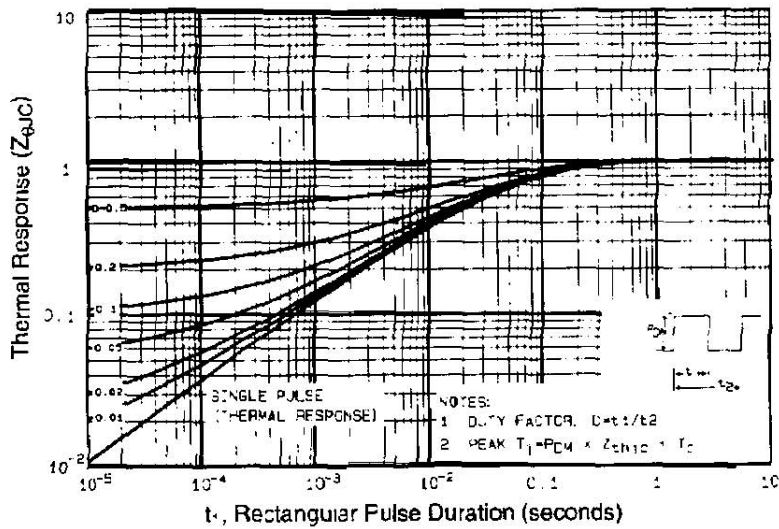
**Fig 9.** Maximum Drain Current Vs. Case Temperature



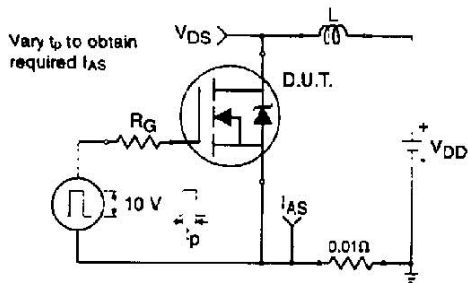
**Fig 10a.** Switching Time Test Circuit



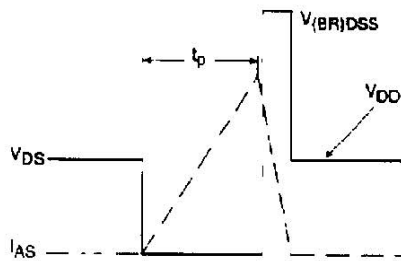
**Fig 10b.** Switching Time Waveforms



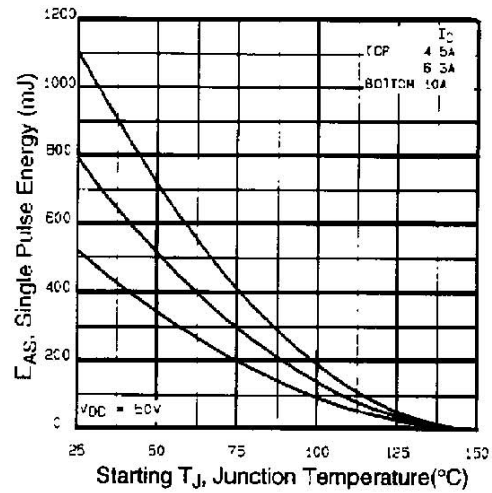
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



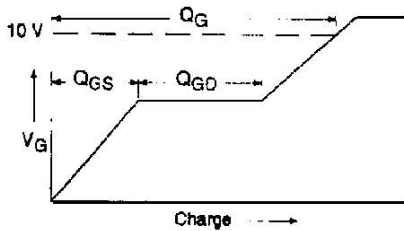
**Fig 12a.** Unclamped Inductive Test Circuit



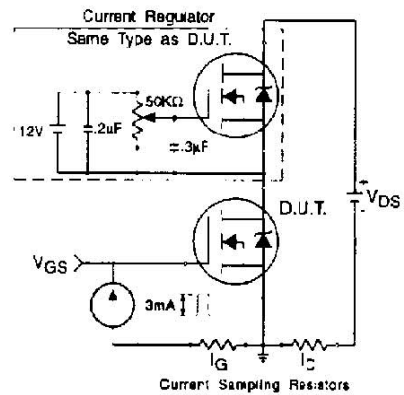
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

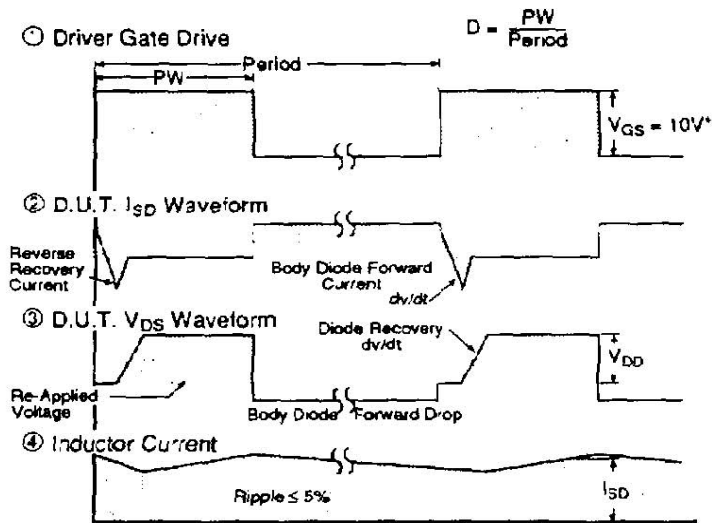
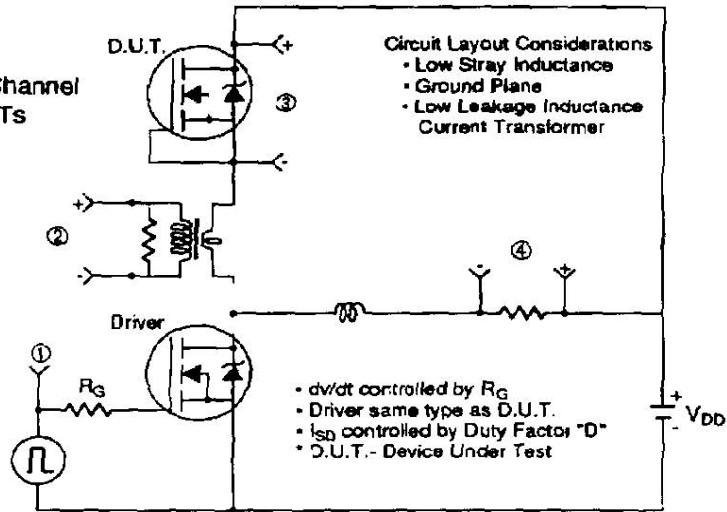
**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit

**Appendix B:** Package Outline Mechanical Drawing

Appendix A

Peak Diode Recovery  $dv/dt$  Test Circuit

Fig 14. For N-Channel HEXFETs



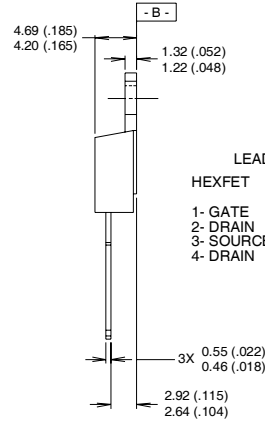
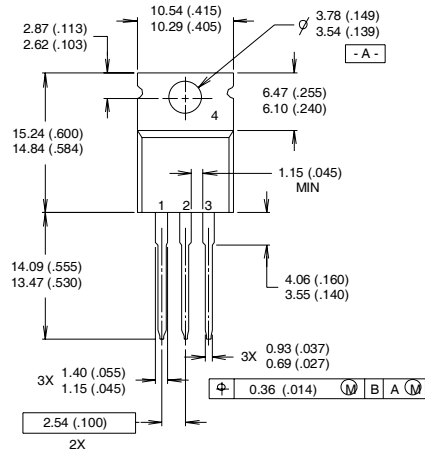
\*  $V_{GS} = 5V$  for Logic Level Devices

# IRF740LCPbF



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

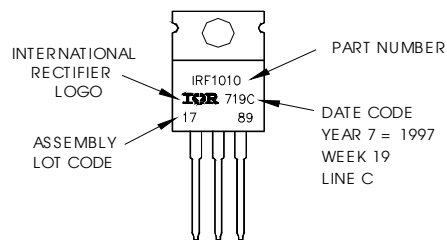
| HEXFET    | IGBTs, CoPACK |
|-----------|---------------|
| 1- GATE   | 1- GATE       |
| 2- DRAIN  | 2- COLLECTOR  |
| 3- SOURCE | 3- EMITTER    |
| 4- DRAIN  | 4- COLLECTOR  |

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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