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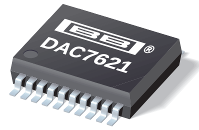

DAC7621

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12-Bit, Parallel Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 2.5mW
- FAST SETTLING: 7µs to 1 LSB
- 1mV LSB WITH 4.095V FULL-SCALE RANGE
- COMPLETE WITH REFERENCE
- 12-BIT LINEARITY AND MONOTONICITY OVER INDUSTRIAL TEMP RANGE
- ASYNCHRONOUS RESET TO 0V

APPLICATIONS

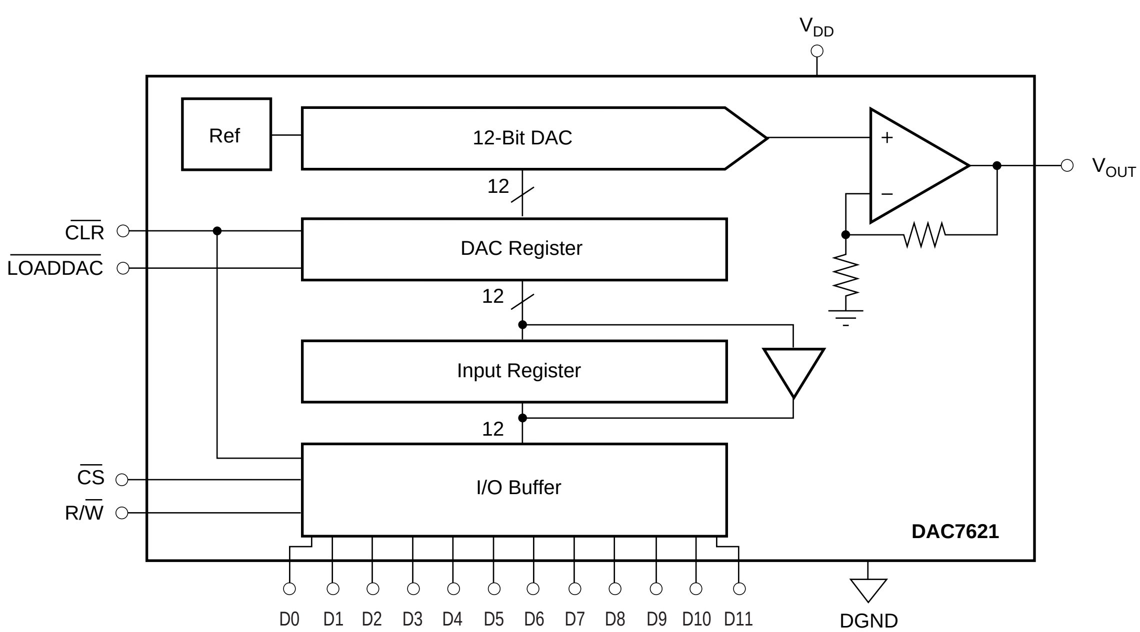
- PROCESS CONTROL
- DATA ACQUISITION SYSTEMS
- CLOSED-LOOP SERVO-CONTROL
- PC PERIPHERALS
- PORTABLE INSTRUMENTATION

DESCRIPTION

The DAC7621 is a 12-bit digital-to-analog converter (DAC) with guaranteed 12-bit monotonicity performance over the industrial temperature range. It requires a single +5V supply and contains an input register, latch, 2.435V reference, DAC, and high speed rail-to-rail output amplifier. For a full-scale step, the output will settle to 1 LSB within 7µs. The device consumes 2.5mW (0.5mA at 5V).

The parallel interface is compatible with a wide variety of microcontrollers. The DAC7621 accepts a 12-bit parallel word, has a double-buffered input logic structure and provides data readback. In addition, two control pins provide a chip select ($\overline{CS}$) function and asynchronous clear ($\overline{CLR}$) input. The $\overline{CLR}$ input can be used to ensure that the DAC7621 output is 0V on power-up or as required by the application.

The DAC7621 is available in a 20-lead SSOP package and is fully specified over the industrial temperature range of –40°C to +85°C.



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SBAS107

SPECIFICATIONS

ELECTRICAL

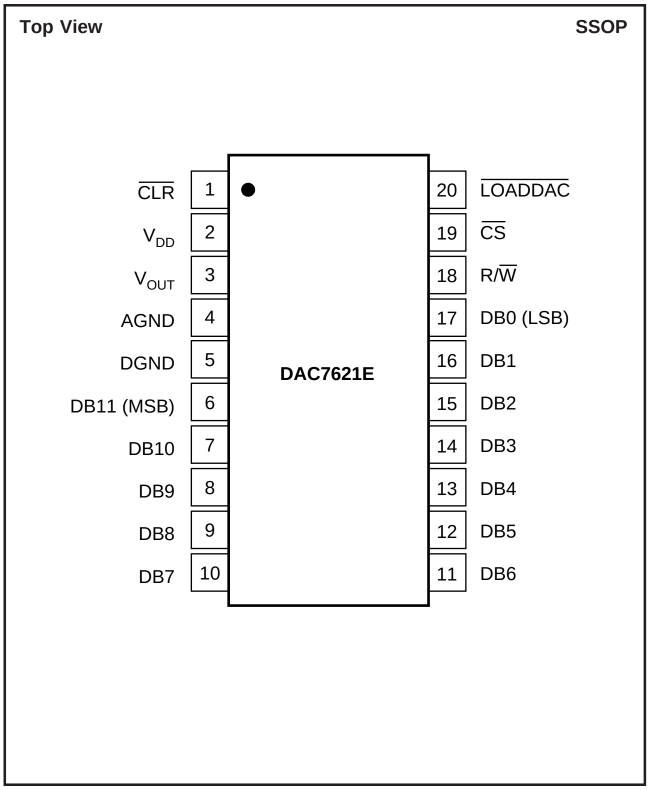
At T_A = –40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7621E MIN	DAC7621E TYP	DAC7621E MAX	DAC7621EB MIN	DAC7621EB TYP	DAC7621EB MAX	UNITS
RESOLUTION		12			*			Bits
ACCURACY								
Relative Accuracy[1]		–2	±1/2	+2	–1	±1/4	+1	LSB
Differential Nonlinearity	Guaranteed Monotonic	–1	±1/2	+1	–1	±1/4	+1	LSB
Zero-Scale Error	Code 000_H	–1	+1	+3	*	*	*	LSB
Full Scale Voltage	Code FFF_H	4.079	4.095	4.111	4.087	4.095	4.103	V
ANALOG OUTPUT								
Output Current	Code 800_H	±5	±7		*	*		mA
Load Regulation	$R_{LOAD} \geq 402\Omega$, Code 800_H		1	3		*	*	LSB
Capacitive Load	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	GND or V_{DD}		Indefinite			*		
DIGITAL INPUT								
Data Format			Parallel			*		
Data Coding			Straight Binary			*		
Logic Family			CMOS			*		
Logic Levels								
V_{IH}		0.7 • V_{DD}			*			V
V_{IL}				0.3 • V_{DD}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DYNAMIC PERFORMANCE								
Settling Time[2] (t_S)	To ±1 LSB of Final Value		7			*		µs
DAC Glitch			5			*		nV-s
Digital Feedthrough			2			*		nV-s
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
I_{DD}	V_{IH} = 5V, V_{IL} = 0V, No Load, at Code 000_H		0.5	1		*	*	mA
Power Dissipation	V_{IH} = 5V, V_{IL} = 0V, No Load		2.5	5		*	*	mW
Power Supply Sensitivity	ΔV_{DD} = ±5%		0.001	0.004		*	*	%/%
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specification as for DAC7621E.

NOTES: (1) This term is sometimes referred to as Linearity Error or Integral Nonlinearity (INL). (2) Specification does not apply to negative-going transitions where the final output voltage will be within 3 LSBs of ground. In this region, settling time may be double the value indicated.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	$\overline{CLR}$	Reset. Resets the DAC register to zero. Active LOW. Asynchronous input.
2	V_{DD}	Postive Power Supply
3	V_{OUT}	DAC Output Voltage
4	AGND	Analog Ground
5	DGND	Digital Ground
6	DB11	Data Bit 11, MSB
7	DB10	Data Bit 10
8	DB9	Data Bit 9
9	DB8	Data Bit 8
10	DB7	Data Bit 7
11	DB6	Data Bit 6
12	DB5	Data Bit 5
13	DB4	Data Bit 4
14	DB3	Data Bit 3
15	DB2	Data Bit 2
16	DB1	Data Bit 1
17	DB0	Data Bit 0, LSB
18	R/$\overline{W}$	Read and Write Control
19	$\overline{CS}$	Chip Select. Active LOW.
20	$\overline{LOADDAC}$	Loads the internal DAC register. The DAC register is a transparent latch and is transparent when $\overline{LOADDAC}$ is LOW (regardless of the state of $\overline{CS}$ or CLK).

ABSOLUTE MAXIMUM RATINGS[(1)]

V_{DD} to GND	–0.3V to 6V
Digital Inputs to GND	–0.3V to V_{DD} + 0.3V
V_{OUT} to GND	–0.3V to V_{DD} + 0.3V
Power Dissipation	325mW
Thermal Resistance, θ_{JA}	150°C/W
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

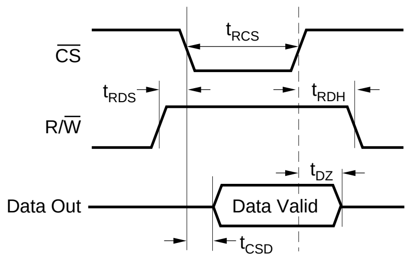
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

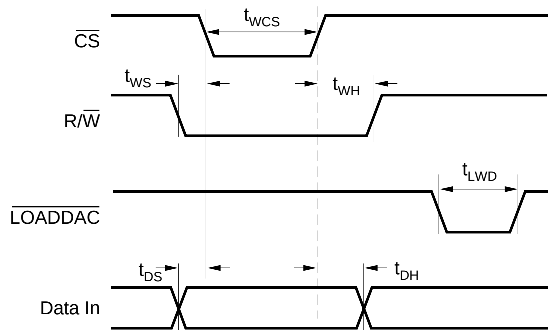
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[(1)]	ORDERING NUMBER[(2)]	TRANSPORT MEDIA
DAC7621E	±2	±1	–40°C to +85°C	20-Lead SSOP	334	DAC7621E	Rails
"	"	"	"	"	"	DAC7621E/1K	Tape and Reel
DAC7621EB	±1	±1	–40°C to +85°C	20-Lead SSOP	334	DAC7621EB	Rails
"	"	"	"	"	"	DAC7621EB/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7621E/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

TIMING DIAGRAMS



Data Output Timing



Digital Input Timing

TIMING SPECIFICATIONS

T_A = –40°C to +85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	200			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	0			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance		100		ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	160	ns
t_{WCS}	$\overline{CS}$ LOW for Write	50			
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	5			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	5			ns
t_{LWD}	$\overline{LOADDAC}$ LOW	50			ns

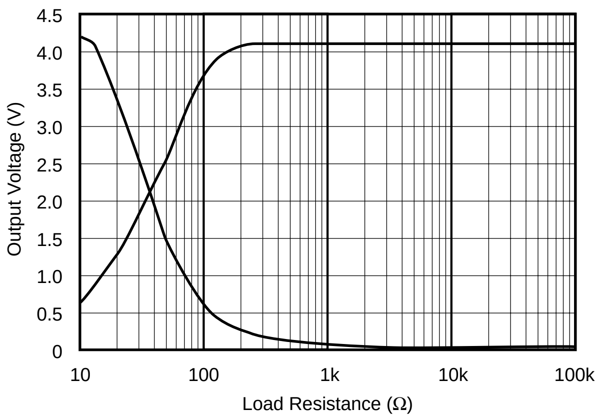
LOGIC TRUTH TABLE

R/$\overline{W}$	$\overline{CS}$	$\overline{LOADDAC}$	INPUT REGISTER	DAC REGISTER	MODE
L	L	L	Write	Write	Write
L	L	H	Write	Hold	Write Input
H	L	H	Read	Hold	Read Input
X	H	L	Hold	Update	Update
X	H	H	Hold	Hold	Hold

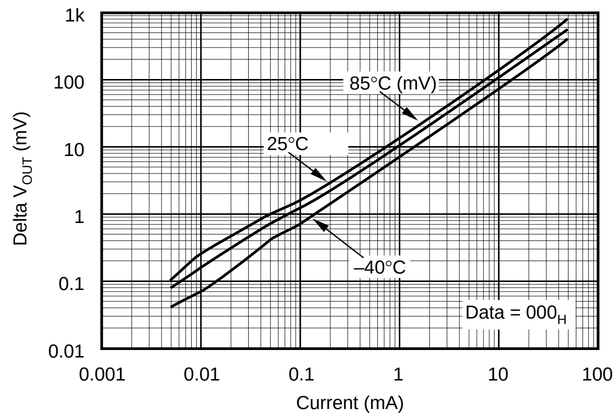
X = Don't Care.

TYPICAL PERFORMANCE CURVES

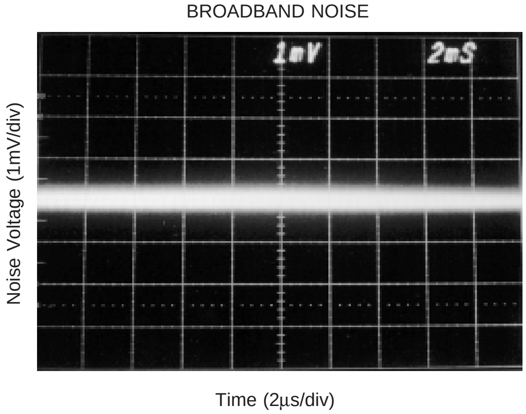
At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.



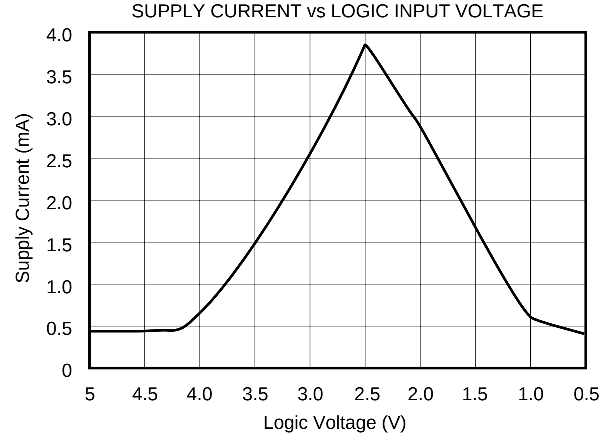
OUTPUT SWING vs LOAD



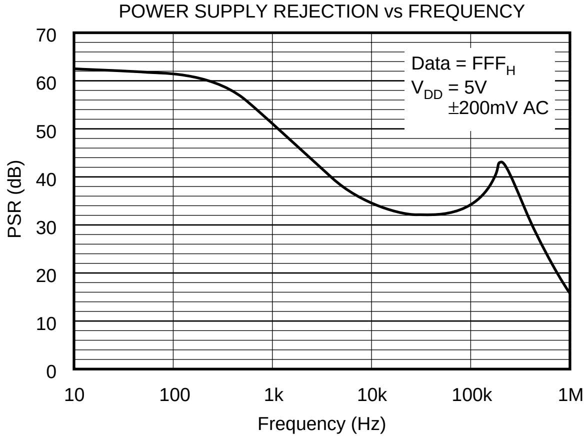
PULL-DOWN VOLTAGE vs OUTPUT SINK CURRENT



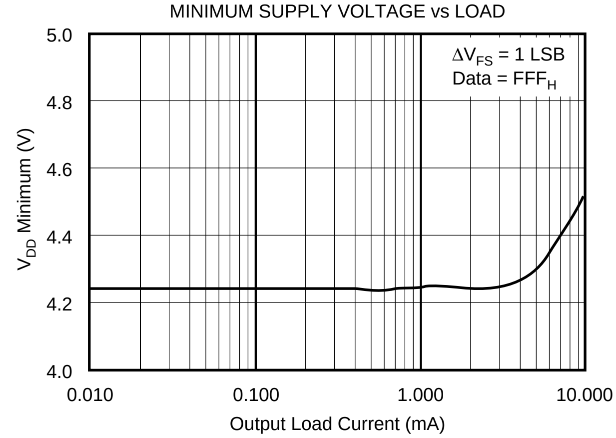
BROADBAND NOISE



SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY

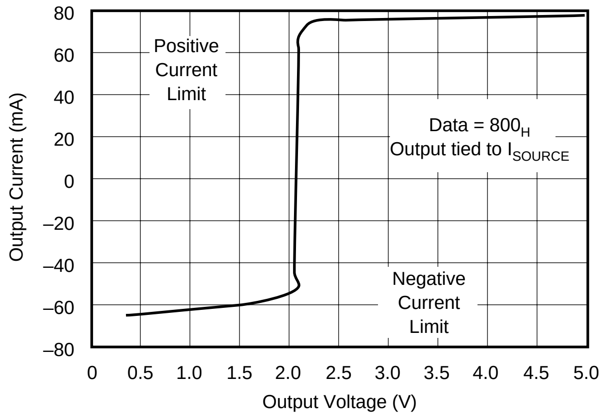


MINIMUM SUPPLY VOLTAGE vs LOAD

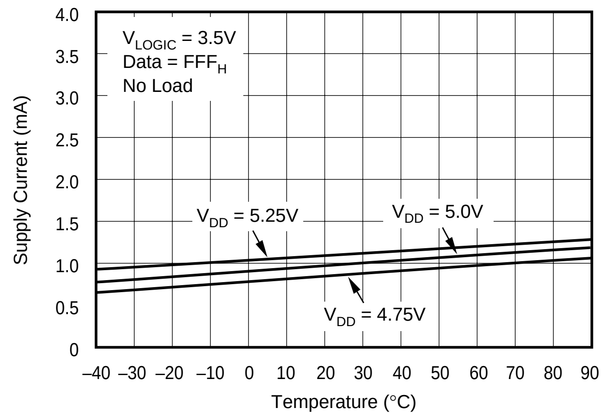
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

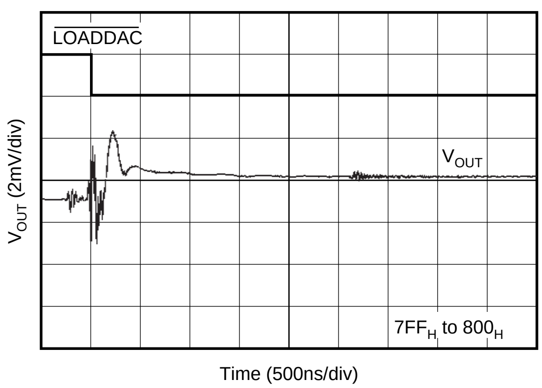
SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



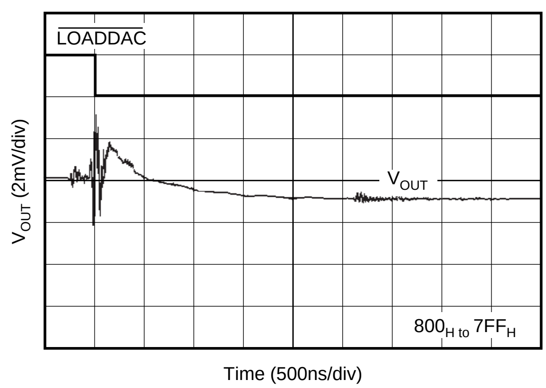
SUPPLY CURRENT vs TEMPERATURE



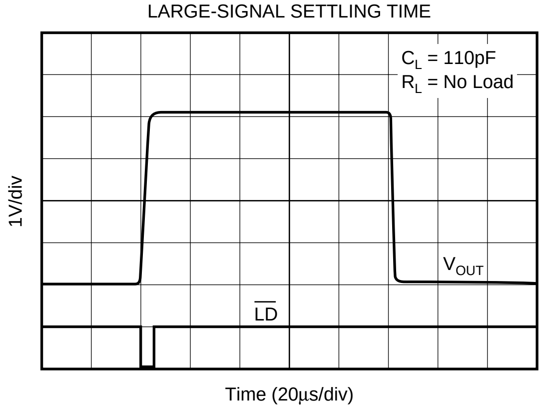
MID-SCALE GLITCH PERFORMANCE



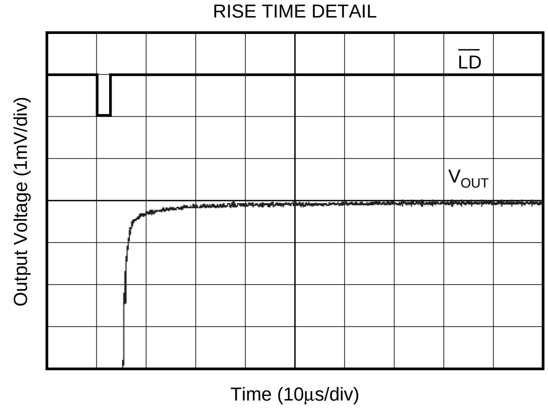
MID-SCALE GLITCH PERFORMANCE



LARGE-SIGNAL SETTLING TIME

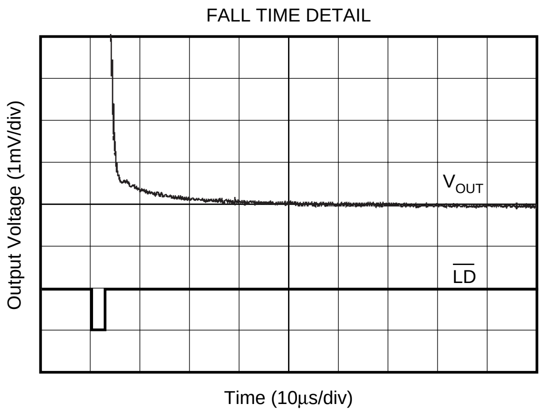


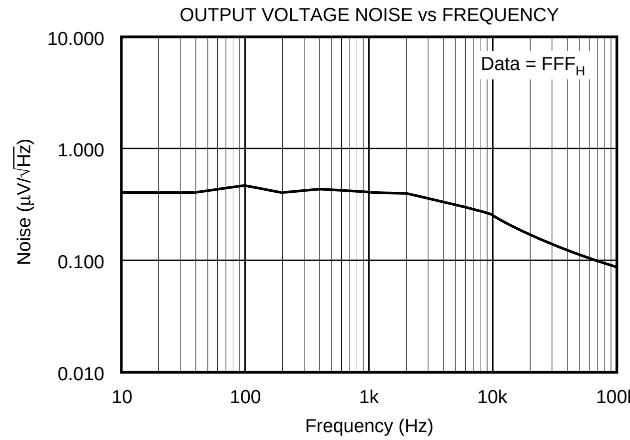
RISE TIME DETAIL

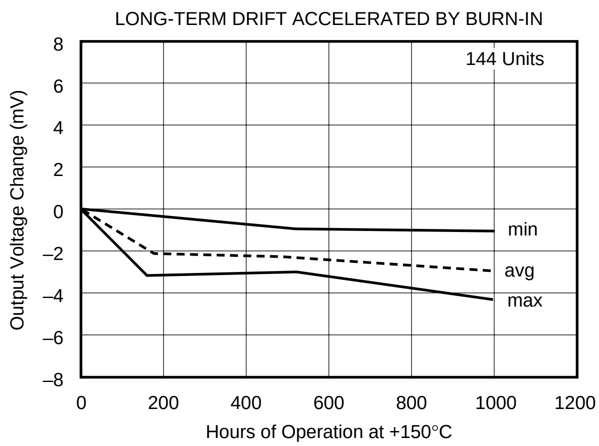


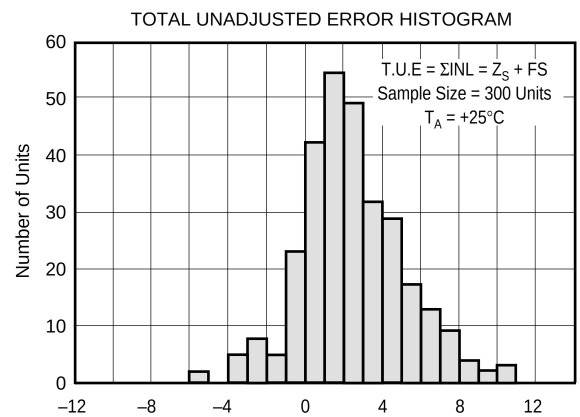
TYPICAL PERFORMANCE CURVES (CONT)

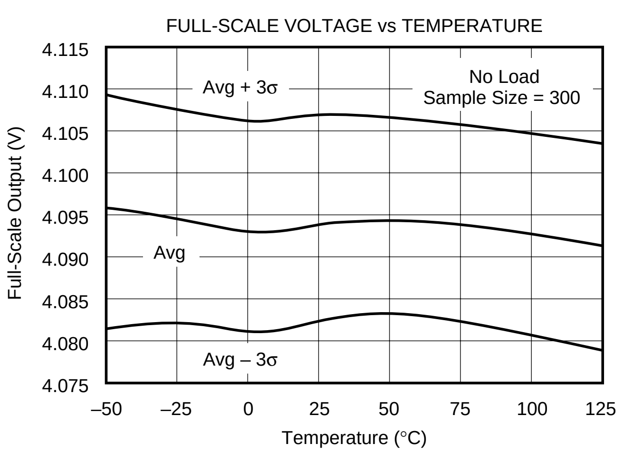
At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

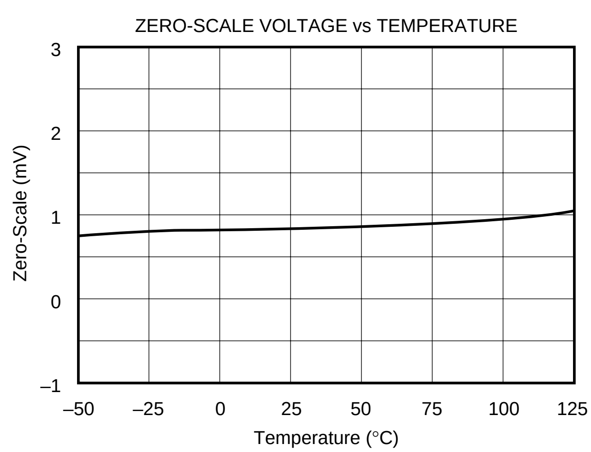








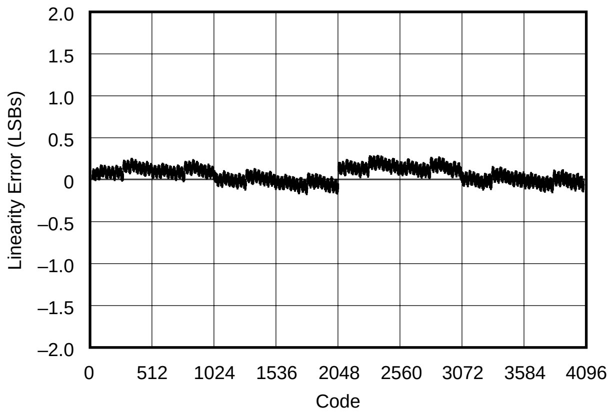




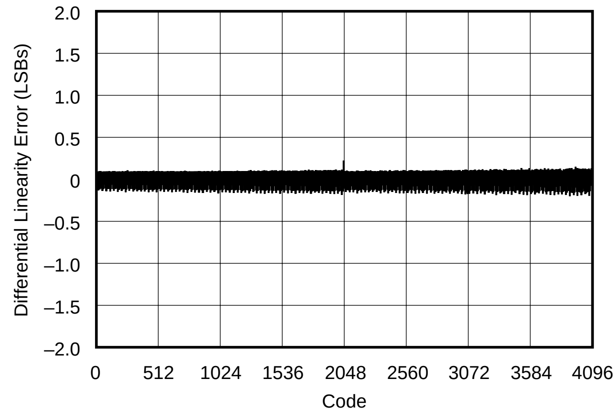
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

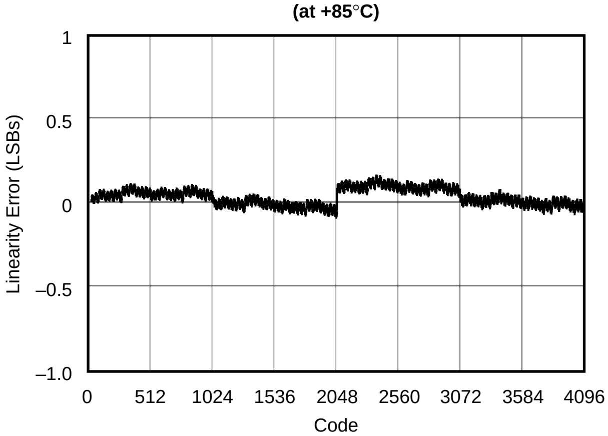
LINEARITY ERROR vs DIGITAL CODE
(at +25°C)



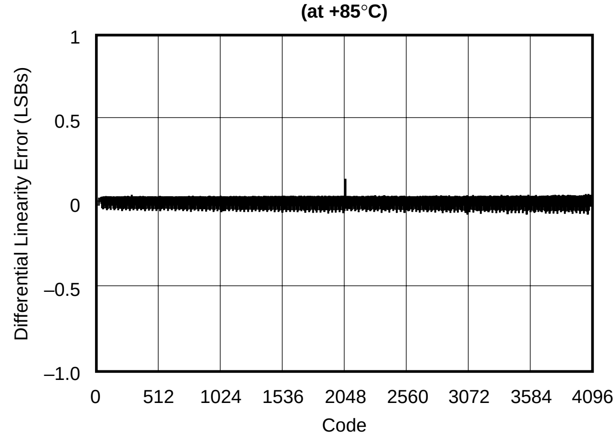
DIFFERENTIAL LINEARITY ERROR vs DIGITAL CODE
(at +25°C)



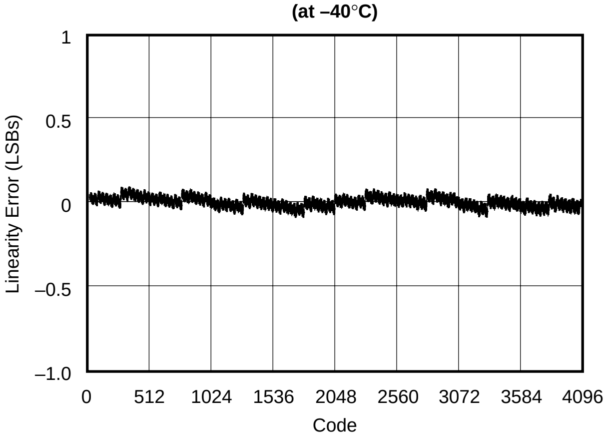
LINEARITY ERROR vs DIGITAL CODE
(at +85°C)



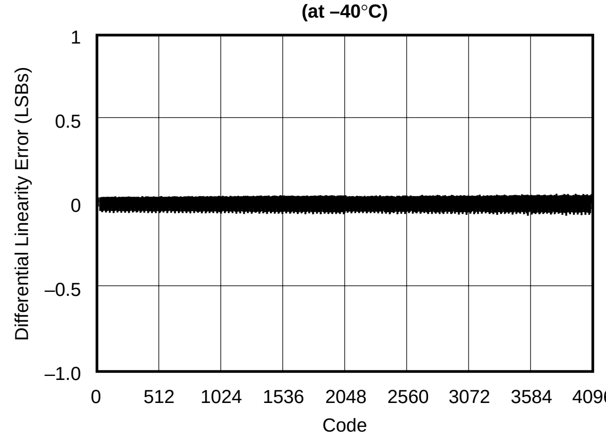
DIFFERENTIAL LINEARITY ERROR vs DIGITAL CODE
(at +85°C)



LINEARITY ERROR vs DIGITAL CODE
(at –40°C)



DIFFERENTIAL LINEARITY ERROR vs DIGITAL CODE
(at –40°C)



OPERATION

The DAC7621 is a 12-bit digital-to-analog converter (DAC) complete with an input shift register, DAC register, laser-trimmed 12-bit DAC, on-board reference, and a rail-to-rail output amplifier. Figure 1 shows the basic operation of the DAC7621.

INTERFACE

Figure 1 shows the basic connection between a microcontroller and the DAC7621. The interface consists of a Read/Write (R/$\overline{\text{W}}$), data, and a load DAC signal ($\overline{\text{LOADDAC}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable the DAC7621 when there are multiple devices. The data format is Straight Binary. An asynchronous clear input ($\overline{\text{CLR}}$) is provided to simplify start-up or periodic resets. Table I shows the relationship between input code and output voltage.

DAC7621 Full-Scale Range = 4.095V Least Significant Bit = 1mV		
DIGITAL INPUT CODE STRAIGHT OFFSET BINARY	**ANALOG OUTPUT (V)**	**DESCRIPTION**
FFF_H	+4.095	Full Scale
801_H	+2.049	Midscale + 1 LSB
800_H	+2.048	Midscale
$7FF_H$	+2.047	Midscale – 1 LSB
000_H	0	Zero Scale

TABLE I. Digital Input Code and Corresponding Ideal Analog Output.

The digital data into the DAC7621 is double-buffered. This means that new data can be entered into the DAC without disturbing the old data and the analog output of the converter. At some point after the data has been entered into the serial shift register, this data can be transferred into the DAC register. This transfer is accomplished with a HIGH to LOW transition of the $\overline{\text{LOADDAC}}$ pin. However, the $\overline{\text{LOADDAC}}$ pin makes the DAC register transparent. If new data becomes available on the bus register while $\overline{\text{LOADDAC}}$ is LOW, the DAC output voltage will change as the data changes. To prevent this, $\overline{\text{CS}}$ must be returned HIGH prior to changing data on the bus.

At any time, the contents of the DAC register can be set to 000_H (analog output equals 0V) by taking the $\overline{\text{CLR}}$ input LOW. The DAC register will remain at this value until $\overline{\text{CLR}}$ is returned HIGH and $\overline{\text{LOADDAC}}$ is taken LOW to allow the contents of the input register to be transferred to the DAC register. If $\overline{\text{LOADDAC}}$ is LOW when $\overline{\text{CLR}}$ is taken LOW, the DAC register will be set to 000_H and the analog output driven to 0V. When $\overline{\text{CLR}}$ is returned HIGH, the DAC register and the analog output will respond accordingly.

DIGITAL-TO-ANALOG CONVERTER

The internal DAC section is a 12-bit voltage output device that swings between ground and the internal reference voltage. The DAC is realized by a laser-trimmed R-2R ladder network which is switched by N-channel MOSFETs. The DAC output is internally connected to the rail-to-rail output operational amplifier.

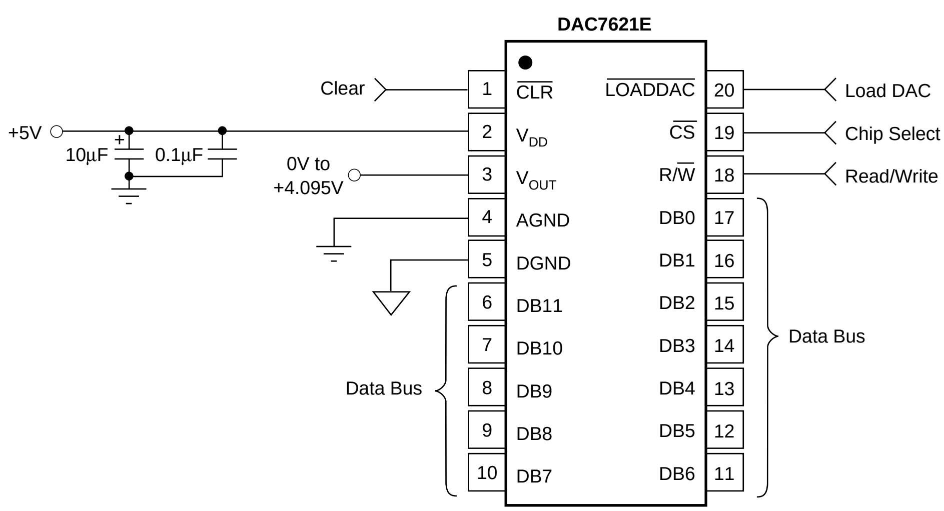


FIGURE 1. Basic Operation of the DAC7621.

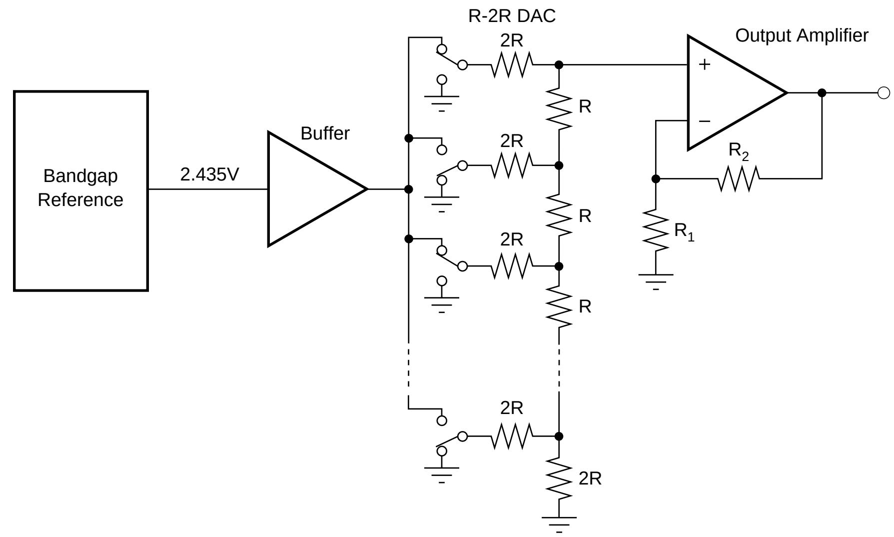


FIGURE 2. Simplified Schematic of Analog Portion.

OUTPUT AMPLIFIER

A precision, low-power amplifier buffers the output of the DAC section and provides additional gain to achieve a 0V to 4.095V range. The amplifier has low offset voltage, low noise, and a set gain of 1.682V/V (4.095/2.435). See Figure 2 for an equivalent circuit schematic of the analog portion of the DAC7621.

The output amplifier has a 7µs typical settling time to ±1 LSB of the final value. Note that there are differences in the settling time for negative-going signals versus positive-going signals.

The rail-to-rail output stage of the amplifier provides the full-scale range of 0V to 4.095V while operating on a supply voltage as low as 4.75V. In addition to its ability to drive resistive loads, the amplifier will remain stable while driving capacitive loads of up to 500pF. See Figure 3 for an equivalent circuit schematic of the amplifier's output driver and the Typical Performance Curves section for more information regarding settling time, load driving capability, and output noise.

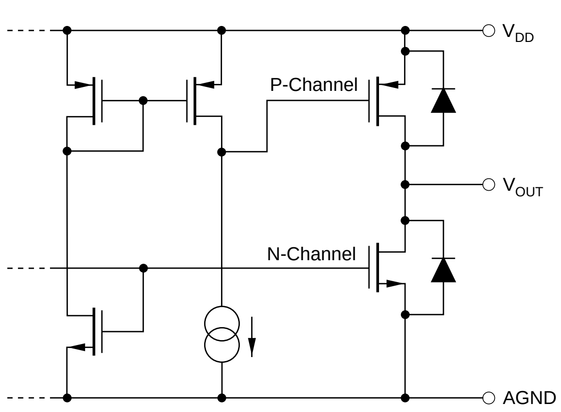


FIGURE 3. Simplified Driver Section of Output Amplifier.

POWER SUPPLY

A BiCMOS process and careful design of the bipolar and CMOS sections of the DAC7621 result in a very low power device. Bipolar transistors are used where tight matching and low noise are needed to achieve analog accuracy, and CMOS transistors are used for logic, switching functions and for other low power stages.

If power consumption is critical, it is important to keep the logic levels on the digital inputs ($R/\overline{W}$, CLK, $\overline{CS}$, $\overline{LOADDAC}$, $\overline{CLR}$) as close as possible to either V_{DD} or ground. This will keep the CMOS inputs (see "Supply Current vs Logic Input Voltages" in the Typical Performance Curves) from shunting current between V_{DD} and ground.

The DAC7621 power supply should be bypassed as shown in Figure 1. The bypass capacitors should be placed as close to the device as possible, with the 0.1µF capacitor taking priority in this regard. The "Power Supply Rejection vs Frequency" graph in the Typical Performance Curves section shows the PSRR performance of the DAC7621. This should be taken into account when using switching power supplies or DC/DC converters.

In addition to offering guaranteed performance with V_{DD} in the 4.75V to 5.25V range, the DAC7621 will operate with reduced performance down to 4.5V. Operation between 4.5V and 4.75V will result in longer settling time, reduced performance, and current sourcing capability. Consult the "V_{DD} vs Load Current" graph in the Typical Performance Curves section for more information.

APPLICATIONS

POWER AND GROUNDING

The DAC7621 can be used in a wide variety of situations—from low power, battery operated systems to large-scale industrial process control systems. In addition, some applications require better performance than others, or are particularly sensitive to one or two specific parameters. This diversity makes it difficult to define definite rules to follow concerning the power supply, bypassing, and grounding. The following discussion must be considered in relation to the desired performance and needs of the particular system.

A precision analog component requires careful layout, adequate bypassing, and a clean, well-regulated power supply. As the DAC7621 is a single-supply, +5V component, it will often be used in conjunction with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance.

The DAC7621 has separate analog ground and digital ground pins. The current through DGND is mostly switching transients and are up to 4mA peak in amplitude. The current through AGND is typically 0.5mA.

For best performance, separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DGND and AGND be connected directly to the ground planes under the package.

If several DAC7621s are used, or if sharing supplies with other components, connecting the AGND and DGND lines together at the power supplies once, rather than at each chip, may produce better results.

The power applied to V_{DD} should be well regulated and low-noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between V_{DD} and V_{OUT}.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 10µF and 0.1µF capacitors shown in Figure 4 are strongly recommended and should be installed as close to V_{DD} and ground as possible. In some situations, additional bypassing may be required such as a 100µF electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

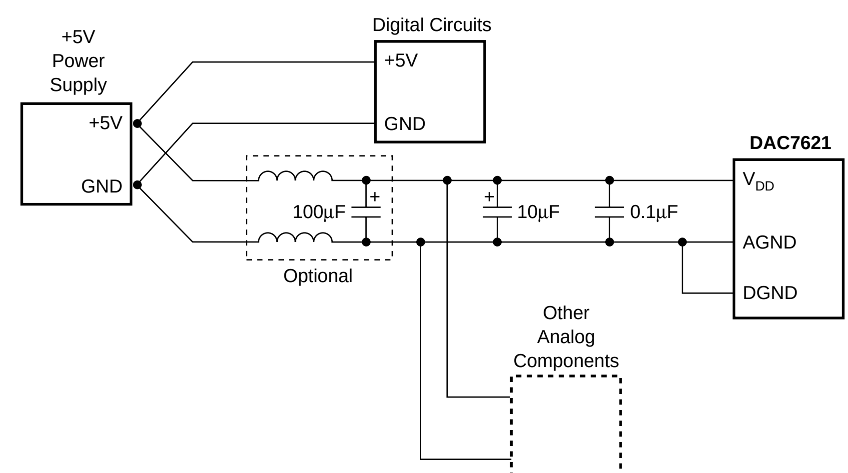


FIGURE 4. Suggested Power and Ground Connections for a DAC7621 Sharing a +5V Supply with a Digital System with a Single Ground Plane.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC7621E	ACTIVE	SSOP	DB	20	68	TBD	CU SNPB	Level-3-220C-168 HR
DAC7621E/1K	ACTIVE	SSOP	DB	20	1000	TBD	CU SNPB	Level-3-220C-168 HR
DAC7621EB	ACTIVE	SSOP	DB	20	68	TBD	CU SNPB	Level-3-220C-168 HR
DAC7621EB/1K	ACTIVE	SSOP	DB	20	1000	TBD	CU SNPB	Level-3-220C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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