

FEATURES

High common-mode voltage range

–8 V to +28 V at a 5 V supply voltage

Operating temperature range: –40°C to +125°C

Supply voltage range: 3.5 V to 12 V

Low-pass filter (1-pole or 2-pole)

EXCELLENT AC AND DC PERFORMANCE

±1 mV voltage offset

±1 ppm/°C typ gain drift

80 dB CMRR min dc to 10 kHz

PLATFORMS

Transmission control

Diesel injection control

Engine management

Adaptive suspension control

Vehicle dynamics control

GENERAL DESCRIPTION

The AD8202 is a single-supply difference amplifier for amplifying and low-pass filtering small differential voltages in the presence of a large common-mode voltage. The input CMV range extends from –8 V to +28 V at a typical supply voltage of 5 V.

The AD8202 is offered in die and packaged form. Both package options are specified over a wide temperature range of –40°C to +125°C, making the AD8202 well-suited for use in many automotive platforms.

Automotive platforms demand precision components for better system control. The AD8202 provides excellent ac and dc performance, which keeps errors to a minimum in the user's system. Typical offset and gain drift in the SOIC package are 0.3 $\mu\text{V}/^\circ\text{C}$ and 1 ppm/°C, respectively. Typical offset and gain drift in the MSOP package are 2 $\mu\text{V}/^\circ\text{C}$ and 1 ppm/°C, respectively. The device also delivers a minimum CMRR of 80 dB from dc to 10 kHz.

The AD8202 features an externally accessible 100 k Ω resistor at the output of the preamp A1, which can be used for low-pass filter applications and for establishing gains other than 20.

Rev. C

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

FUNCTIONAL BLOCK DIAGRAM

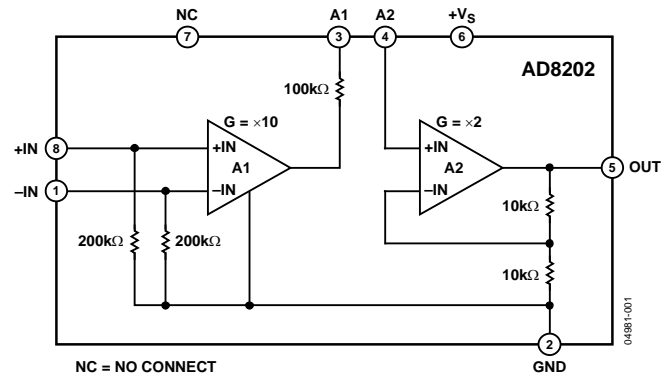


Figure 1. SOIC (R) Package Die Form

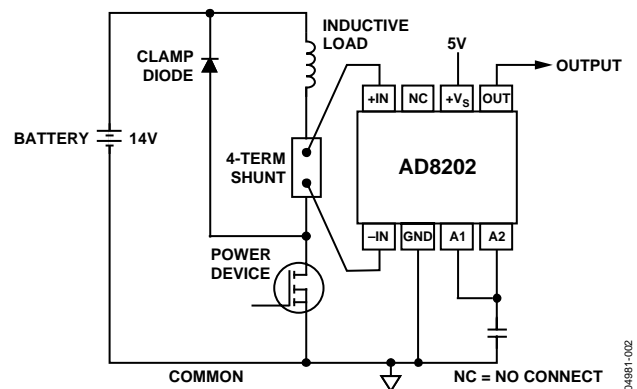


Figure 2. High-Line Current Sensor

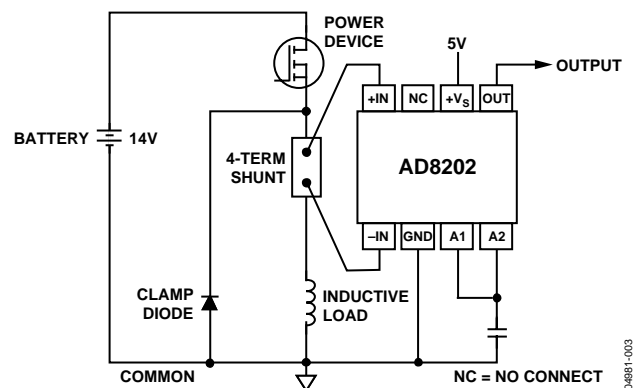


Figure 3. Low-Line Current Sensor

TABLE OF CONTENTS

Specifications—Single Supply	3	Gain Trim	14
Absolute Maximum Ratings.....	5	Low-Pass Filtering.....	14
ESD Caution.....	5	High-Line Current Sensing with LPF and Gain Adjustment.....	15
Pin Configuration and Function Descriptions.....	6	Driving Charge Redistribution ADCs.....	15
Typical Performance Characteristics	7	Outline Dimensions	16
Theory of Operation	12	Ordering Guide	16
Applications.....	13		
Current Sensing	13		
Gain Adjustment	13		

REVISION HISTORY

2/05—Rev. B to Rev. C

Changes to Table 1.....	3
Changes to Figure 14.....	8
Changes to Figure 22.....	9

1/05—Rev. A to Rev. B

Changes to the General Description.....	1
Changes to Specifications.....	3
Added Figure 14 to Figure 33.....	8
Changes to Figure 38.....	14
Changes to Figure 40 and Figure 41.....	15
Changes to Ordering Guide.....	16

11/04—Rev. 0 to Rev. A

Changes to the Features.....	1
Changes to the General Description.....	1
Changes to Specifications (Table 1)	3
Changes to Absolute Maximum Ratings (Table 2)	4
Changes to Pin Function Descriptions (Table 3)	5
Changes to Figure 5.....	5
Changes to Figure 9 and Figure 10.....	6
Updated Outline Dimensions	12
Changes to the Ordering Guide.....	12

7/04—Revision 0: Initial Version

SPECIFICATIONS—SINGLE SUPPLY

T_A = operating temperature range, $V_S = 5$ V, unless otherwise noted.

Table 1.

Parameter	Conditions	AD8202 SOIC			AD8202 MSOP			AD8202 Die			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SYSTEM GAIN											
Initial			20			20			20		V/V
Error	$0.02 \leq V_{OUT} \leq 4.8$ V dc @ 25°C	-0.3		+0.3				-0.3		+0.3	%
vs. Temperature			1	20		1	25		1	30	ppm/°C
VOLTAGE OFFSET											
Input Offset (RTI)	$V_{CM} = 0.15$ V; 25°C	-1		+1	-2		+2	-1		+1	mV
vs. Temperature	-40°C to +125°C	-10	+0.3	+10	-20	+2	+20	-10	+0.3	+10	μ V/°C
	-40°C to +150°C							-15	+5	+15	μ V/°C
INPUT											
Input Impedance											
Differential		260	325	390	260	325	390	260	325	390	k Ω
Common-Mode		135	170	205	135	170	205	135	170	205	k Ω
CMV	Continuous	-8		+28	-8		+28	-8		+28	V
Common-Mode Rejection ¹	$V_{CM} = -8$ V to +28 V										
	f = dc	82			82			82			dB
	f = 1 kHz	82			82			82			dB
	f = 10 kHz ²	80			80			80			dB
PREAMPLIFIER											
Gain			10			10			10		V/V
Gain Error		-0.3		+0.3	-0.3		+0.3	-0.3		+0.3	%
Output Voltage Range		0.02		4.8	0.02		4.8	0.02		4.8	V
Output Resistance		97	100	103	97	100	103	97	100	103	k Ω
OUTPUT BUFFER											
Gain			2			2			2		V/V
Gain Error	$0.02 \leq V_{OUT} \leq 4.8$ V dc	-0.3		+0.3	-0.3		+0.3	-0.3		+0.3	%
Output Voltage Range		0.02		4.8	0.02		4.8	0.02		4.8	V
Input Bias Current			40			40			40		nA
Output Resistance			2			2			2		Ω
DYNAMIC RESPONSE											
System Bandwidth	$V_{IN} = 0.1$ V p-p; $V_{OUT} = 2.0$ V p-p	30	50		30	50		30	50		kHz
Slew Rate	$V_{IN} = 0.2$ V dc; $V_{OUT} = 4$ V step		0.28			0.28			0.28		V/ μ s
NOISE											
0.1 Hz to 10 Hz			10			10			10		μ V p-p
Spectral Density, 1 kHz (RTI)			275			275			275		nV/ \sqrt Hz
POWER SUPPLY											
Operating Range		3.5		12	3.5		12	3.5		12	V
Quiescent Current vs. Temperature	$V_O = 0.1$ V dc		0.25	1.0		0.25	1.0		0.25	1.0	mA
PSRR	$V_S = 3.5$ V to 12 V	75	83		75	83		75	83		dB
TEMPERATURE RANGE											
For Specified Performance		-40		+125	-40		+125	-40		+150	°C

See notes on next page.

AD8202

¹ Source imbalance < 2 Ω .

² The AD8202 preamplifier exceeds 80 dB CMRR at 10 kHz. However, because the signal is available only by way of a 100 k Ω resistor, even the small amount of pin-to-pin capacitance between Pins 1, 8 and 3, 4 might couple an input common-mode signal larger than the greatly attenuated preamplifier output. The effect of pin-to-pin coupling can be neglected in all applications by using filter capacitors at Node 3.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	12.5 V
Transient Input Voltage (400 ms)	44 V
Continuous Input Voltage (Common Mode)	35 V
Reversed Supply Voltage Protection	0.3 V
Operating Temperature Range	
Die	−40°C to +150°C
SOIC	−40°C to +125°C
MSOP	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Output Short-Circuit Duration	Indefinite
Lead Temperature Range (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD8202

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

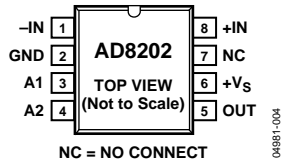


Figure 4. 8-Lead SOIC

Table 3. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	X	Y
1	-IN	-409.0	-205.2
2	GND	-244.6	-413.0
3	A1	+229.4	-413.0
4	A2	+410.0	-308.6
5	OUT	+410.0	+272.4
6	+Vs	+121.0	+417.0
7	NC	NA	NA
8	+IN	-409.0	+205.2

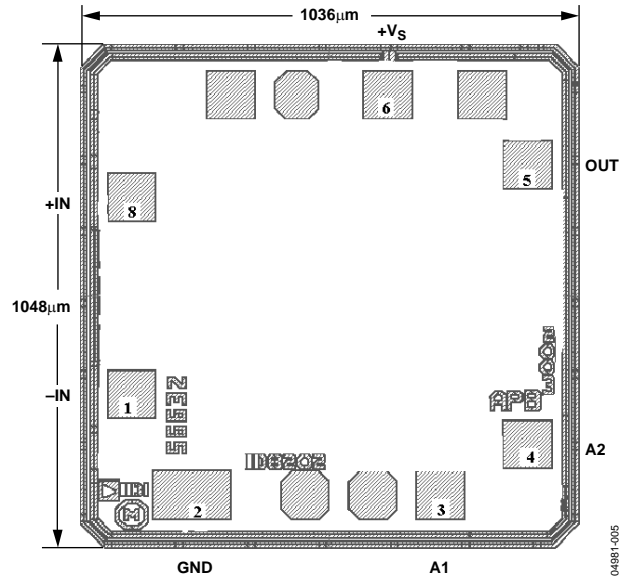


Figure 5. Metallization Photograph

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = 0\text{ V}$, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

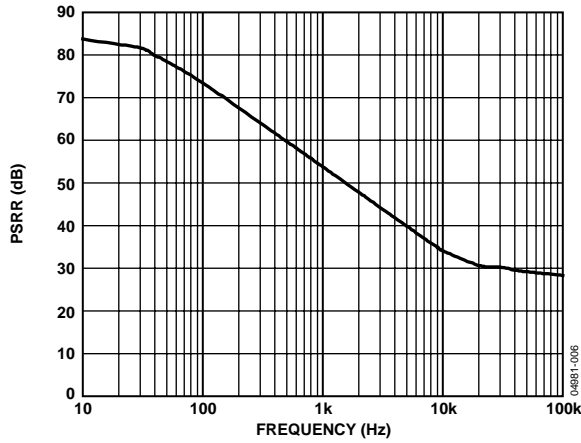


Figure 6. Power Supply Rejection Ratio vs. Frequency Valid for CM Range -8 V to $+28\text{ V}$

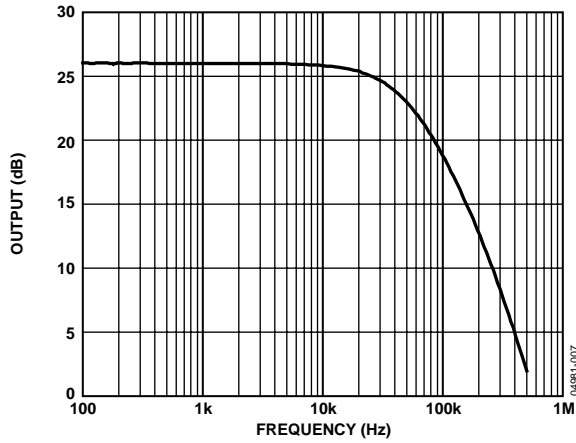


Figure 7. AD8202 Bandwidth

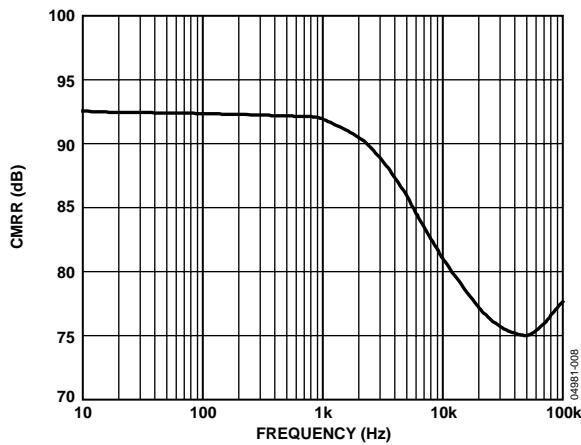


Figure 8. Common-Mode Rejection Ratio vs. Frequency Valid for CM Range -8 V to $+28\text{ V}$

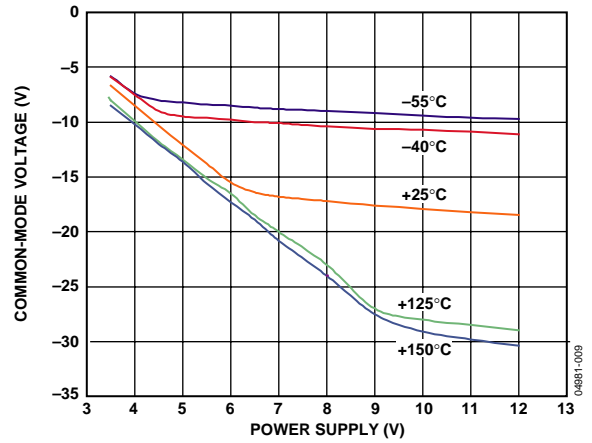


Figure 9. Negative Common-Mode Voltage vs. Voltage Supply

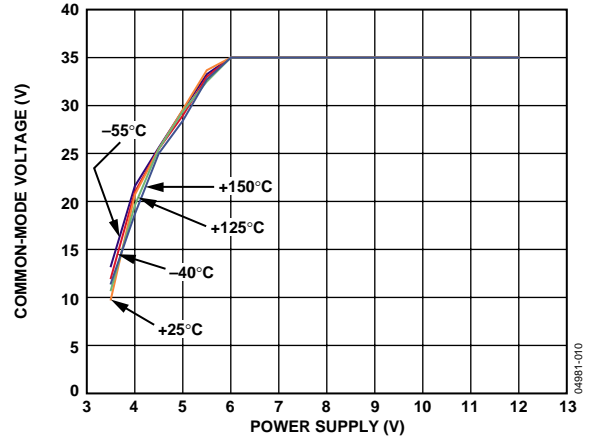


Figure 10. Positive Common-Mode Voltage vs. Voltage Supply

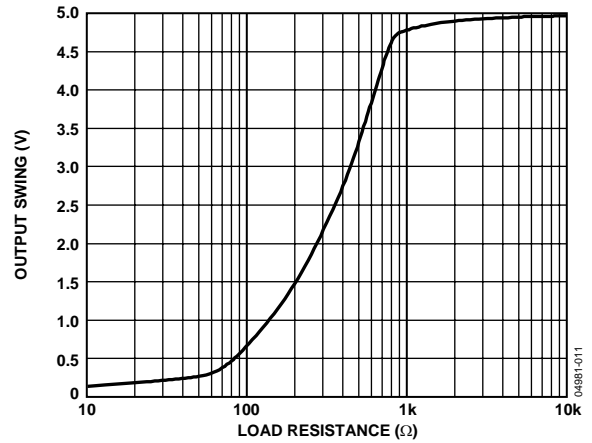


Figure 11. Output Swing vs. Load Resistance

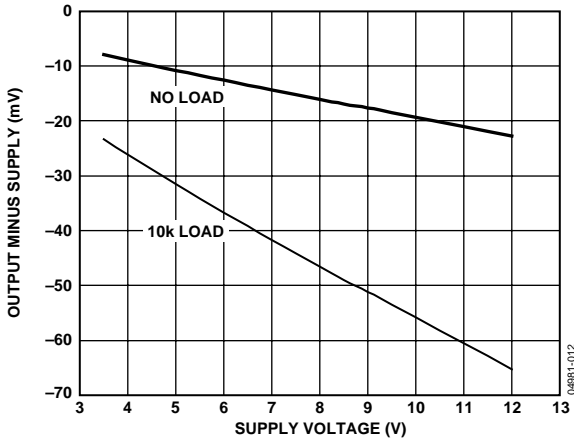


Figure 12. Output Minus Supply vs. Supply Voltage

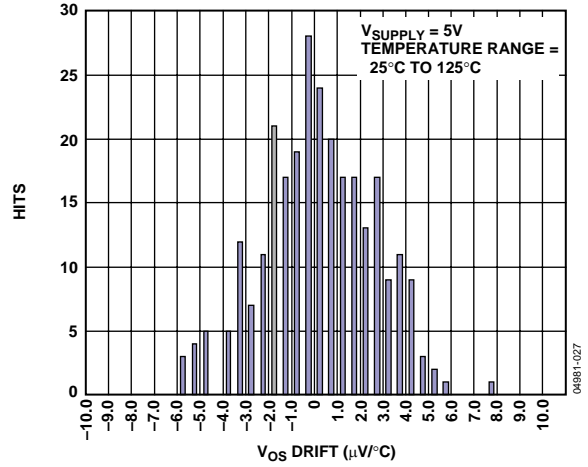


Figure 15. Offset Drift Distribution, SOIC

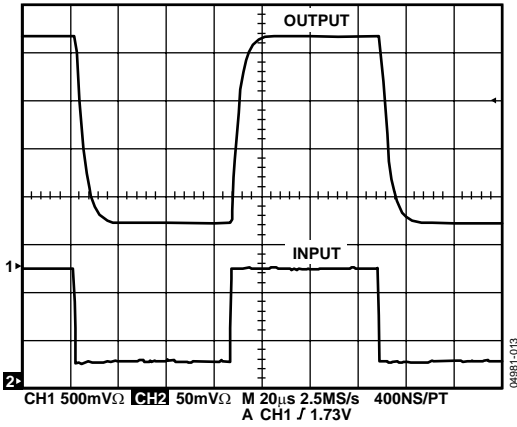


Figure 13. Pulse Response

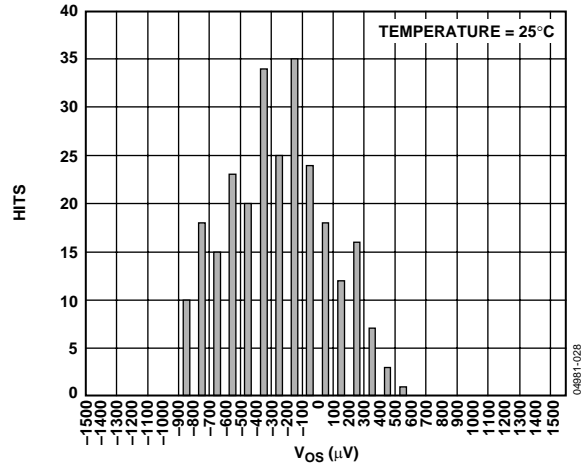


Figure 16. V_{OS} Distribution, SOIC

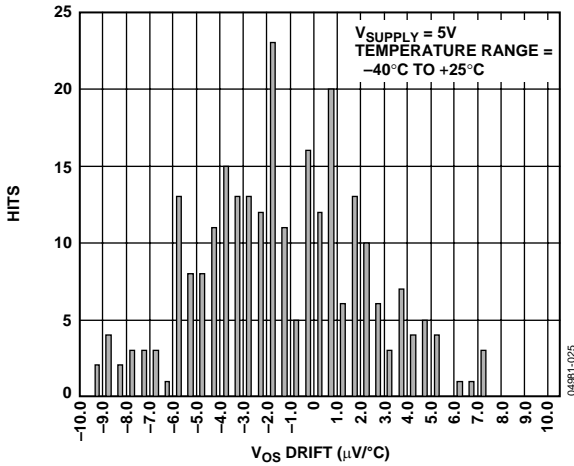


Figure 14. Offset Drift Distribution, SOIC

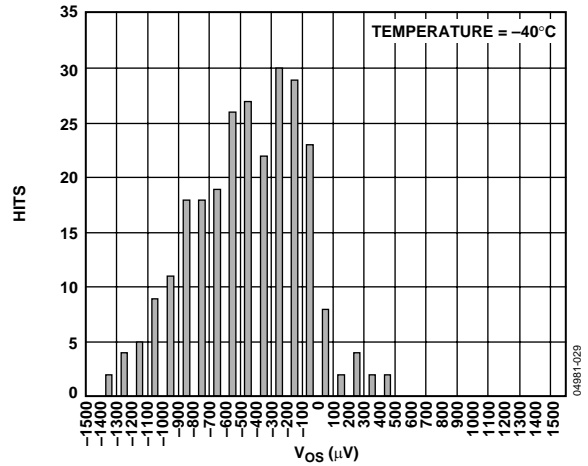


Figure 17. V_{OS} Distribution, SOIC

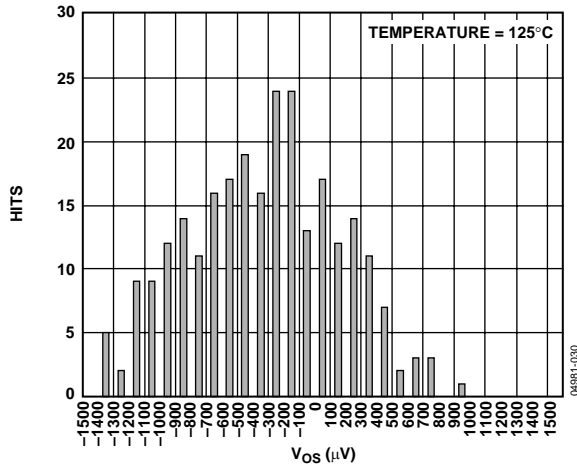


Figure 18. V_{OS} Distribution, SOIC

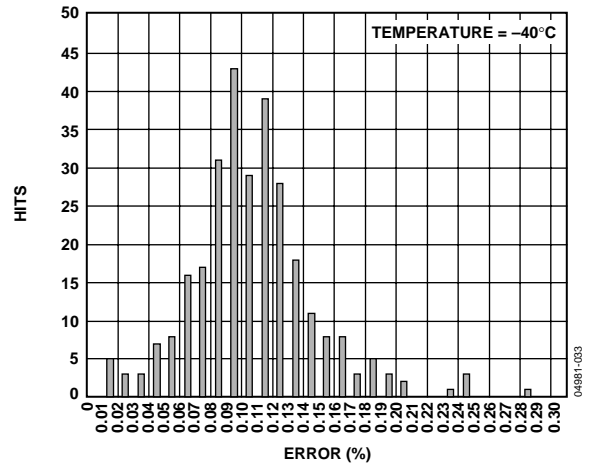


Figure 21. SOIC Gain Accuracy

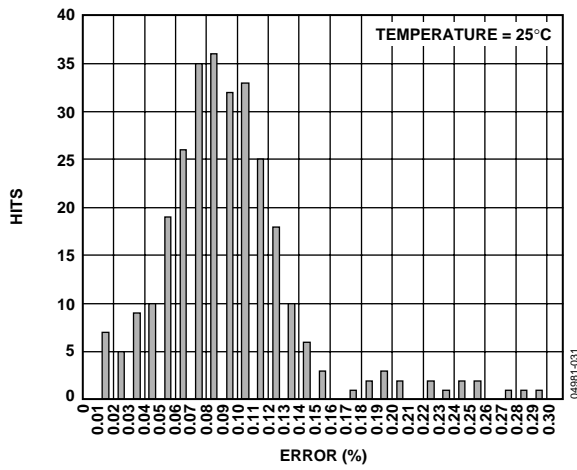


Figure 19. SOIC Gain Accuracy

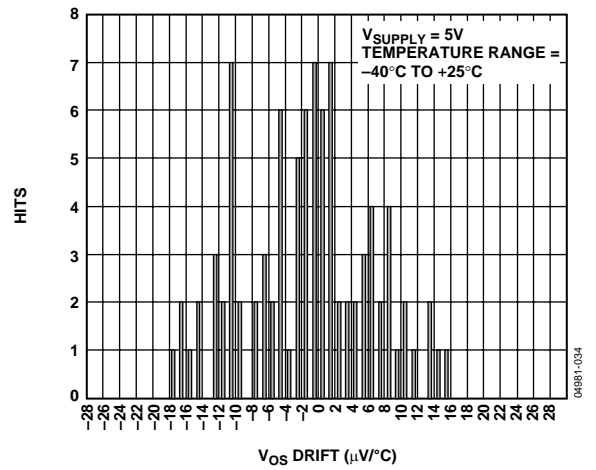


Figure 22. Offset Drift Distribution, MSOP

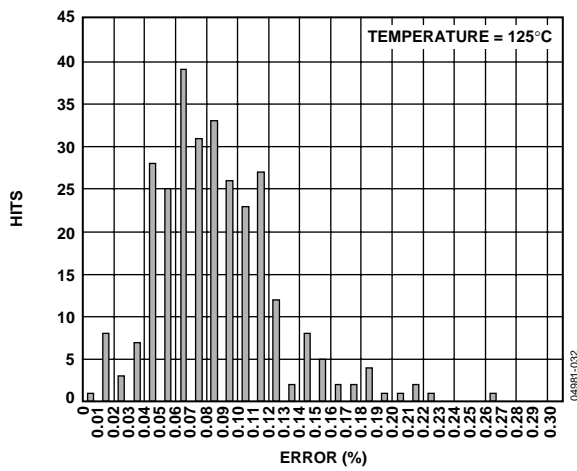


Figure 20. SOIC Gain Accuracy

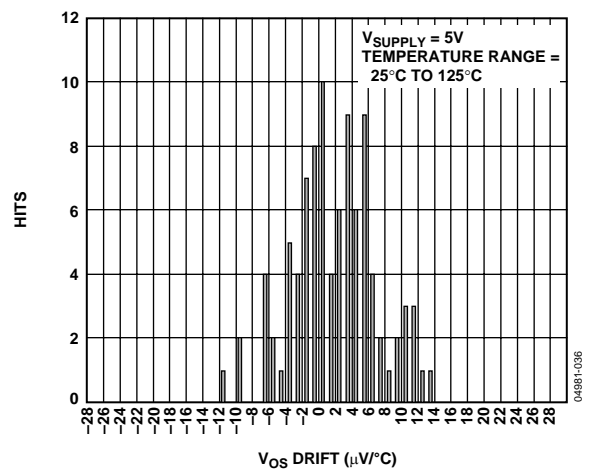


Figure 23. Offset Drift Distribution, MSOP

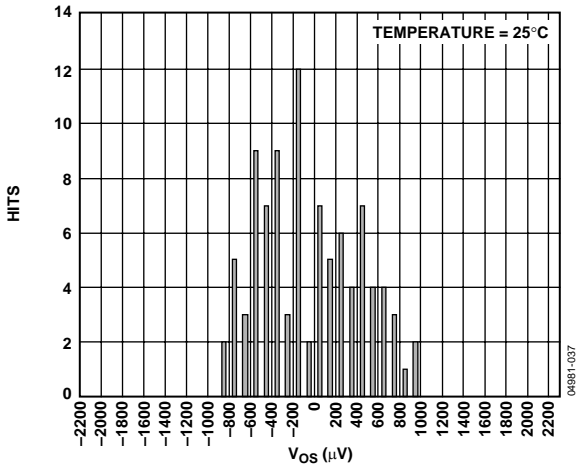


Figure 24. V_{OS} Distribution, MSOP

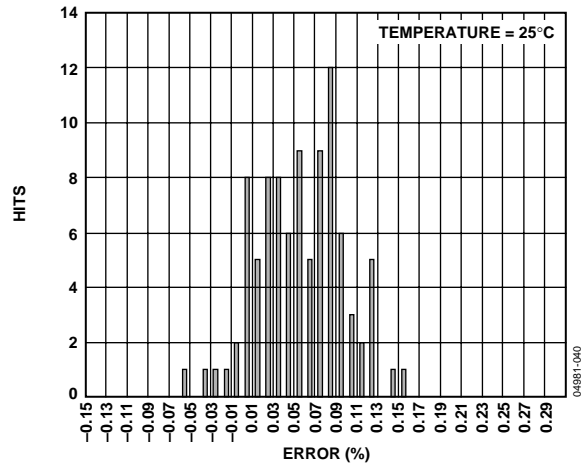


Figure 27. MSOP Gain Accuracy

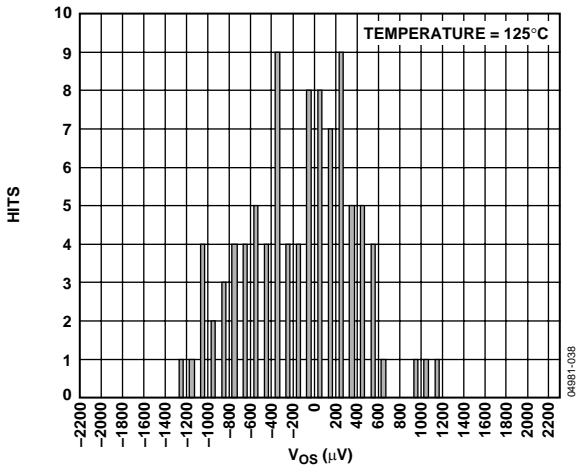


Figure 25. V_{OS} Distribution, MSOP

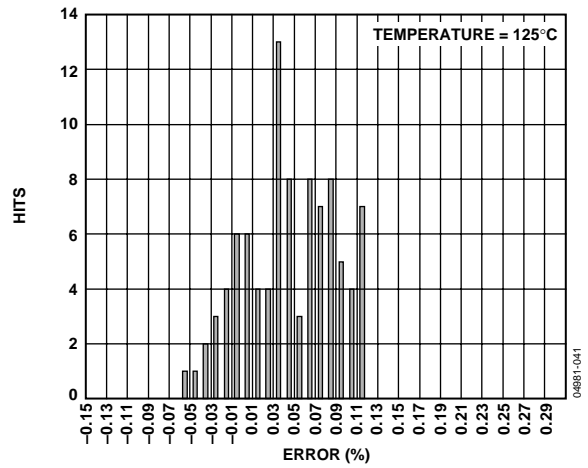


Figure 28. MSOP Gain Accuracy

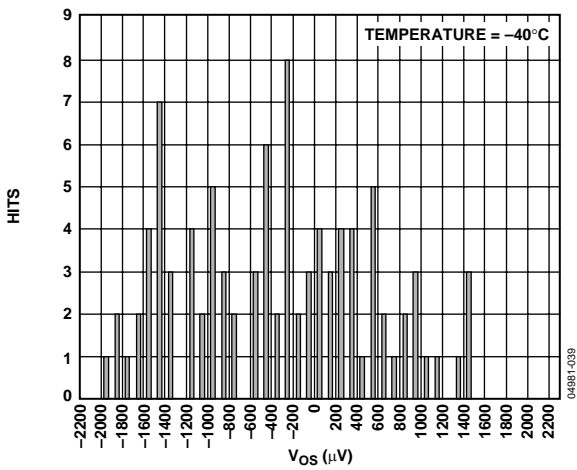


Figure 26. V_{OS} Distribution, MSOP

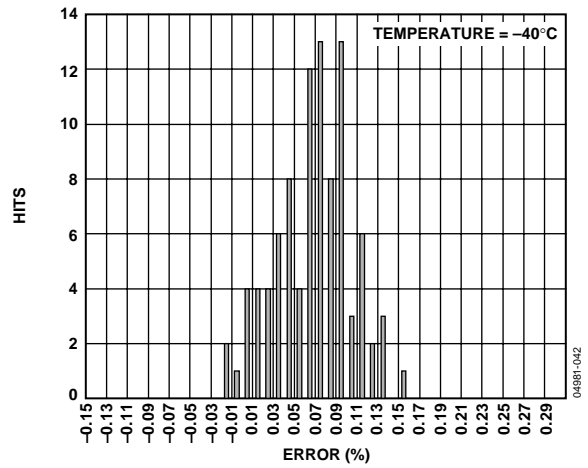


Figure 29. MSOP Gain Accuracy

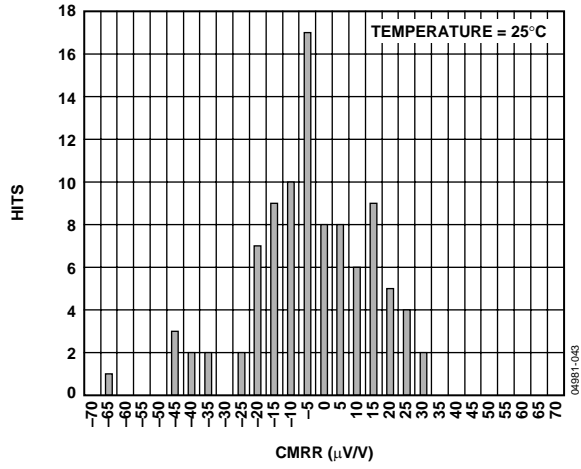


Figure 30. CMRR Distribution, -8 V to +28 V Common Mode

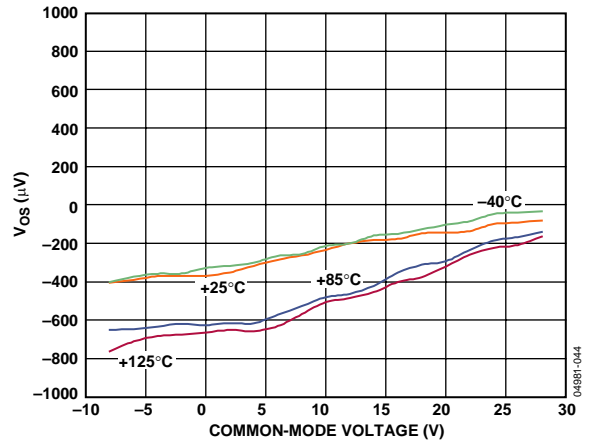


Figure 31. Vos vs. Common-Mode Voltage

THEORY OF OPERATION

The AD8202 consists of a preamp and buffer arranged as shown in Figure 32. Like-named resistors have equal values.

The preamp uses a dynamic bridge (subtractor) circuit. Identical networks (within the shaded areas), consisting of R_A , R_B , R_C , and R_G , attenuate input signals applied to Pins 1 and 8. When equal amplitude signals are asserted at inputs 1 and 8, and the output of A1 is equal to the common potential (that is, 0), the two attenuators form a balanced-bridge network. When the bridge is balanced, the differential input voltage at A1, and thus its output, is 0.

Any common-mode voltage applied to both inputs keeps the bridge balanced and the A1 output at zero. Because the resistor networks are carefully matched, the common-mode signal rejection approaches this ideal state.

However, if the signals applied to the inputs differ, the result is a difference at the input to A1. A1 responds by adjusting its output to drive R_B , by way of R_G , to adjust the voltage at its inverting input until it matches the voltage at its noninverting input.

By attenuating voltages at Pins 1 and 8, the amplifier inputs are held within the power supply range, even if Pin 1 and Pin 8 input levels exceed the supply or fall below common (ground). The input network also attenuates normal (differential) mode voltages. R_C and R_G form an attenuator that scales A1 feedback, forcing large output signals to balance relatively small differential inputs. The resistor ratios establish the preamp gain at 10.

Because the differential input signal is attenuated and then amplified to yield an overall gain of 10, Amplifier A1 operates at a higher noise gain, multiplying deficiencies such as input offset voltage and noise with respect to Pins 1 and 8.

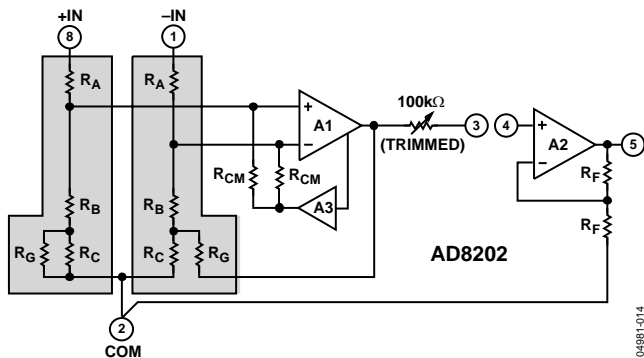


Figure 32. Simplified Schematic

To minimize these errors while extending the common-mode range, a dedicated feedback loop is employed to reduce the range of common-mode voltage applied to A1 for a given over-all range at the inputs. By offsetting the voltage range applied to the compensator, the input common-mode range is also offset to include voltages more negative than the power supply. Amplifier A3 detects the common-mode signal applied to A1 and adjusts the voltage on the matched R_{CM} resistors to reduce the common-mode voltage range at the A1 inputs. By adjusting the common voltage of these resistors, the common-mode input range is extended while, at the same time, the normal mode signal attenuation is reduced, leading to better performance referred to input.

The output of the dynamic bridge taken from A1 is connected to Pin 3 by way of a 100 k Ω series resistor, provided for low-pass filtering and gain adjustment. The resistors in the input networks of the preamp and the buffer feedback resistors are ratio trimmed for high accuracy.

The output of the preamp drives a gain-of-2 buffer amplifier, A2, implemented with carefully matched feedback resistors, R_F .

The 2-stage system architecture of the AD8202 enables the user to incorporate a low-pass filter prior to the output buffer. By separating the gain into two stages, a full-scale, rail-to-rail signal from the preamp can be filtered at Pin 3, and a half-scale signal, resulting from filtering, can be restored to full scale by the output buffer amp. The source resistance seen by the inverting input of A2 is approximately 100 k Ω to minimize the effects of A2's input bias current. However, this current is quite small and errors resulting from applications that mismatch the resistance are correspondingly small.

APPLICATIONS

The AD8202 difference amplifier is intended for applications where it is required to extract a small differential signal in the presence of large common-mode voltages. The differential input resistance is nominally 325 k Ω , and the device can tolerate common-mode voltages higher than the supply voltage and lower than ground.

The open-collector output stage sources current to within 20 mV of ground and to within 200 mV of V_S .

CURRENT SENSING

High-Line, High Current Sensing

Basic automotive applications using the large common-mode range are shown in Figure 2 and Figure 3. The capability of the device to operate as an amplifier in primary battery-supply circuits is shown in Figure 2; Figure 3 illustrates the ability of the device to withstand voltages below system ground.

Low Current Sensing

The AD8202 can also be used in low current sensing applications, such as the 4 to 20 mA current loop shown in Figure 33. In such applications, the relatively large shunt resistor can degrade the common-mode rejection. Adding a resistor of equal value on the low impedance side of the input corrects for this error.

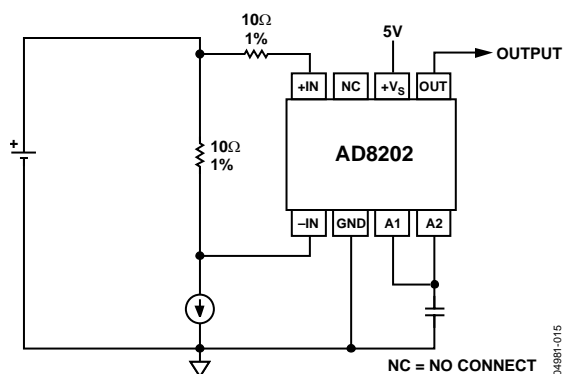


Figure 33. 4 to 20 mA Current Loop Receiver

GAIN ADJUSTMENT

The default gain of the preamplifier and buffer are $\times 10$ and $\times 2$, respectively, resulting in a composite gain of $\times 20$. With the addition of external resistor(s) or trimmer(s), the gain may be lowered, raised, or finely calibrated.

Gains Less than 20

Because the preamplifier has an output resistance of 100 k Ω , an external resistor connected from Pins 3 and 4 to GND decreases the gain by a factor $R_{EXT}/(100\text{ k}\Omega + R_{EXT})$ as shown in Figure 34.

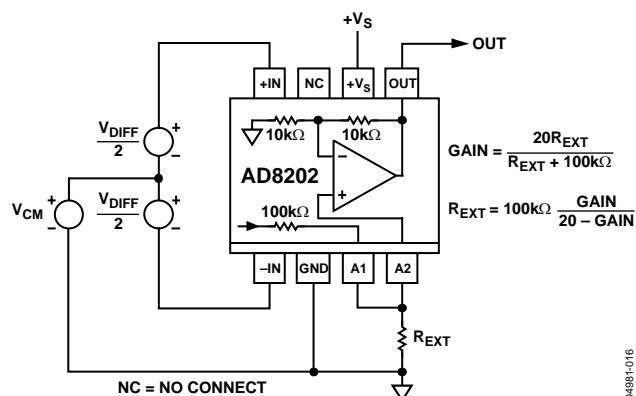


Figure 34. Adjusting for Gains Less than 20

The overall bandwidth is unaffected by changes in gain by using this method, although there may be a small offset voltage due to the imbalance in source resistances at the input to the buffer. In many cases this can be ignored, but if desired, it can be nulled by inserting a resistor equal to 100 k Ω minus the parallel sum of R_{EXT} and 100 k Ω , in series with Pin 4. For example, with $R_{EXT} = 100\text{ k}\Omega$ (yielding a composite gain of $\times 10$), the optional offset nulling resistor is 50 k Ω .

Gains Greater than 20

Connecting a resistor from the output of the buffer amplifier to its noninverting input, as shown in Figure 35, increases the gain. The gain is multiplied by the factor $R_{EXT}/(R_{EXT} - 100\text{ k}\Omega)$; for example, it is doubled for $R_{EXT} = 200\text{ k}\Omega$. Overall gains as high as 50 are achievable in this way. The accuracy of the gain becomes critically dependent on the resistor value at high gains. Also, the effective input offset voltage at Pin 1 and Pin 8 (about six times the actual offset of A1) limits the part's use in high gain, dc-coupled applications.

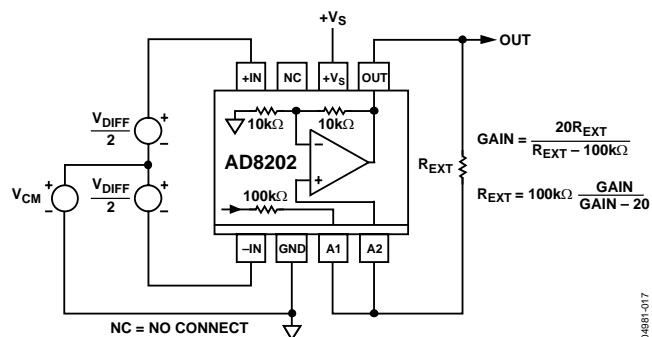


Figure 35. Adjusting for Gains Greater than 20

AD8202

GAIN TRIM

Figure 36 shows a method for incremental gain trimming by using a trim potentiometer and external resistor, R_{EXT} .

The following approximation is useful for small gain ranges:

$$\Delta G \approx (10 \text{ M}\Omega \div R_{EXT})\%$$

Thus, the adjustment range is $\pm 2\%$ for $R_{EXT} = 5 \text{ M}\Omega$; $\pm 10\%$ for $R_{EXT} = 1 \text{ M}\Omega$, and so on.

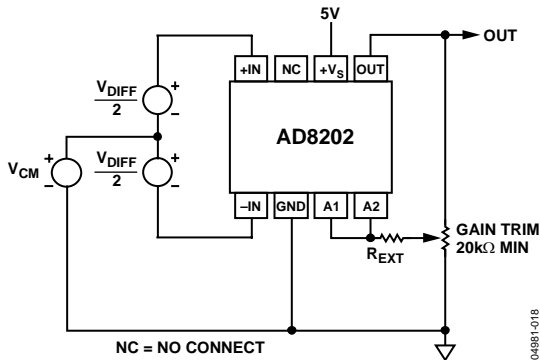


Figure 36. Incremental Gain Trim

Internal Signal Overload Considerations

When configuring gain for values other than 20, the maximum input voltage with respect to the supply voltage and ground must be considered, because either the preamplifier or the output buffer reaches its full-scale output (approximately $V_s - 0.2 \text{ V}$) with large differential input voltages. The input of the AD8202 is limited to $(V_s - 0.2) \div 10$ for overall gains ≤ 10 , because the preamplifier, with its fixed gain of $\times 10$, reaches its full-scale output before the output buffer. For gains greater than 10, the swing at the buffer output reaches its full scale first and limits the AD8202 input to $(V_s - 0.2) \div G$, where G is the overall gain.

LOW-PASS FILTERING

In many transducer applications, it is necessary to filter the signal to remove spurious high frequency components including noise, or to extract the mean value of a fluctuating signal with a peak-to-average ratio (PAR) greater than unity. For example, a full-wave rectified sinusoid has a PAR of 1.57, a raised cosine has a PAR of 2, and a half-wave sinusoid has a PAR of 3.14. Signals having large spikes may have PARs of 10 or more.

When implementing a filter, the PAR should be considered so that the output of the AD8202 preamplifier (A1) does not clip before A2, because this nonlinearity would be averaged and appear as an error at the output. To avoid this error, both amplifiers should clip at the same time. This condition is achieved when the PAR is no greater than the gain of the second amplifier (2 for the default configuration). For example, if a PAR of 5 is expected, the gain of A2 should be increased to 5.

Low-pass filters can be implemented in several ways by using the AD8202. In the simplest case, a single-pole filter (20 dB/decade) is formed when the output of A1 is connected to the input of A2 via the internal $100 \text{ k}\Omega$ resistor by tying Pin 3 and Pin 4 and adding a capacitor from this node to ground, as shown in Figure 37. If a resistor is added across the capacitor to lower the gain, the corner frequency increases; it should be calculated using the parallel sum of the resistor and $100 \text{ k}\Omega$.

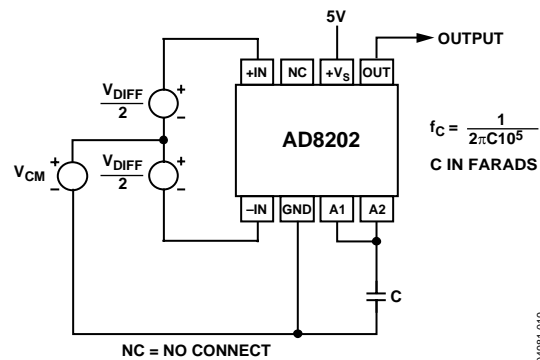


Figure 37. Single-Pole, Low-Pass Filter Using the Internal $100 \text{ k}\Omega$ Resistor

If the gain is raised using a resistor, as shown in Figure 35, the corner frequency is lowered by the same factor as the gain is raised. Thus, using a resistor of $200 \text{ k}\Omega$ (for which the gain would be doubled), the corner frequency is now $0.796 \text{ Hz}/\mu\text{F}$ ($0.039 \mu\text{F}$ for a 20 Hz corner frequency.)

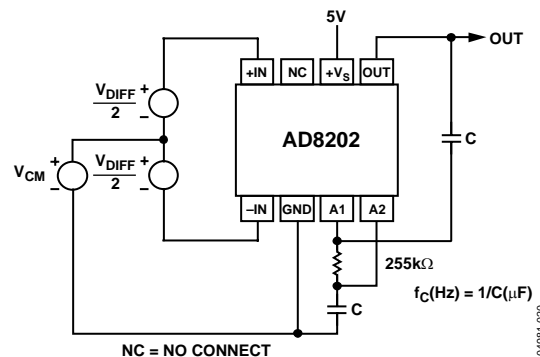


Figure 38. 2-Pole, Low-Pass Filter

A 2-pole filter (with a roll-off of 40 dB/decade) can be implemented using the connections shown in Figure 38. This is a Sallen-Key form based on a $\times 2$ amplifier. It is useful to remember that a 2-pole filter with a corner frequency f_2 and a 1-pole filter with a corner at f_1 have the same attenuation at the frequency (f_2^2/f_1) . The attenuation at that frequency is $40 \log (f_2/f_1)$, which is illustrated in Figure 39. Using the standard resistor value shown and equal capacitors (Figure 38), the corner frequency is conveniently scaled at $1 \text{ Hz}/\mu\text{F}$ ($0.05 \mu\text{F}$ for a 20 Hz corner). A maximally flat response occurs when the resistor is lowered to $196 \text{ k}\Omega$ and the scaling is then $1.145 \text{ Hz}/\mu\text{F}$. The output offset is raised by approximately 5 mV (equivalent to $250 \mu\text{V}$ at the input pins).

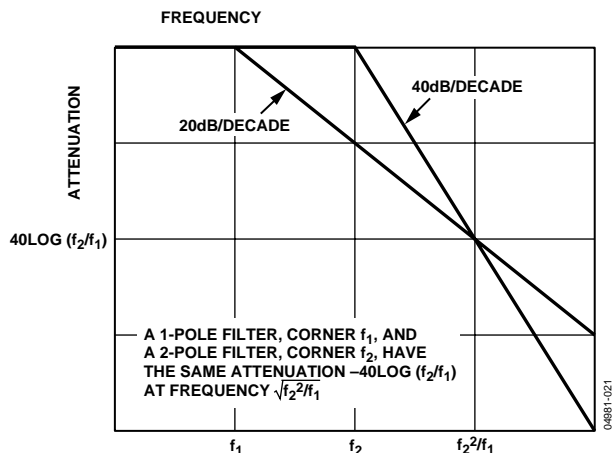


Figure 39. Comparative Responses of 1-Pole and 2-Pole Low-Pass Filters

HIGH-LINE CURRENT SENSING WITH LPF AND GAIN ADJUSTMENT

Figure 40 is another refinement of Figure 2, including gain adjustment and low-pass filtering.

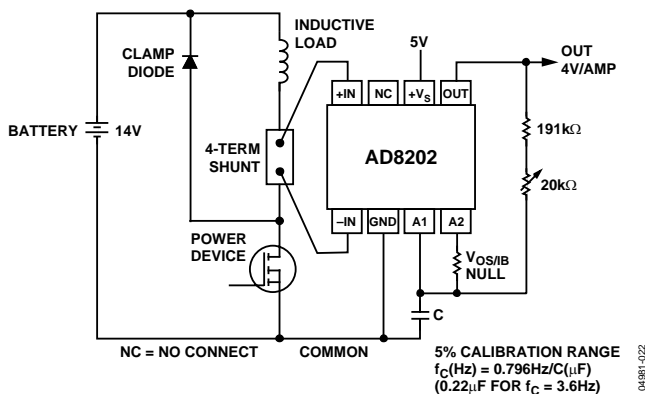


Figure 40. High-Line Current Sensor Interface; Gain = ×40, Single-Pole, Low-Pass Filter

A power device that is either on or off controls the current in the load. The average current is proportional to the duty cycle of the input pulse and is sensed by a small value resistor. The average differential voltage across the shunt is typically 100 mV, although its peak value is higher by an amount that depends on the inductance of the load and the control frequency. The common-mode voltage, conversely, extends from roughly 1 V above ground for the on condition to about 1.5 V above the battery voltage in the off condition. The conduction of the clamping diode regulates the common-mode potential applied to the device. For example, a battery spike of 20 V may result in an applied common-mode potential of 21.5 V to the input of the devices.

To produce a full-scale output of 4 V, a gain ×40 is used, adjustable by ±5% to absorb the tolerance in the shunt. Sufficient headroom allows 10% overrange (to 4.4 V). The roughly triangular voltage across the sense resistor is averaged by a 1-pole,

low-pass filter, set here with a corner frequency of 3.6 Hz, which provides about 30 dB of attenuation at 100 Hz. A higher rate of attenuation can be obtained using a 2-pole filter with $f_c = 20$ Hz, as shown in Figure 41. Although this circuit uses two separate capacitors, the total capacitance is less than half that needed for the 1-pole filter.

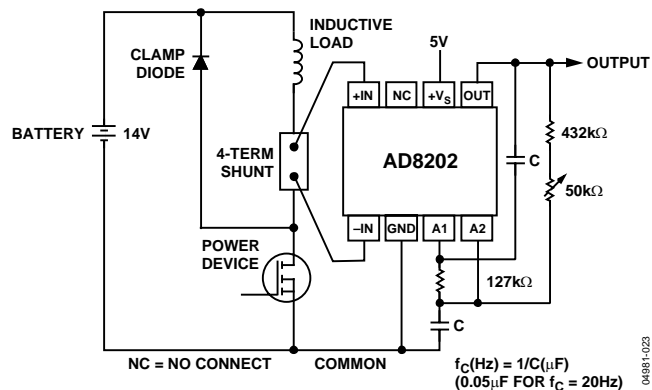


Figure 41. 2-Pole Low-Pass Filter

DRIVING CHARGE REDISTRIBUTION ADCS

When driving CMOS ADCs such as those embedded in popular microcontrollers, the charge injection (ΔQ) can cause a significant deflection in the output voltage of the AD8202. Though generally of short duration, this deflection may persist until after the sample period of the ADC expires due to the relatively high open-loop output impedance (typ 21 k Ω) of the AD8202. Including an R-C network in the output can significantly reduce the effect. The capacitor helps to absorb the transient charge, effectively lowering the high frequency output impedance of the AD8202. For these applications, the output signal should be taken from the midpoint of the $R_{LAG} - C_{LAG}$ combination, as shown in Figure 42.

Because the perturbations from the analog-to-digital converter are small, the output impedance of the AD8202 appears to be low. The transient response, therefore, has a time constant governed by the product of the two LAG components, $C_{LAG} \times R_{LAG}$. For the values shown in Figure 42, this time constant is programmed at approximately 10 μs . Therefore, if samples are taken at several tenths of microseconds or more, there is negligible charge stack-up.

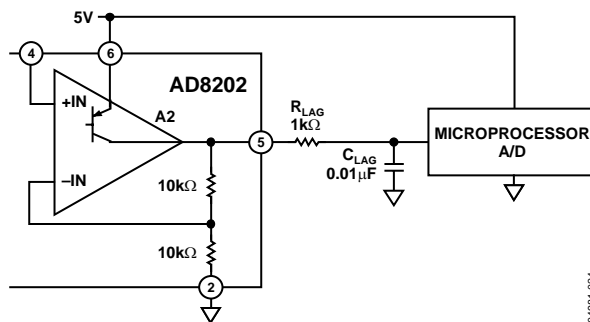
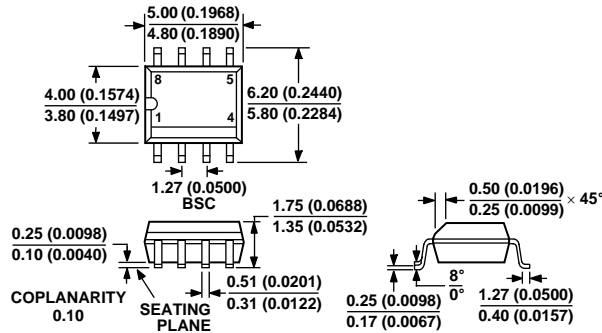


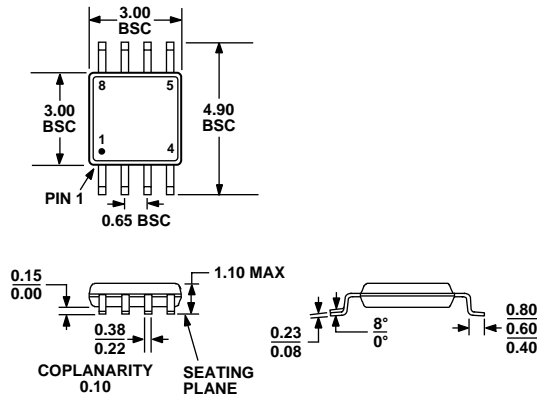
Figure 42. Recommended Circuit for Driving CMOS A/D

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N], Narrow Body (R-8), Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 44. 8-Lead Mini Small Outline Package [MSOP], (RM-8), Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline	Branding
AD8202YR	-40°C to +125°C	8 Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YR-REEL	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YR-REEL7	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YRZ ¹	-40°C to +125°C	8 Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YRZ-RL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YRZ-R7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8202YRMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	JWY
AD8202YRMZ-RL ¹	-40°C to +125°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	JWY
AD8202YRMZ-R7 ¹	-40°C to +125°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	JWY
AD8202YCSURF		Die		

¹ Z = Pb-free part.