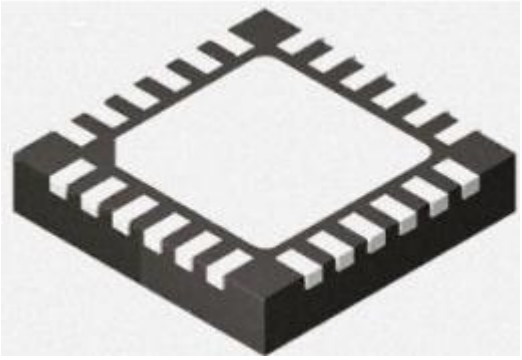
TEXAS INSTRUMENTS

CDCLVP2102 Four LVPECL Output Clock Buffer

General Description:

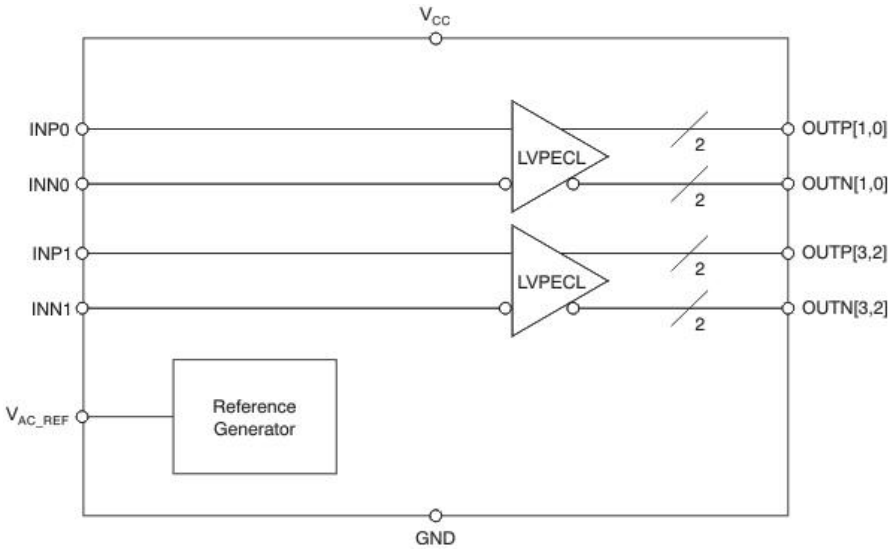
The CDCLVP2102 is a highly versatile, low additive jitter buffer that can generate four copies of LVPECL clock outputs from two LVPECL, LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. Each buffer block consists of one input that feeds two LVPECL outputs. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 10 ps, making the device a perfect choice for use in demanding applications.



The CDCLVP2102 clock buffer distributes two clock inputs (IN0, IN1) to four pairs of differential LVPECL clock outputs (OUT0, OUT3) with minimum skew for clock distribution. Each buffer block consists of one input that feeds two LVPECL clock outputs.

Key Features:

- Dual 1:2 Differential Buffer
- Two Clock Inputs
- Universal Inputs Can Accept LVPECL, LVDS, LVCMOS/LVTTL
- Four LVPECL Outputs
- Maximum Clock Frequency: 2 GHz
- Maximum Core Current Consumption: 48 mA
- Very Low Additive Jitter: <100 fs,rms in 10-kHz to 20-MHz Offset Range



- 2.375-V to 3.6-V Device Power Supply
- Maximum Propagation Delay: 450 ps
- Maximum Within Bank Output Skew: 10 ps
- LVPECL Reference Voltage, VAC_REF, Available for Capacitive-Coupled Inputs
- Industrial Temperature Range: –40°C to +85°C
- Available in 3-mm × 3-mm QFN-16 (RGT) Package
- ESD Protection Exceeds 2 kV (HBM)

Applications:

- Wireless Communications
- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment

Related Products Information:

Mfr Part #	Farnell #	Newark #	Description
CDCLVP2102RGTT	1778214	50R7243	Four LVPECL Output Clock Buffer
CDCLVP2108RGZT	1755711	14R9548	LOW JITTER, DUAL, 1:8 LVPECL BUFFER
CDCLVP215RHBT	1689415	45P3336	CLOCK DRIVER, DUAL, 1:5 DIFF, 32QFN
CDCLVP2104RHDT	1781316	50R9644	Clock IC