PKS603-607

PeakSwitch® Family

Enhanced, Energy-Efficient, Off-Line Switcher IC With Super Peak Power Performance

Product Highlights

EcoSmart®– Extremely Energy-Efficient

- Standby output power ≥0.6 W for 1 W input (high line)
- Sleep mode power ≥2.4 W at 3 W input (high line)
- No-load consumption <200 mW at 265 VAC input
- Surpasses California Energy Commission (CEC), ENERGY STAR, and EU requirements

PeakSwitch Features Reduce System Cost

- Delivers peak power of up to three times maximum continuous output power
- 277 kHz operation during peak power signi f cantly reduces transformer size
- Programmable smart AC line sensing provides latching shutdown during short circuit, overload and open loop faults, and prevents glitches during power down or brownout
- Two external components reset latch on AC removal
- Adaptive switching cycle on-time extension increases low line peak output power, minimizing bulk capacitor size
- Adaptive current limit reduces output overload power
- Frequency jittering reduces EMI f lter cost
- Tight I^2f tolerances and negligible temperature variation of key parameters ease design and lower cost
- Accurate hysteretic thermal shutdown with automatic recovery provides complete system level overload protection and eliminates need for manual reset

Better System Cost/Performance over RCC & Discrete

- Simple ON/OFF control – no loop compensation needed
- Very low component count – higher reliability and single side printed circuit board
- High bandwidth provides fast turn on with no overshoot and excellent transient load response
- Peak current limit operation rejects line frequency ripple
- Built-in current limit and hysteretic thermal protection

Applications

- Inkjet printer
- Data storage, audio ampli f er, DC motor drives

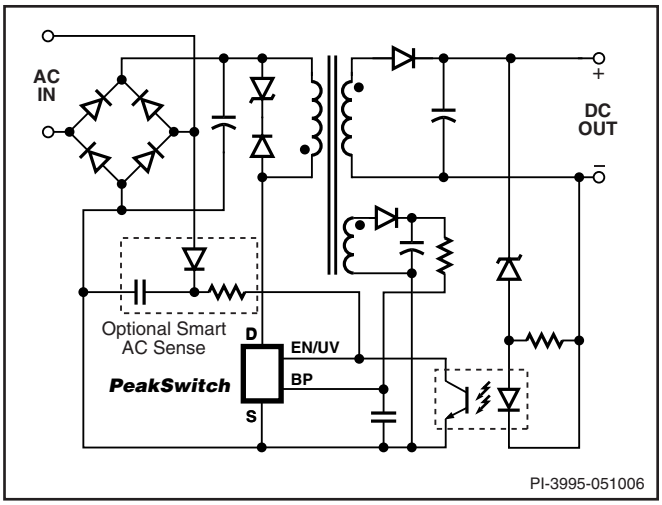

Figure 1. Typical Peak Power Application.

OUTPUT POWER TABLE				
PRODUCT[3]	230 VAC ±15%		85-265 VAC	
	Adapter Cont.[1]	Adapter Peak[2]	Adapter Cont.[1]	Adapter Peak[2]
PKS603 P	13 W	32 W	9 W	25 W
PKS604 P	23 W	56 W	16 W	44 W
PKS604 Y/F	35 W	56 W	23 W	44 W
PKS605 P	31 W	60 W	21 W	44 W
PKS605 Y/F	46 W	79 W	30 W	58 W
PKS606 P	35 W	66 W	25 W	46 W
PKS606 Y/F	68 W	117 W	45 W	86 W
PKS607 Y/F	75 W	126 W	50 W	93 W

Table 1.

Notes:
1. Typical continuous power in a non-ventilated enclosed adapter measured at +50 °C ambient.
2. Typical peak power for a period of 100 ms and a duty cycle of 10% in a non-ventilated enclosed adapter measured at +50 °C (see Key Applications section for details).
3. See Part Ordering Information.

Description

PeakSwitch is designed to address applications with high peak-to-continuous power ratio demands. The very high switching frequency during peak power loads and excellent load transient response reduce system cost as well as component count and size. *PeakSwitch* incorporates a 700 V power MOSFET, oscillator, high voltage switched current source for startup, current limit, and thermal shutdown onto a monolithic device. In addition, these devices incorporate auto-restart, line under-voltage sense and frequency jittering. An innovative design minimizes audio frequency components in the simple ON/OFF control scheme to practically eliminate audible noise with standard varnished transformer construction.

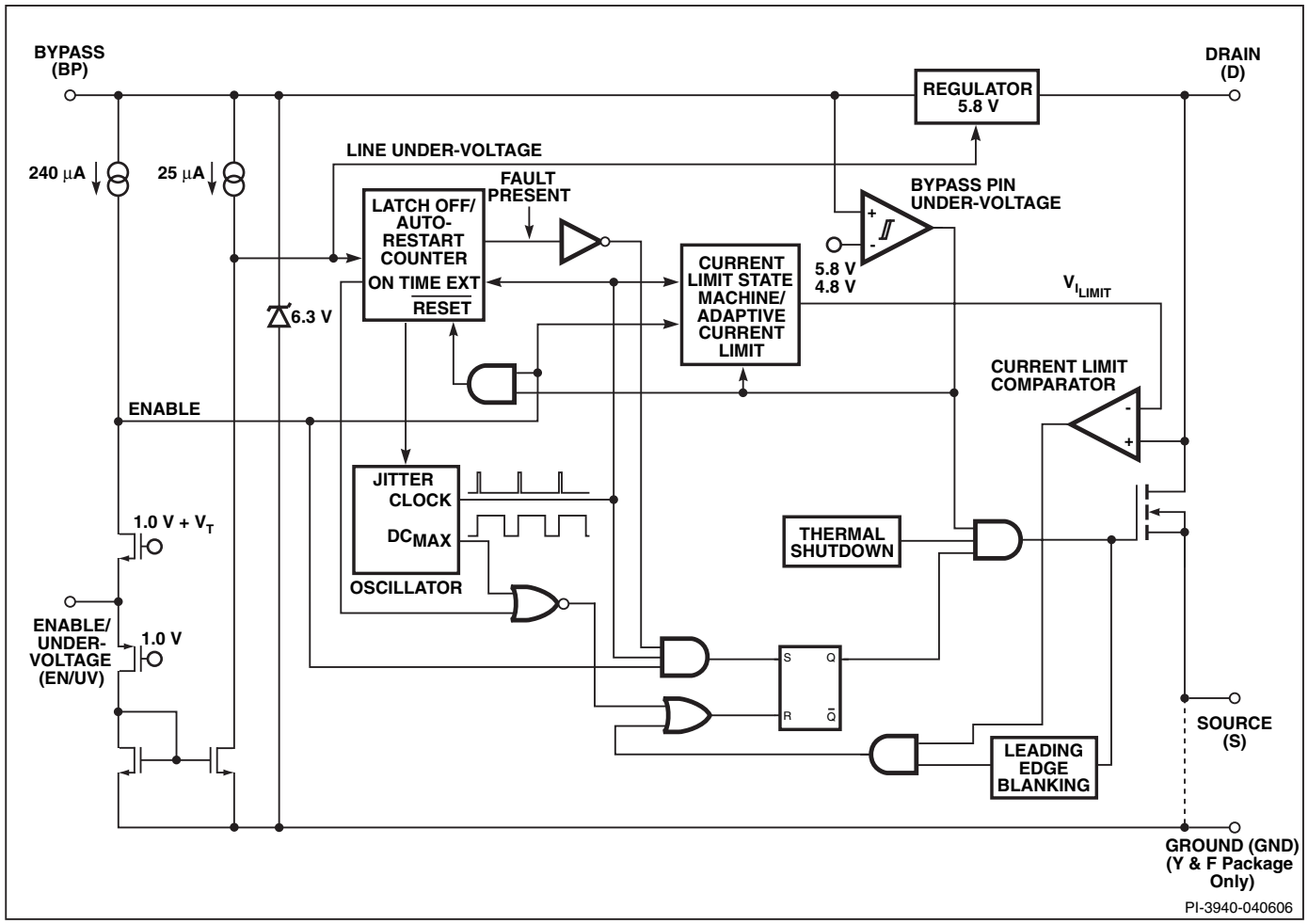

Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
The power MOSFET drain connection provides internal operating current for both startup and steady-state operation.

BYPASS (BP) Pin:
A 0.33 µF external bypass capacitor for the internally generated 5.8 V supply is connected to this pin. In typical applications, this pin must be externally supplied via a bias winding.

ENABLE/UNDER-VOLTAGE (EN/UV) Pin:
This pin has dual functions: enable input and line under-voltage sense. During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a current greater than 240 µA is drawn from this pin. This pin may also sense line under-voltage conditions through either an external resistor connected to the DC line voltage or an AC sense circuit.

SOURCE (S) Pin:
This is the MOSFET source connection for high voltage return and control circuit common.

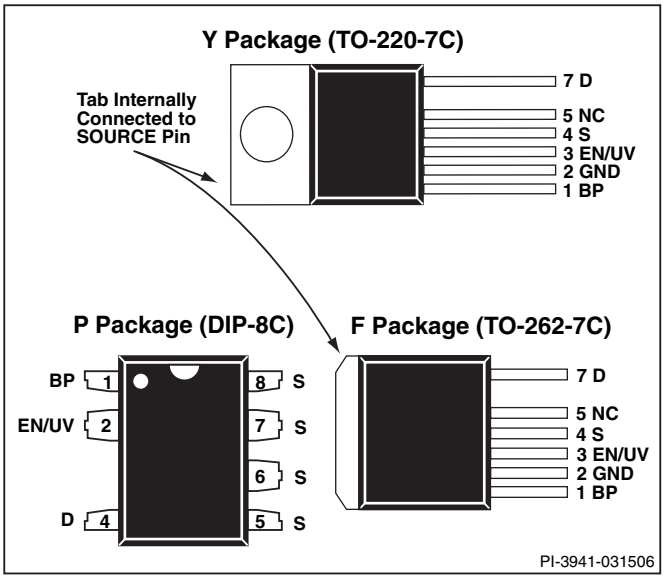

Figure 3. Pin Configuration.

GROUND (GND) Pin (Y or F Package Only):
This is the signal ground for the bypass capacitor and optocoupler.

PeakSwitch Functional Description

PeakSwitch integrates a 700 V power MOSFET switch with a power supply controller on the same die. Unlike conventional pulse width modulation (PWM) controllers, *PeakSwitch* uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit (sense and logic), current-limit state machine, 5.8 V regulator, BYPASS pin under-voltage circuit, over-temperature protection, current limit circuit, and leading edge blanking. *PeakSwitch* incorporates additional circuitry for adaptive current limit, line under-voltage sense, programmable smart line sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. Figure 2 is a functional block diagram of the device's most important features.

Oscillator

The typical oscillator frequency is internally set to an average of 277 kHz. Two signals are generated from the oscillator: the maximum duty cycle (DC_{MAX}) signal and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 16 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1.1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter.

Enable Input and Current-Limit State Machine

The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.0 V. The current through the source follower is limited to 240 µA. When the current out of this pin exceeds 240 µA, a low logic level (disable) is generated at the output of the enable circuit. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

The current-limit state machine reduces the current limit by discrete amounts at light loads when *PeakSwitch* is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density, including the associated audible noise. The state machine monitors the sequence of EN/UV pin voltage levels to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.0 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the *PeakSwitch* operates from the energy stored in the bypass capacitor. The voltage on the DRAIN pin powers the bypass during start-up.

There is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided through an external resistor from the bias winding in normal operation. Powering the *PeakSwitch*

Figure 4. Frequency Jitter.

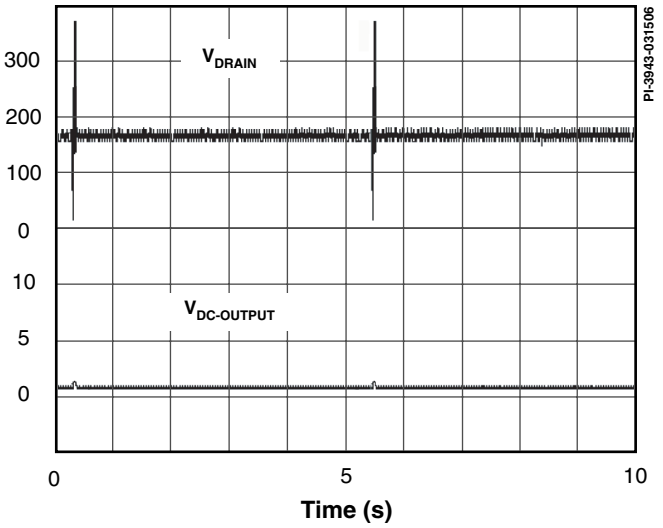

Figure 6. PeakSwitch Auto-Restart Operation.

the line under-voltage sense circuit prevents a restart attempt until the AC input voltage is removed (I_{EN} <25 µA). Then the internal auto-restart latch is reset and the power MOSFET switching will resume once the AC input voltage is applied again (I_{EN} >25 µA). This effectively provides a latching shutdown function with AC reset during such a fault condition.

When a brownout or line sag occurs, output regulation may be lost and the EN/UV pin will receive no feedback (it is pulled low). After 30 ms of no feedback, MOSFET switching is disabled. Since the AC line is abnormally low (I_{EN} <25 µA) MOSFET switching remains disabled until normal line voltage is restored. The power MOSFET switching will resume once the AC input returns to normal (I_{EN} >25 µA). This effectively disables the latching shutdown function during such a condition.

Auto-Restart (UV resistor not present)

In the event of a fault condition such as output overload, output short circuit or an open loop condition, *PeakSwitch* enters into auto-restart operation. An internal counter clocked by the oscillator is reset every time the EN/UV pin is pulled low. When the EN/UV pin receives no feedback for 30 ms, the power MOSFET switching is disabled for 5 seconds (150 ms for the frst auto-restart event). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 6 illustrates auto-restart circuit operation in the presence of an output short circuit.

Adaptive Switching Cycle On-time Extension

Adaptive switching cycle on-time extension keeps the MOSFET on until current limit is reached, instead of terminating after the DC_{MAX} signal goes low. This on-time extension is adaptive because it only occurs after the ENABLE pin has been high for approximately 750 µs, a condition that would arise if the peak output power was required in low line conditions. On-time extension is disabled during the startup of the power supply.

PeakSwitch Operation

PeakSwitch devices operate in the current-limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the highest current limit level and frequency

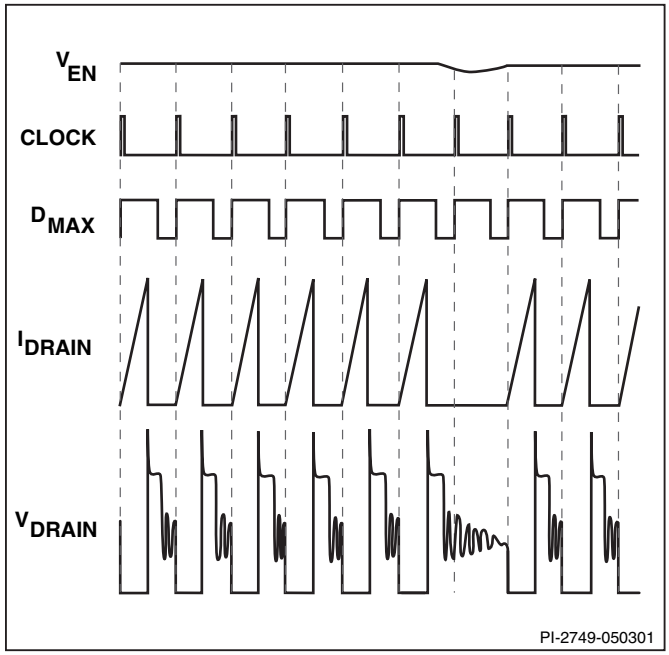

Figure 7. PeakSwitch Operation at Near Maximum Loading.

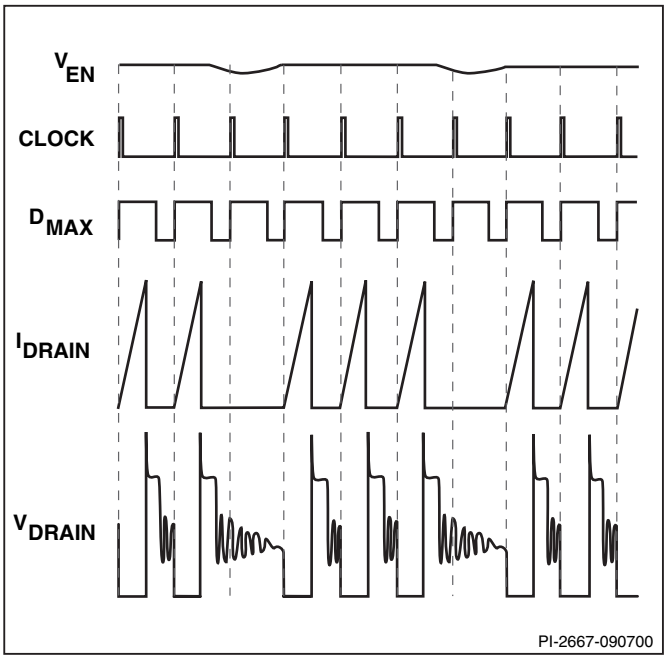

Figure 8. PeakSwitch Operation at Moderately Heavy Loading.

low.
circuit for improved accuracy.

ON/OFF Operation with Current-Limit State Machine

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PI-2377-091100

Figure 9. PeakSwitch Operation at Medium Loading.

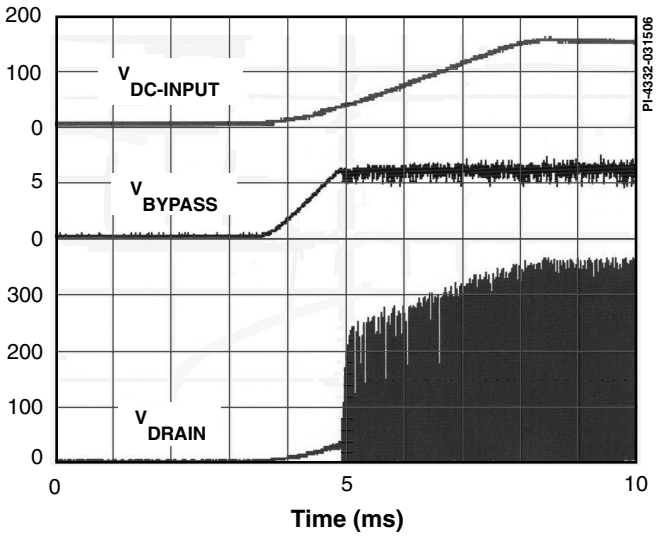


Figure 12. PeakSwitch Power Up Without Optional External UV Resistor Connected to EN/UV Pin.

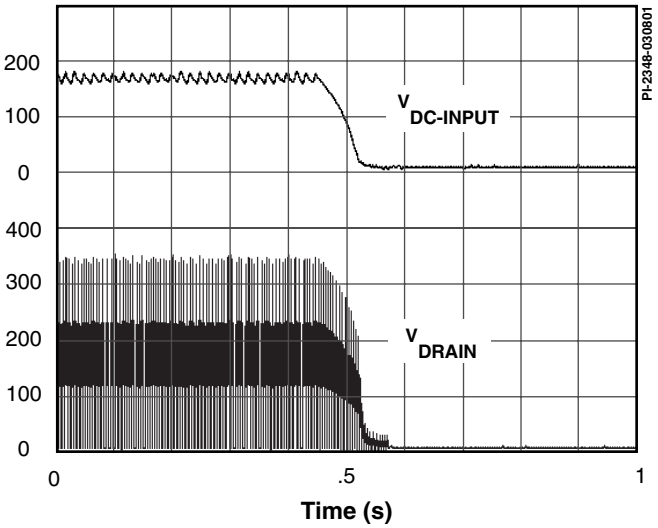


Figure 13. Normal Power Down Timing (Without UV).

At maximum peak load, *PeakSwitch* will conduct during nearly all of its clock cycles (Figure 7). At the rated continuous load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 8). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 9). At very light loads, the current limit will be reduced even further (Figure 10). Only a small percentage of cycles will occur to satisfy the internal power consumption of the power supply at no-load.

The response time of the ON/OFF control scheme is very fast compared to normal PWM control. This provides tight regulation and excellent transient response.

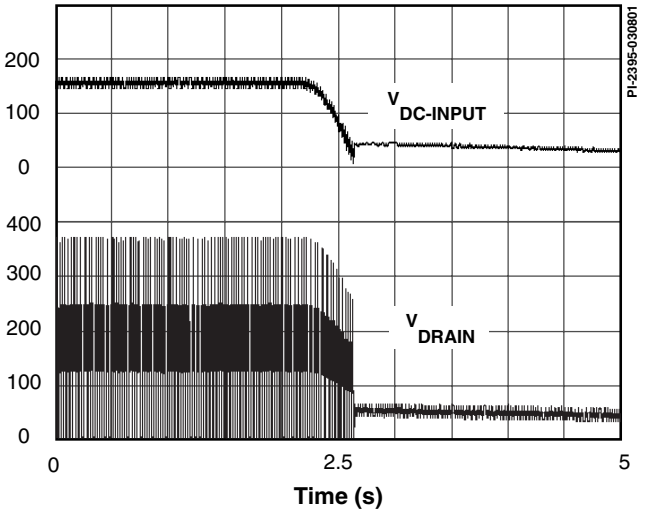


Figure 14. Slow Power Down Timing With Optional External (4 MΩ) UV Resistor Connected to EN/UV Pin.

Power Up/Down

The *PeakSwitch* requires only a 0.33 µF capacitor on the BYPASS pin. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically less than 1.5 ms. Due to the fast nature of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor is connected from the positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power up until the DC line voltage exceeds the threshold (100 V). Figures 11 and 12 show the power up timing waveform in applications with and without an external resistor (4 MΩ) connected to the EN/UV pin.

During power down, when an external resistor is used, the power MOSFET will switch for 30 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the under-voltage function prohibits restart when the line voltage is low.

Figure 13 illustrates a typical power-down timing waveform. Figure 14 illustrates a very slow power-down timing waveform as in standby applications. An external resistor is connected to the EN/UV pin in this case to prevent unwanted restarts.

Current Limit Operation

Each switching cycle is terminated when the DRAIN current reaches the current limit of the *PeakSwitch*. Current limit operation provides good line ripple rejection.

BYPASS Pin Capacitor

The BYPASS pin uses a small 0.33 uF ceramic capacitor for decoupling the internal power supply.

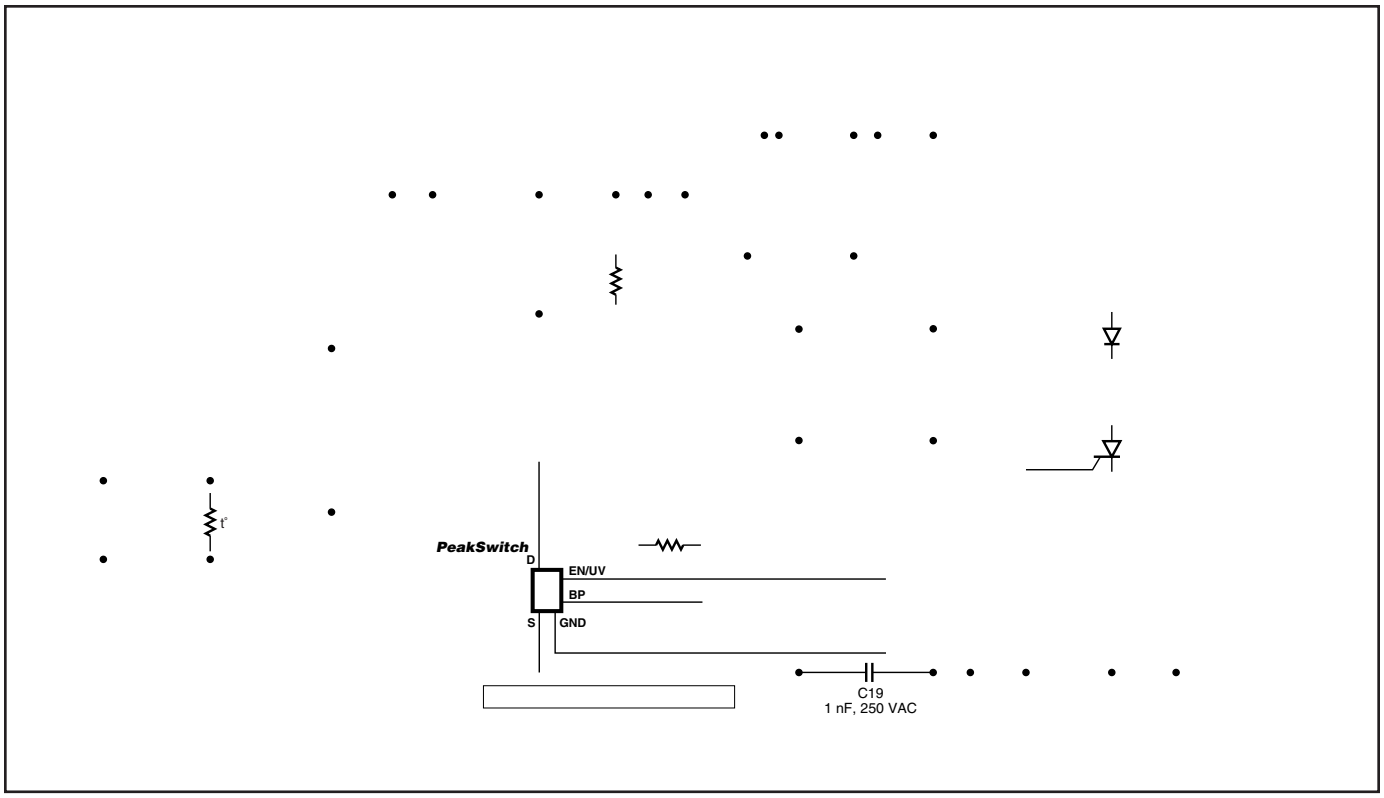


Figure 15. PeakSwitch PKS606Y, 32 W Continuous, 81 W Peak, Universal Input Power Supply.

off the power supply. This protects the load and supply from a continuous fault condition. Removing the AC input resets this condition.

The output voltage is determined by the Zener diode VR2, the voltage drop across R12 and the forward drop of D9 and the LED of optocoupler U2. Resistor R13 provides bias current through D9 and VR2, to ensure that VR2 is operating close to its knee voltage, while R12 sets the overall gain of the feedback loop. Capacitor C15 boosts high frequency loop gain to help distribute the enabled switching cycles and reduce pulse grouping.

When the output voltage exceeds the feedback threshold voltage, current will flow in the optocoupler LED, causing current flow in the transistor of the optocoupler. When this exceeds the ENABLE pin threshold current the next switching cycle is inhibited, as the output voltage falls (below the feedback threshold) a conduction cycle is allowed to occur and by adjusting the number of enabled cycles output regulation is maintained. As the load reduces the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

PeakSwitch device U1 is supplied from an auxillary winding on the transformer which is rectified and filtered by D7 and C6. Resistor R7 provides approximately 2 mA of supply current into the BYPASS pin capacitor C8. During startup or fault conditions when the bias voltage is low, the BYPASS pin is supplied from a high voltage current source within U1, eliminating the need for separate startup components.

Components Q1-2, R9-11, R14, C13, C16, and VR3 form an overvoltage and overcurrent protection circuit. An output overvoltage or overcurrent condition fires SCR Q2, clamping the output voltage and forcing *PeakSwitch* U1 into latching shutdown after 30 ms. The low pass filter formed by R10 and C13 adds a delay to the over-current sense. The shutdown condition can be reset by briefly removing AC power for ~3 seconds (maximum). The latching function within *PeakSwitch* significantly reduces the size of the SCR and output rectifier, D8, as the short circuit current only flows for 50 ms before the supply latches off.

This design meets EN55022 Class B conducted EMI with >10 dB margin even with the output RTN directly connected to earth ground.

Key Application Considerations

PeakSwitch Design Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or single 100/115 VAC with a voltage doubler.
2. Efficiency of 70% for Y/F packaged devices, 75% for P packaged devices at 85-265 VAC, 75% for 230 VAC input all packages
3. Minimum datasheet value of I^2f
4. Transformer primary inductance tolerance of ±10%
5. Reflected output voltage (V_{OR}) of 135 V
6. Voltage only output of 15 V with an ultra fast PN rectifier diode
7. Continuous conduction mode operation with transient K_P* value of 0.25
8. Sufficient heatsinking is provided, either externally (Y/F packages) or through an area of PC board copper (P package) to keep the SOURCE pin or tab temperature at or below 110 °C.
9. Device ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters

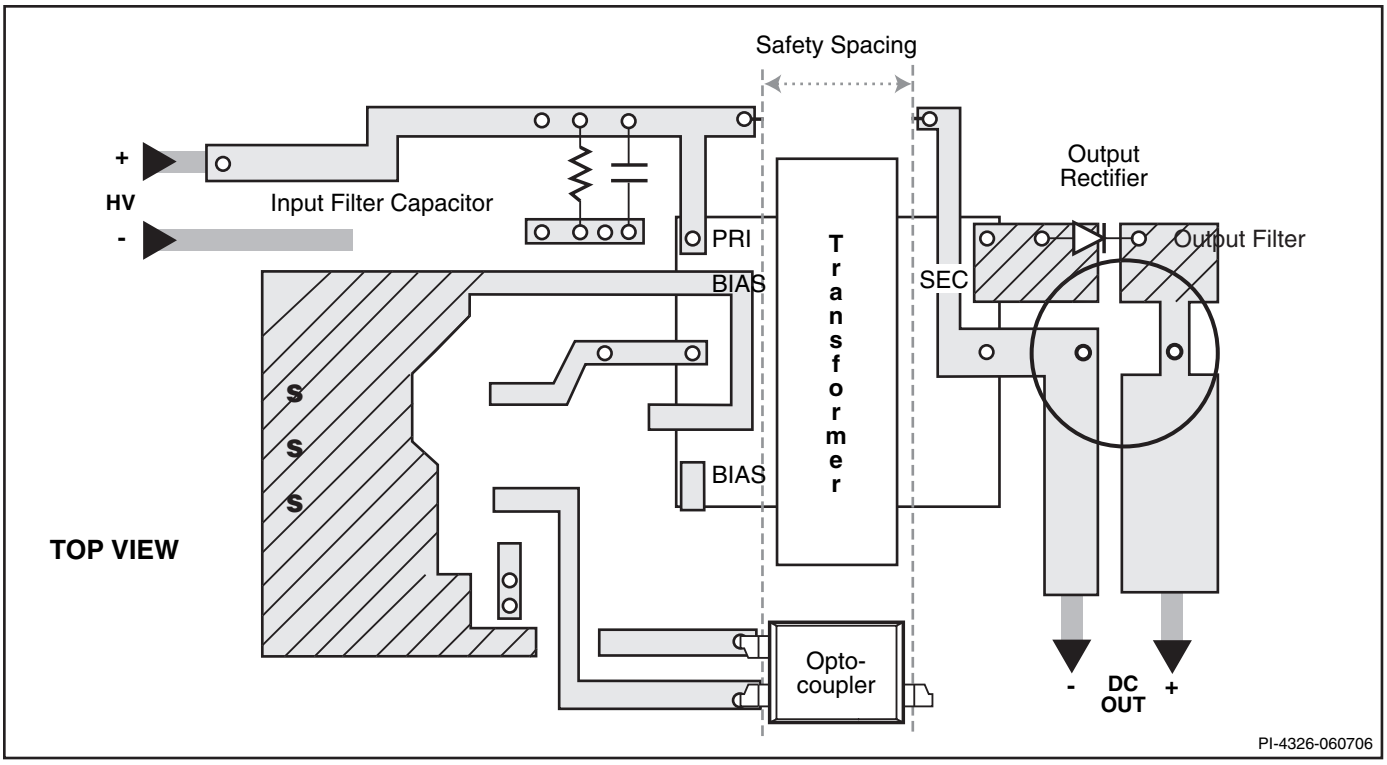
*Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power capability due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This avoids the initial current limit (I_{INIT}) being exceeded at MOSFET turn on.

Peak vs. Continuous Power

PeakSwitch devices have current limit values that allow the specified peak power values in the power table. With sufficient heatsinking, these power levels could be provided continuously, however this may not be practical in many applications. *PeakSwitch* is optimized for use in applications that have short duration, high peak power demand, but a significantly lower continuous or average power. Typical ratios would be $P_{PEAK} \geq 2 \times P_{AVE}$. The high switching frequency of *PeakSwitch* allows a small core size to be selected to deliver the peak power, but the short duration prevents the transformer winding from overheating. As average power increases, it may be necessary to select a larger transformer to allow increased copper area for the windings based on the measured transformer temperature.

The power table provides some guidance between peak power and continuous power in sealed adapters, however specific applications may differ. For example, if the peak power condition is very low duty cycle, say a 2 second peak occurring only at power up to accelerate a hard disk drive, then the transformer's thermal rise is only a function of the continuous power. However, if the peak power occurs every 200 ms for 50 ms then it would need to be considered.

In all cases, the acceptable temperature rise of the *PeakSwitch* and transformer should be verified under worst case ambient and load conditions.



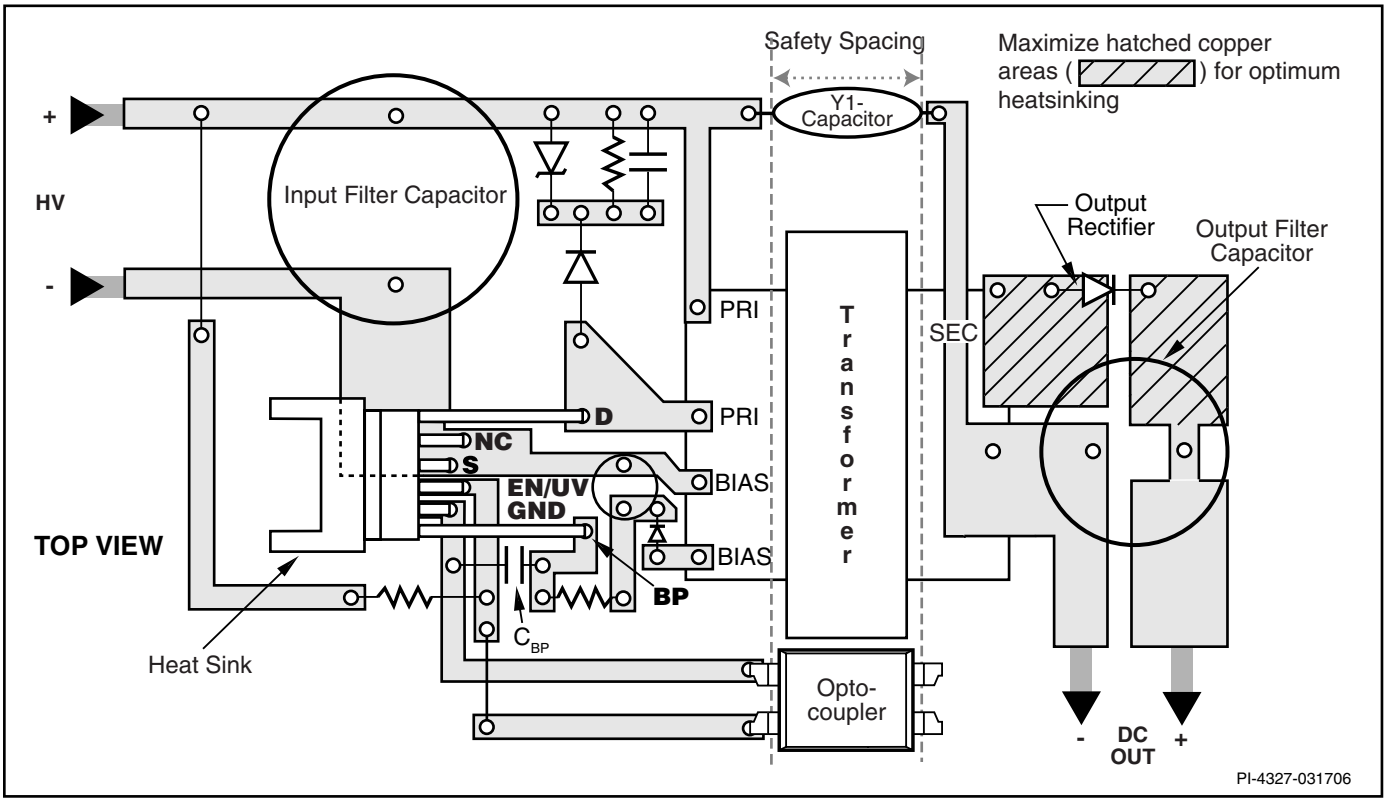


Figure 17. Recommended Layout for PeakSwitch in (a) P and (b) Y/F Packages.

ABSOLUTE MAXIMUM RATINGS[1,4]

DRAIN Voltage .....-0.3 V to 700 V
DRAIN Peak Current: ..... $2 \times I_{LIMIT}$ (Typical)[5]
EN/UV Voltage .....-0.3 V to 9 V
EN/UV Current ....100 mA
BYPASS Voltage .....-0.3 V to 9 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature[2] .....-40 °C to 150 °C
Lead Temperature[3]..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Maximum ratings specified may be applied one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.
5. Peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V. See also Figure 29.

THERMAL IMPEDANCE

Thermal Impedance: Y/F Package:
(θ_{JA})[1] .....80 °C/W
(θ_{JC})[2] .....2 °C/W
P Package:
(θ_{JA}) .....70 °C/W[3]; 60 °C/W[4]
(θ_{JC})[5] ..... 10 °C/W[5]

Notes:
1. Free standing with no heatsink.
2. Measured at the back surface of tab.
3. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
5. Measured on the SOURCE pin close to plastic interface.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	T_J = 25 °C See Figure 4	Average	250	277	304	kHz
			Peak-Peak Jitter		16		
Maximum Duty Cycle	DC_{MAX}	S1 Open		62	65	68	%
EN/UV Pin Turn Off Threshold Current	I_{DIS}			-350	-240	-200	µA
EN/UV Pin Voltage	V_{EN}	$I_{EN/UV}$ = -125 µA		0.4	1.0	1.5	V
		$I_{EN/UV}$ = 25 µA		1.3	2.0	2.7	
DRAIN Supply Current	I_{S1}	$V_{EN/UV}$ = 0 V		350	475	600	µA
	I_{S2}	EN/UV Open (MOSFET Switching) See Note A, B	PKS603	460	570	690	
			PKS604	600	725	870	
			PKS605	700	875	1050	
			PKS606	950	1175	1400	
			PKS607	1160	1430	1700	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C See Note C	PKS603-604	-7.5	-5.0	-2.5	mA
			PKS605-607	-10.0	-6.6	-3.2	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C See Note C	PKS603-604	-4.5	-3.0	-1.5	
			PKS605-607	-6.5	-4.5	-2.5	

Power Coefficient

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)		Min	Typ	Max	Units
CIRCUIT PROTECTION (cont.)							
Initial Current Limit	I_{INIT}	See Figure 21 See Note F		0.75 × $I_{LIMIT(Min)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note F		170	215		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Notes F, G			150		ns
Thermal Shutdown Temperature				135	142	150	°C
Thermal Shutdown Hysteresis					75		°C
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	PKS603 I_D = 81 mA	T_J = 25 °C		7.8	9.0	Ω
			T_J = 100 °C		11.7	13.5	
		PKS604 I_D = 150 mA	T_J = 25 °C		5.2	6.0	
			T_J = 100 °C		7.8	9.0	
		PKS605 I_D = 200 mA	T_J = 25 °C		3.9	4.5	
			T_J = 100 °C		5.8	6.7	
		PKS606 I_D = 300 mA	T_J = 25 °C		2.6	3.0	
			T_J = 100 °C		3.9	4.5	
		PKS607 I_D = 300 mA	T_J = 25 °C		2.0	2.3	
			T_J = 100 °C		3.0	3.5	
OFF-State Drain Leakage Current	I_{DSS1}	V_{BP} = 6.2 V $V_{EN/UV}$ = 0 V V_{DS} = 560 V T_J = 125 °C See Note H				200	µA
	I_{DSS2}	V_{BP} = 6.2 V $V_{EN/UV}$ = 0 V	V_{DS} = 375 V T_J = 50 °C See Note H		15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, See Note I, T_J = 25 °C		700			V
Drain Supply Voltage				50			V
Output EN/UV Delay	$t_{EN/UV}$	See Figure 20				5	µs
Output Disable Setup Time	t_{DST}				0.5		µs

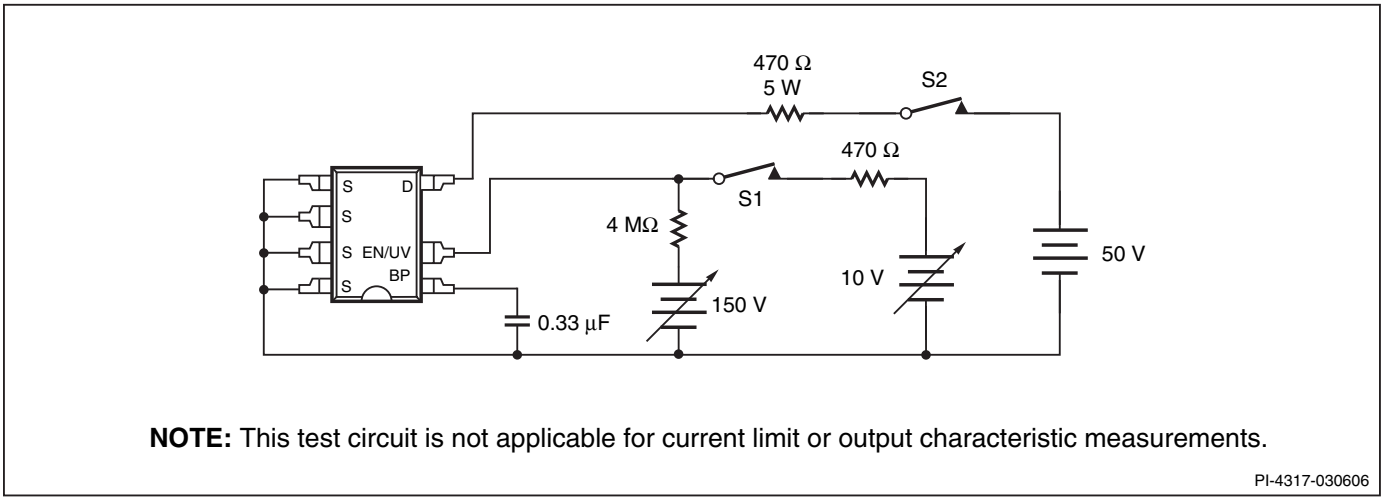


Figure 18. PeakSwitch General Test Circuit.

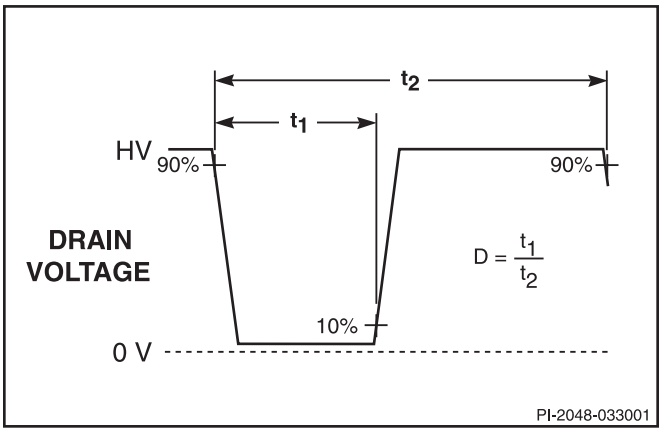


Figure 19. Duty Cycle Measurement.

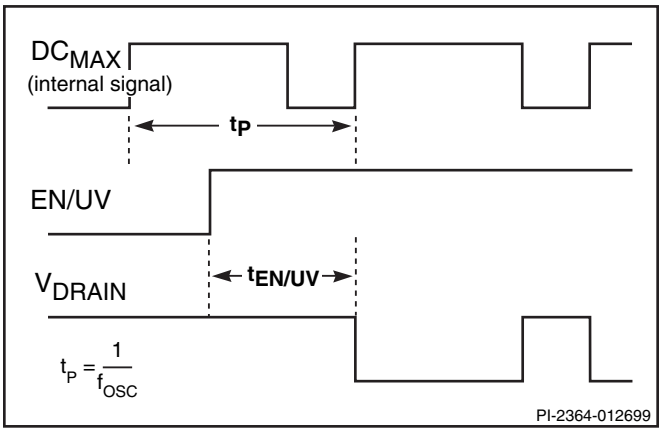


Figure 20. Output Enable Timing.

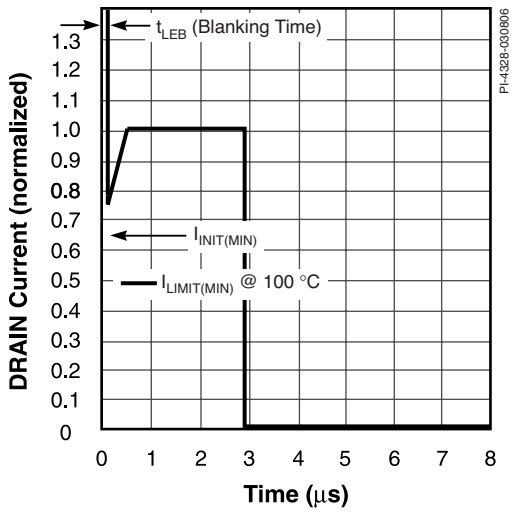


Figure 21. Current Limit Envelope.

Typical Performance Characteristics (cont.)

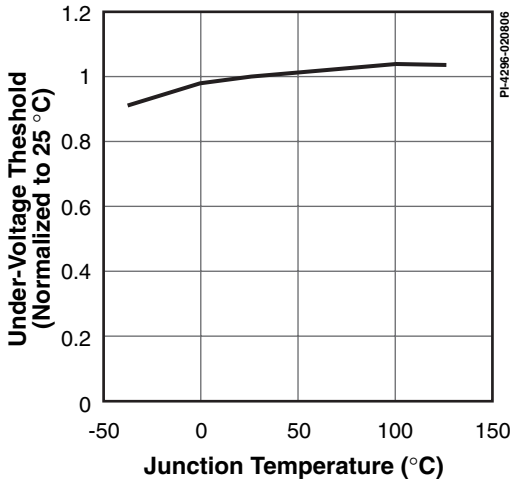


Figure 28. Under-Voltage Threshold vs. Temperature.

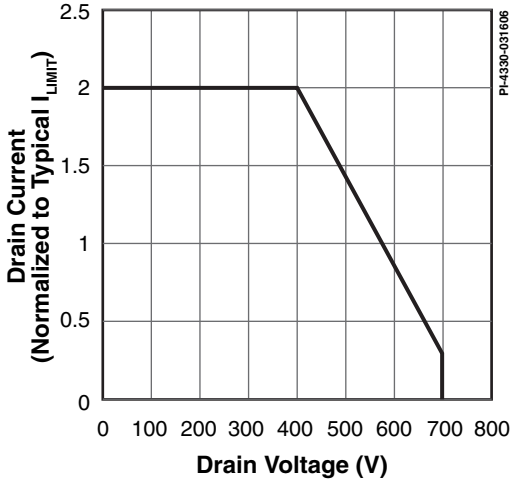
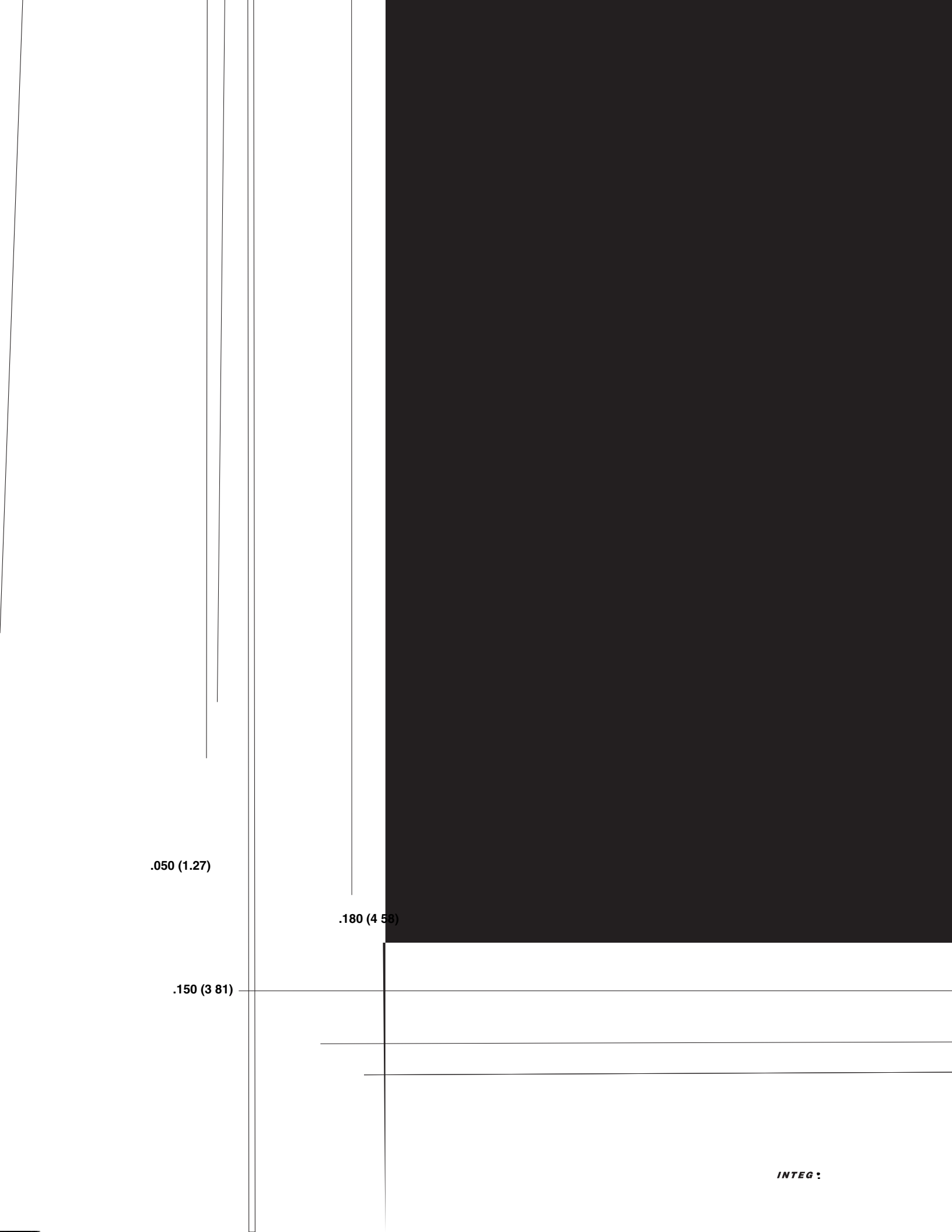
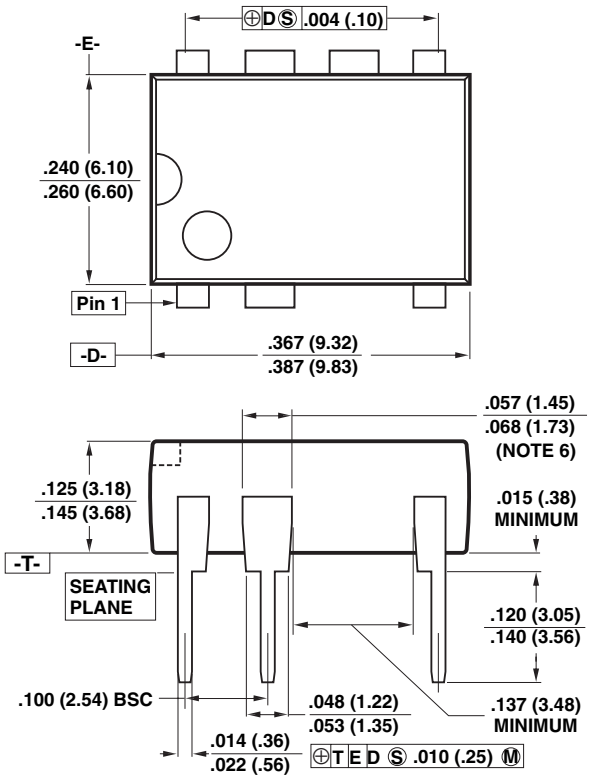


Figure 29. Maximum Allowable Drain Current vs. Drain Voltage.



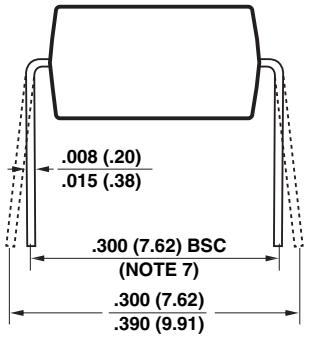
INTEG :

DIP-8C



Notes:

1. **Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.**
2. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.**
5. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
6. **Lead width measured at package body.**
7. **Lead spacing measured with the leads constrained to be perpendicular to plane T.**



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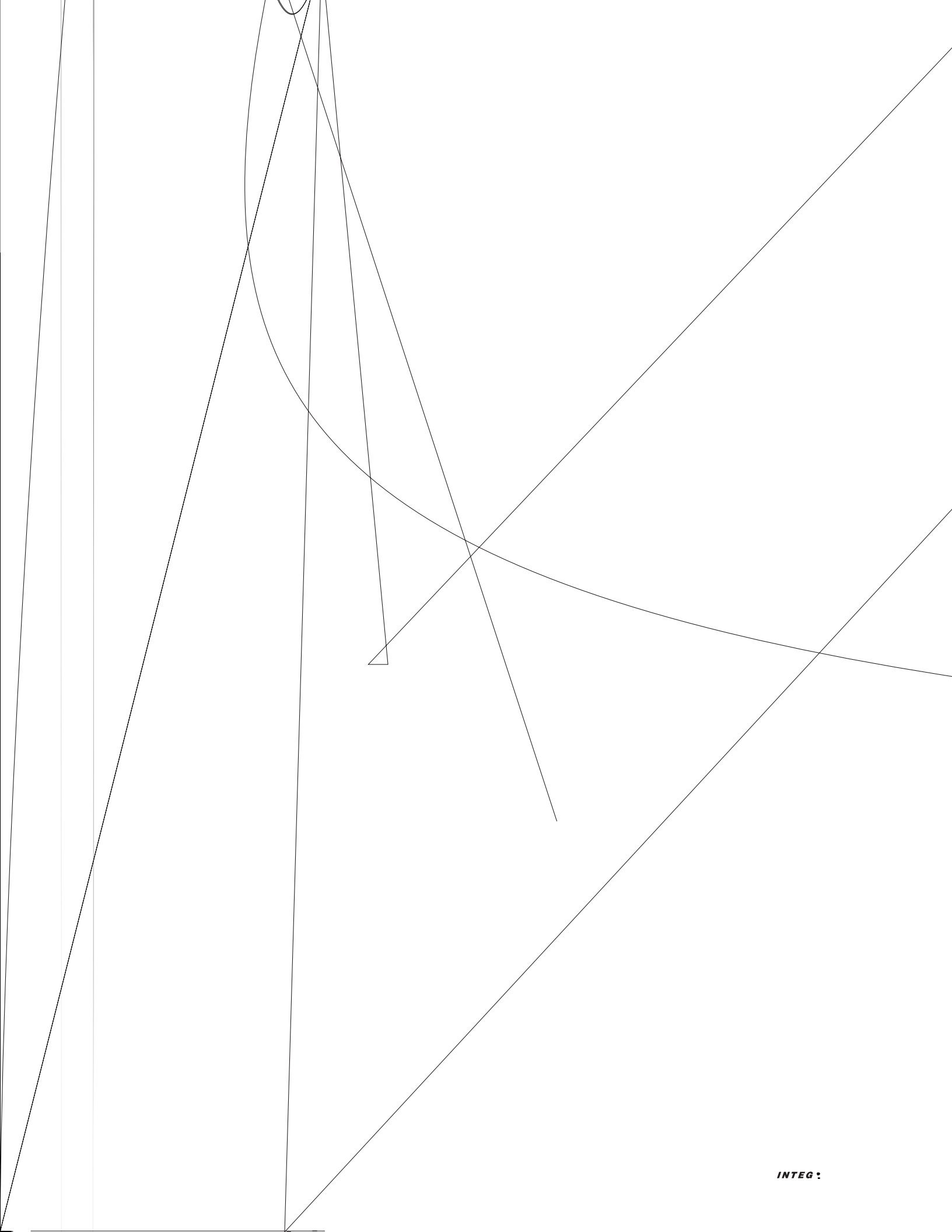

INTEG:

Revision	Notes	Date
F	1) Final Release Data Sheet.	3/06
G	Revised device symbol in Figures 1 and 15 to be consistent with other PI documentation (added second ground connection). Revised layout of Figure 17 (PI-4326).	4/06
H	Revised grounding in Figure 1 to match actual implementation.	6/06
I	Added PKS607.	2/07

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