HEWLETT PACKARD

500 to 1500 Mbps - 850 nm VCSEL Transceiver in Low Cost 1x9 Package Style

942-868

Preliminary Data

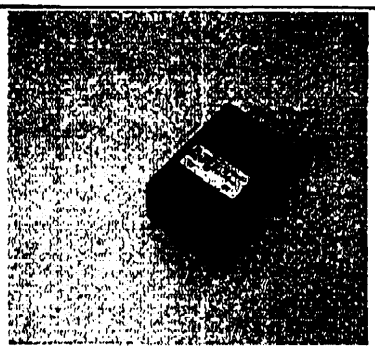
HFBR-5315

Preliminary Product Disclaimer

This preliminary data sheet is provided to assist you in the evaluation of engineering samples of the product which is under development and targeted for release in 1996. Until Hewlett-Packard releases this product for general sales, HP reserves the right to alter prices, specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time.

Features

- Compatible with HDMP-1012/14 integrated transmit/receive ICs
- 850nm Vertical Cavity Surface Emitting Laser (VCSEL) Source Technology
- Industry Standard 1x9 Pin-Out Package Style with Integral Duplex SC Connector
- Class 1 Laser Safety (Certification Pending)
- Single +5 V Power Supply Operation and PECL Logic Interfaces
- Wave Solder and Aqueous Wash Process Compatible
- Designed and Manufactured in an ISO 9001 Certified Facility
- Bus Extension Applications
- High Speed interface for File Servers



Applications

- Switch to Switch Interface

Description

General

The HFBR-5315 transceiver from Hewlett-Packard provide the system designer with products to implement a range of solutions for 500 to 1500 Mbps multimode fiber interfaces.

The overall package for HP transceivers consist of three basic elements; two optical subassemblies, an electrical subassembly, and the housing which incorporates a duplex SC connector interface.

Transmitter Section

The transmitter section consists of an 850 nm VCSEL in an optical subassembly (OSA), which mates to the fiber cable. The VCSEL OSA is driven by a custom, silicon bipolar IC which converts differential PECL logic signals, ECL referenced to a +5 Volt supply, into an analog Laser Diode drive current.

Eye-Safe Design

The VCSEL driver is designed to be Class 1 eye-safe (CDRH21 CFR(J), IEC 825.1) under a single fault condition. To be eye-safe, only one of two results can occur in the event of a single fault. The transmitter must either maintain normal eye-safe operation or the transmitter should be disabled.

There are three key elements to the safety circuitry: a monitor diode, a window detector circuit, and direct control of the laser bias. The window detection circuit monitors the average optical power using the monitor diode. If a fault occurs such that the DC regulation circuit cannot maintain the preset bias conditions within +/- 20%, the transmitter will automatically be disabled. Once this has occured, only a electrical power reset will allow an attempted turn-on of the transmitter.

Receiver Section

The receiver includes a silicon PIN photo-diode mounted together with a custom, silicon-bipolar transimpedance preamplifier IC in an OSA. This OSA is mated to a custom silicon-bipolar circuit that providese post-amplification and quantization.

The custom silicon-bipolar circuit also includes a Signal Detect circuit which provides a PECL logic-high output upon detection of a usable input optical signal level. This single-ended low-power PECL output is designed to drive a standard PECL input through a 50Ω ECL load.

Product Variations Available by Special Request

Hewlett-Packard offers two additional 850nm VCSEL transceivers for the following applications:

* Fibre Channel - HFBR-5303
* Gigabit Ethernet - HFBR-5305

Hewlett-Packard has support ICs for both of these applications. Please contact your local Hewlett-Packard Sales Engineer for more information on these products.

Singlemode 1300nm laser based transceivers will also be provided in the future for use with the HDMP-1012/14 integrated circuits to provide links to several kilometers in singlemode fiber.

Data Line Interconnections

Hewlett-Packard's HFBR-5305 fiber-optic transceiver is designed to directly couple to +5 V PECL signals. The transmitter inputs are internally dc-coupled to the VCSEL driver circuit from the transmitter input pins (pins 7, 8). There is no internal, capacitively-coupled 50 Ohm termination resistance within the transmitter input section. The transmitter driver circuit for the VCSEL light source is a dc-coupled circuit as well which regulates the output optical power. This regulated light output will maintain a constant output optical power provided the data pattern is reasonably balanced in duty factor. If the data duty factor has long, continuous state times (low or high data duty factor), then the output optical power will gradually change its average output optical power level to the nominal value of -7 dBm avg. As for the receiver section, it is internally ac-coupled between the pre-amplifier and the post-amplifier stages. The actual Data and Data-bar outputs of the post-amplifier are dc-coupled, without any internal capacitive coupling, to their respective output pins (pins 2, 3). Signal Detect is a single-ended, +5 V PECL output signal that is dc-coupled to pin 4 of the module. Signal Detect should not be ac-coupled externally to the follow-on circuits because of its infrequent state changes. Caution should be taken to account for the proper interconnection between the supporting Physical Layer integrated circuits and this HFBR-5305 transceiver. Figure 3a illustrates a recommended interface circuit for interconnecting to a +5 Vdc PECL device. Figure 3b illustrates a recommended test interface circuit for interconnecting to test equipment or to logic devices that are not +5 V PECL logic components. Some fiber-optic transceiver suppliers' modules include internal capacitors, with or without 50 Ohm termination, to couple their Data and Data-bar lines to the I/O pins of their module. When designing to use these type of transceivers along with Hewlett-Packard transceivers, it is important that the interface circuit can accomodate either internal or external capacitive coupling with 50 Ohm termination components for proper operation of both transceiver designs. The internal dc-coupled design of the HFBR-5315 I/O connections was done to provide the designer with the most flexibility for interfacing to various types of circuits.

Regulatory Compliance

See the Regulatory Compliance Table for the targeted typical and measured performance for these transceivers.

The overall equipment design will determine the level it is able to be certified to. These transceiver performance targets are offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)
There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The targeted performance has been shown to provide adequate performance in typical industry production environments.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever system-level ESD test criteria that the equipment is intended to meet. The targeted performance is more robust than typical industry equipment requirements of today.

Electromagnetic Interference (EMI)
Most equipment designs utilizing these high-speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

These transceivers, with their shielded design, are targeted to perform to the limits listed in the table below to assist the designer in the management of the overall equipment EMI performance.

Immunity
Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Eye Safety
These 850 nm VCSEL-based transceivers provide Class 1 eye safety by design. Hewlett-Packard has tested the current transceiver design for compliance with the requirements listed below under normal operating conditions and will test for compliance under fault conditions when the product design is completed. HP will obtain certification from outside test facilities for eye safety.

This performance will enable the transceivers to be used without concern for eye safety in the same way that LED-based transceivers are used today.

Regulatory Compliance

Feature	Test Method	Targeted Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 1 (>750 Volts)
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	TBD
Electromagnetic Interference (EMI)	FCC Class A CENELEC EN55022 Class A (CISPR 22A) VCCI Class 1	TBD
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 3 V/m field swept from 10 to 450 MHz applied to the transceiver without a chassis enclosure
Eye Safety	FDA CDRH 21-CFR 1040 Class 1 IEC 825 Issue 1 1993:11 Class 1 CENELEC EN60825 Class 1	Compliant per Hewlett-Packard Testing for all three requirements under normal operating conditions. Fault condition testing pending completion of product development.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D			1.6	V	[1]
Output Current	I_o			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Relative Humidity	RH	5		95	%	
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Rejection	PSR		50		mV_{P-P}	
Transmitter Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	[2]
Transmitter Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	[3]
Transmitter Differential Input Voltage	V_D	0.3		1.6	V	
Data Output Load	R_{DL}	50			Ω	[4]
Signal Detect Output Load	R_{SDL}	50			Ω	[5]

Process Compatibility

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Hand Lead-Soldering Temperature / Time	T_{SOLD}/ t_{SOLD}			260/10	°C/ sec.	
Wave Soldering and Aqueous Wash	T_{SOLD}/ t_{SOLD}			260/10	°C/ sec.	

[1] This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the input circuit.

[2] Compatible with 10K, 10KH and 100K ECL and PECL output signals.

[3] Compatible with 10K, 10KH and 100K ECL and PECL output signals.

[4] The outputs are terminated to Vcc - 2 V.

[5] The output is terminated to ground.

Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCT}		85	120	mA	
Power Dissipation	P_{DIST}		0.43	0.63	W	
Data Input Current - Low	I_{IL}	-350	0		µA	
Data Input Current - High	I_{IH}		16	350	µA	

Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCR}		100	120	mA	
Power Dissipation	P_{DISR}		0.31	0.43	W	[6]
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.950		-1.620	V	[7]
Data Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.740	V	[8]
Data Output Rise Time	t_r	0.2	0.3	0.50	ns	[9]
Data Output Fall Time	t_f	0.2	0.3	0.50	ns	[10]
Signal Detect Output Voltage - Low (De-Asserted)	V_{OL} - V_{CC}	-1.950		-1.620	V	[11]
Signal Detect Output Voltage - High (Asserted)	V_{OH} - V_{CC}	-1.045		-0.740	V	[12]
Signal Detect Assert Time (off-to-on)	t_{SDA}		30	100	µs	[13]
Signal Detect Deassert Time (on-to-off)	t_{SDD}		100	350	µs	[14]

[6] Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of Vcc and Icc minus the sum of the products of the output voltages and currents.

[7] These outputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.

[8] These outputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.

[9] These are 20%-80% values.

[10] These are 20%-80% values.

[11] This output is compatible with 10K, 10KH and 100K ECL and PECL inputs.

[12] This output is compatible with 10K, 10KH and 100K ECL and PECL inputs.

[13] The Signal Detect output will change from logic "0" (Low) to "1"(High) within TBD us of a step transition in optical input power from no light condition to -18 dBm avg.

[14] The Signal Detect output will change from logic "1"(High) to "0"(Low) within TBD us of a step transition in optical input power from -16 dBm to no light condition.

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power (EOL) 50/125 µm, NA = 0.20 fiber	P_O	-10		-4	dBm avg.	[15]
Output Optical Power (EOL) 62.5/125 µm, NA = 0.275 fiber	P_O	-10		-4	dBm avg.	[16]
Optical Extinction Ratio		9			dB	
Center Wavelength	λ_C	830	850	860	nm	
Spectral Width - rms	σ			0.85	nm rms	
Optical Rise Time	t_r			0.45	ns	[17]
Optical Fall Time	t_f			0.45	ns	[18]
RIN_{12}				-117	dB/Hz	

Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum	P_{IN}	0		-14	dBm avg.	[19]
Operating Wavelength	λ	770		860	nm	
Return Loss		12			dB	
Signal Detect - Asserted	P_A	P_D + 1.5 dB		-18	dBm avg.	
Signal Detect - Deasserted	P_D	-45			dBm avg.	
Signal Detect - Hysteresis	$P_A - P_D$	1.5			dB	

[15] The maximum Optical Output Power complies with applicable laser eye safety standards.

[16] The maximum Optical Output Power complies with applicable laser eye safety standards.

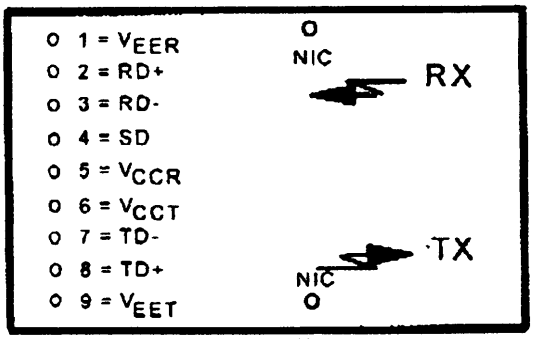
[17] These are 10%-90% values.

[18] These are 10%-90% values.

[19] The sensitivity is provided at a BER of 1 x 10^{-12} with PRBS 2^{10} -1 test data pattern at center of baud interval.

Table 1. Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board, they are embedded in the non-conductive plastic housing and are not tied to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RD+	Receiver Data Out See recommended circuit schematic.
3	RD-	Receiver Data Out Bar See recommended circuit schematic.
4	SD	Signal Detect Normal input optical power levels to the receiver result in a logic "1" output. Low input optical power levels to the receiver result in a fault condition indication shown by a logic "0" output. Signal Detect is a single-ended,PECL output. SD can be terminated with standard PECL techniques via 50 Ω to V_{CCR}-2V. Alternatively, SD can be loaded with a 270 Ω resistor to V_{EER} to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output is used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply Provide +5V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide +5V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD-	Transmitter Data In Bar See recommended circuit schematic.
8	TD+	Transmitter Data In See recommended circuit schematic.
9	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.



TOP VIEW

NIC = No Internal Connection

Figure 1. Pin-Out

Figure 2. Package Outline Drawing and Pinout

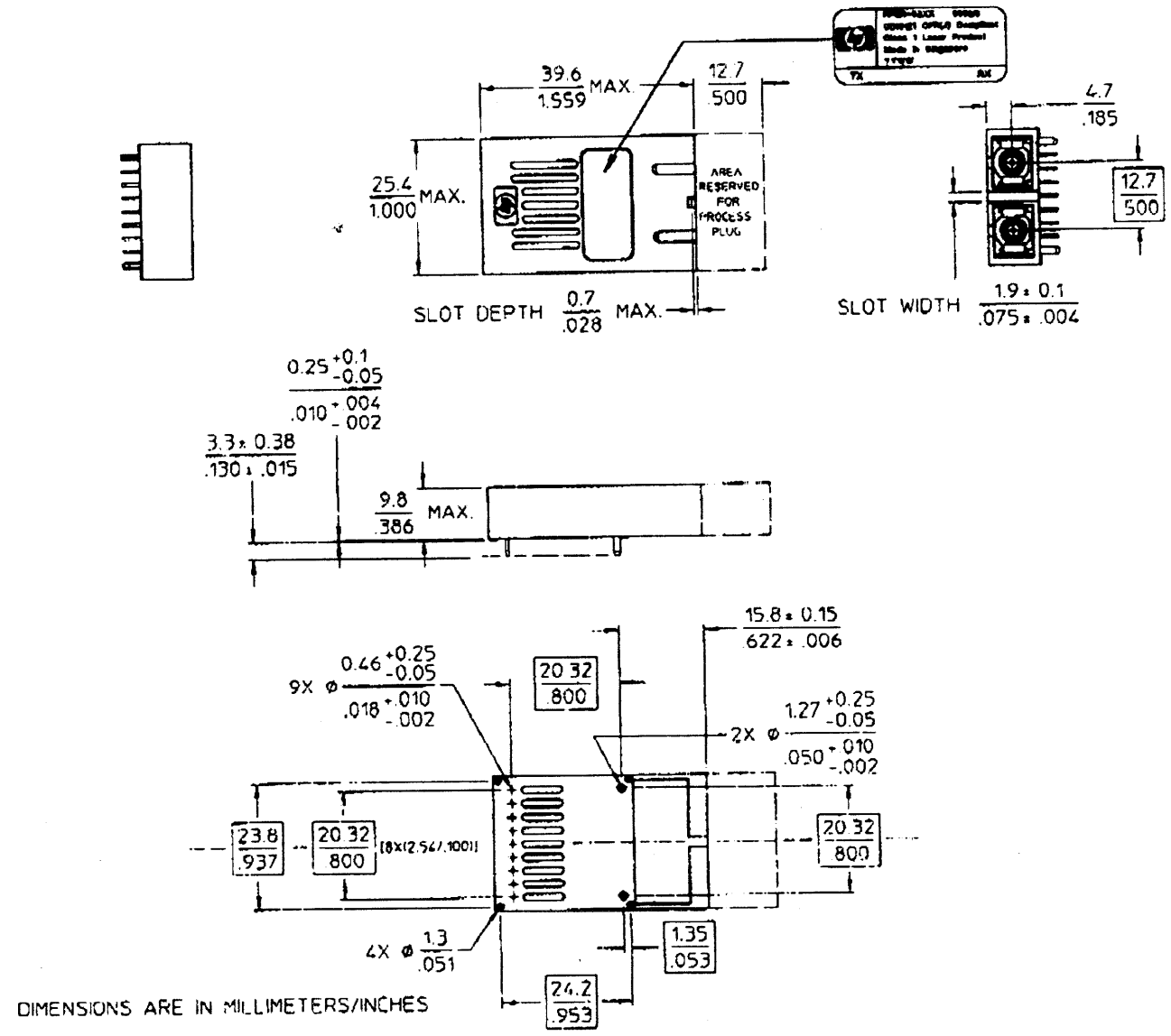
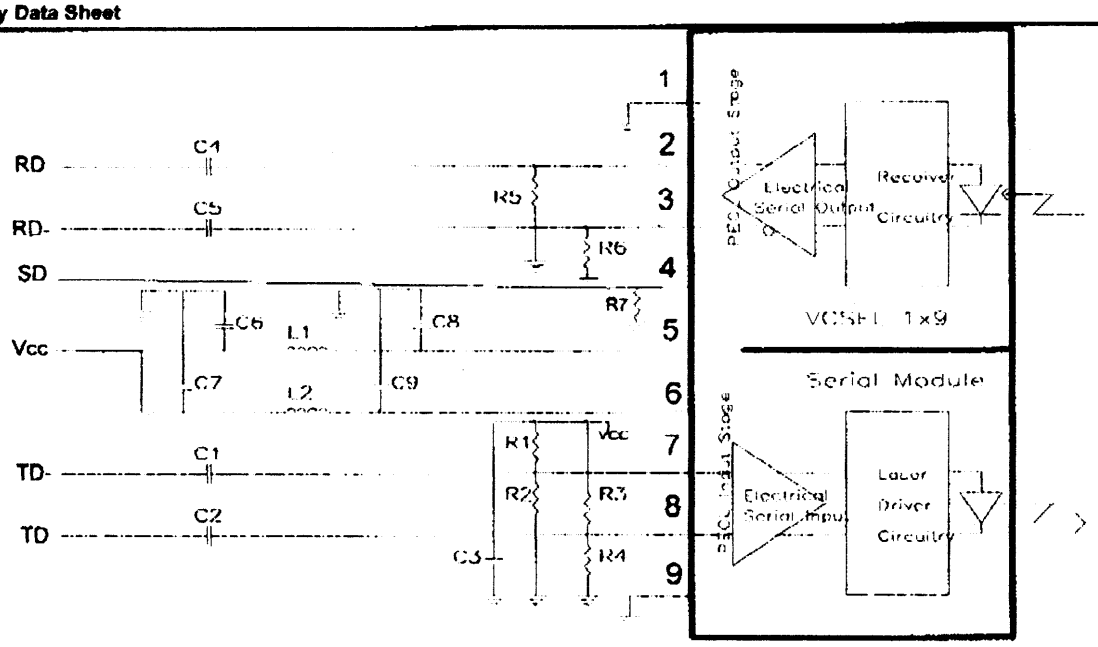


Figure 3. Recommended Circuit Schematic



C1 = C2 = C3 = C4 = C5 = .01 uF
C6 = C7 = C8 = C9 = .01 uF
R1 = R3 = 68 Ohms
R2 = R4 = 192 Ohms R7 = 10 k Ohms
R5 = R6 = 270 Ohms
L1 = L2 = 1 uH

Figure 4 - Recommended Board Layout Hole Pattern