PH 29LE010

638-456.

3.3V-only 1 Megabit Page Mode EEPROM

Features

Single 3.3-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 10 years Data Retention

Low Power Consumption:
- Active Current: 10 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 5 sec. (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 150, 200 and 250 ns
Latched Address and Data
Automatic Write Timing with Internal V_{PP} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-Wide EEPROM Pinouts
Packages Available
- 32-pin TSOP
- 32-Lead PLCC
- 32-pin Plastic DIP

Product Description

The 29LE010 is a 128K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. Breakthroughs in EEPROM cell design and process architecture attain better reliability and manufacturability compared with alternate approaches. The 29LE010 writes with a 3.3-volt-only power supply. Internal erase/program is transparent to the user. The 29LE010 conforms to JEDEC standard pinouts for byte-wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance page write, the 29LE010 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 128K bytes, can be written in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29LE010 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29LE010 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 10 years.

The 29LE010 is best suited for low voltage applications that require reprogrammable nonvolatile storage of program or data memory for laptop computers, notebook computers, cellar telephones, or other low power portable applications. For all system applications, the 29LE010 significantly lowers power consumption, when compared with 5 volt EEPROM or EPROM approaches. In addition, the EEPROM technology makes convenient and economical updating of codes and control programs on-line possible. The 29LE010 improves flexibility while lowering the cost for program and configuration storage applications such as operating systems, BIOS, control programs, software I/O drivers, fonts, or archives.

To meet high density, surface mount requirements, the 29LE010 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is available. The industry standard 32-pin TSOP represents the latest in advanced IC packaging, offering the highest function to area ratio.

Device Operation

The SST page mode EEPROM offers in-circuit electrical erasing and programming capability. The 29LE010 is compatible with industry standard EEPROM pinout and functionality.

Read

The read operation of the 29LE010 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the timing waveforms for further details (Figure 3).

Write

The write operation consists of two steps initiated by forcing CE# and WE# low, and OE# high. Step 1 is the byte-load cycle to a page buffer of the 29LE010. Step 2 is an internally controlled write cycle, for writing the data loaded in

he page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE# whichever occurs last. The data is latched by the rising edge of either CE# or WE# whichever occurs first. The internal write cycle is initiated after the rising edge of either CE# or WE# whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled write cycle timing waveforms and Figure 12 for a flowchart.

The write operation has two functional cycles; the page load cycle and the internal write cycle. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29LE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29LE010 allows the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e. A_7 through A_{16}. Any byte not loaded with user data will be written to FF.

See Figure 4 for the page-write cycle timing waveforms. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 200 µs, the 29LE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 300 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely as long as the host continues to load the device within the byte-load cycle time of 200 µs. The page to be loaded is determined by the page address of the last byte loaded.

Write Operation Status Detection

The 29LE010 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ_7) and Toggle# Bit (DQ_6). The end of write detection mode is enabled after the rising edge of either CE# or WE# whichever occurs first, which initiates internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e. valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29LE010 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data Polling timing waveforms and Figure 13 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e. toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing waveforms and Figure 13 for a flowchart.

Data Protection

The 29LE010 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 15 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5 V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29LE010 provides the JEDEC approved optional software data protection scheme. With this scheme, any

write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is typically used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29LE010 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying the three-byte sequence to the device, in a page-load cycle (Figure 8). The device will then be automatically set into the data protection mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 3 for the specific codes and Figure 8 for the timing waveforms. To set the device to the unprotected mode, a six-byte sequence is required. See Table 3 for specific codes and Figure 9 for the timing waveforms. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends that Software Data Protect always be enabled. See Figure 14 for a flowchart.

The Software Data Protect operation is a global command, affecting the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

3.3-volt-Only Software Chip-Erase

The SST 29LE010 provides a chip-erase mode, which allows the user to clear the memory array to the "1" state. This is useful when the entire device must be quickly erased.

The software chip-erase mode is initiated by issuing the specific six-byte loading sequence, as in the Software Data Protection operation. After the loading cycle, the device enters into an internally timed cycle similar to the write cycle. See Table 4 for specific codes and Figure 10 for the timing waveform and Figure 15 for a flowchart.

Product Identification

The product identification mode identifies the device and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by an external programmer to identify the correct program algorithm for the SST 29LE010. Users may wish to use the software product identification operation to identify the part (i.e., using the device code). For details, see Table 2 for hardware operation or Table 5 for software operation and Figure 15 for a flowchart. The manufacture and device codes are the same for both operations.

Product Identification Table

	BYTE	DATA
Manufacturer Code	0000 H	BF H
Device Code	0001 H	07 H

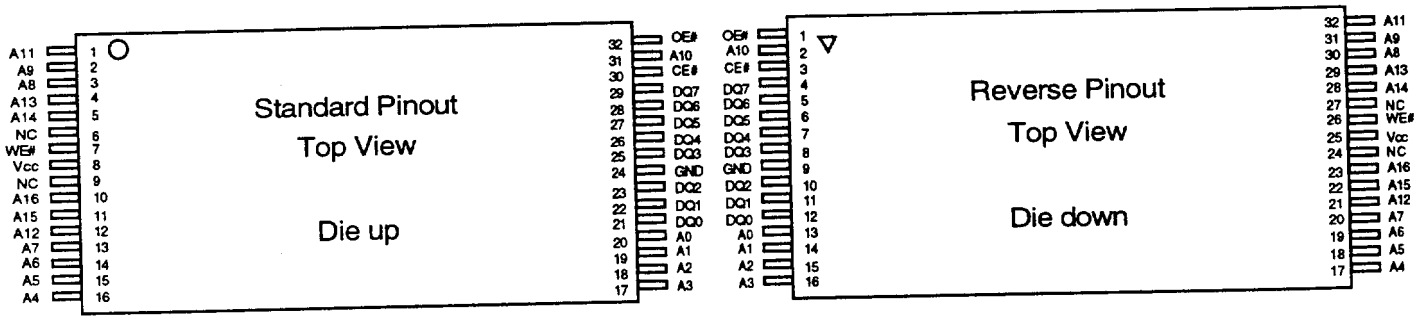


Figure 1A: Standard and Reverse Pin Assignments for 32-pin TSOP Packages.

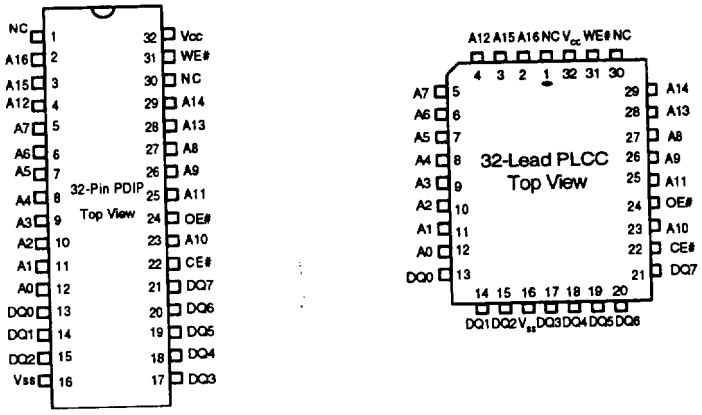


Figure 1B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCC.

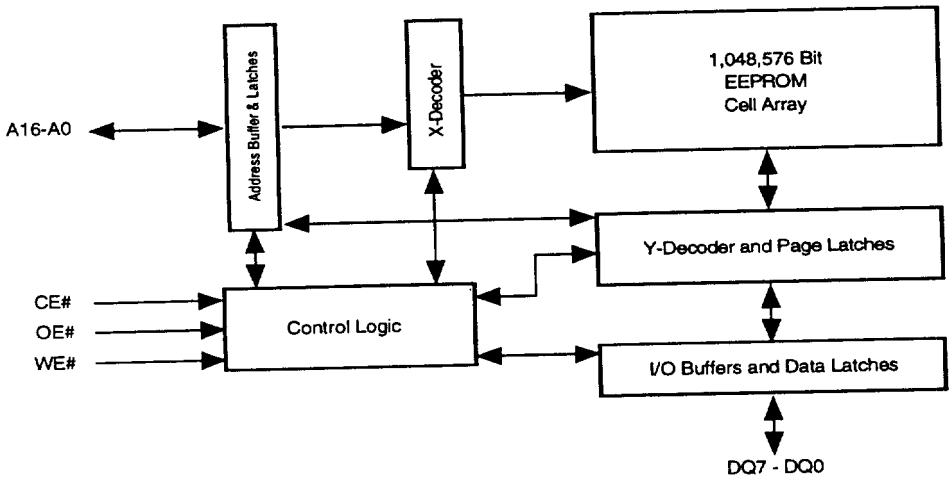


Figure 2: Functional Block Diagram of 29LE010

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{16} - A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6 - A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7 - DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low. CE# high puts the device to standby.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operation.
V_{CC}	Power Supply	To provide 3.3-volt supply (±0.3V)
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

Table 2: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Product Identification	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{16}-A_1 = V_{IL} A_9 = 12V A_0 = V_{IL}
Hardware Mode				Device Code (07)	A_{16}-A_1 = V_{IL} A_9 = 12V A_0 = V_{IH}
Software Mode					See Table 5
SDP Enable & Disable Mode					See Table 3
Software Chip Erase					See Table 4

Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	1,000 & 10,000	Cycles	MIL-STD 883, Method 1033
T_{DR}[1]	Data Retention	10	Years	MIL-STD 883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1,000	Volts	MIL-STD 883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch-up	100	mA	JEDEC Standard 17

Note: [1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 3: Software Data Protection Command Code

Byte Sequence	To Enable Protection		To Disable Protection	
	Address[1]	Data	Address[1]	Data
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write			5555H	AAH
4 Write			2AAAH	55H
5 Write			5555H	20H

[1] Address format A_{14}-A_0 (Hex)

Table 4: Software Chip-Erase Command Code

Byte Sequence	Address[1]	Data
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

[1] Address format A_{14}-A_0 (Hex)

Table 5: Software Product ID Entry Command Code and Exit Command Code

Byte Sequence	Product ID Entry		Product ID Exit	
	Address	Data	Address	Data
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	F0H
3 Write	5555H	AAH		
4 Write	2AAAH	55H		
5 Write	5555H	60H		

Notes for Software Product ID Command Code:
1. Command Code Address format: A_{14}-A_0 (Hex)
2. With A_{14}-A_1=0;
   SST Manufacturer Code = BFH is read with A_0=0
   29LE010 Device Code = 07H is read with A_0=1
3. The device does not remain in Software Product ID Mode if powered down.
4. Addresses > A_{14} are "Don't Care".

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential	-0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Through Hole Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current[1]	100 mA

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	3.3V±0.3V
Industrial	-40°C to +85°C	3.3V±0.3V

AC Conditions of Test

Input Rise/Fall Time	10 ns
Output Load	1 TTL Gate and C_L=100pf
See Figure 11	

DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{CC}	Power Supply Current Read		12	mA	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open. Address input=V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} = V_{CC} max
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC} = V_{CC} max
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} - 0.3V, V_{CC} = V_{CC} max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{CC}, V_{CC} = V_{CC} max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{CC}, V_{CC} = V_{CC} max
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} max
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} max
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} min
V_{OH}	Output High Voltage	2.4		V	I_{OH} = - 100µA, V_{CC} = V_{CC} min

Note : (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU.READ}$ (1)	Power-up to Read Operation	100	µs
$T_{PU.WRITE}$ (1)	Power-up to Write Operation	5	ms

Capacitance (Ta=25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$ (1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pf
C_{IN} (1)	Input Capacitance	V_{IN} = 0V	6 pf

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Characteristics

Read Cycle Timing Parameters

Symbol	Parameter	29LE010-150		29LE010-200		29LE010-250		Units
		Min	Max	Min	Max	Min	Max	
T_{RC}	Read Cycle Time	150		200		250		ns
T_{CE}	Chip Enable Access Time		150		200		250	ns
T_{AA}	Address Access Time		150		200		250	ns
T_{OE}	Output Enable Access Time		90		100		120	ns
$T_{CLZ(1)}$	CE# Low to Active Output	0		0		0		ns
$T_{OLZ(1)}$	OE# Low to Active Output	0		0		0		ns
$T_{CHZ(1)}$	CE# High to High-Z Output		50		55		60	ns
$T_{OHZ(1)}$	OE# High to High-Z Output		50		55		60	ns
$T_{OH(1)}$	Output Hold from Address Change	0		0		0		ns

Byte / Page-Write Cycle Timing Parameter

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	100		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	150		ns
T_{WP}	WE# Pulse Width	150		ns
T_{DS}	Data Setup Time	100		ns
T_{DH}	Data Hold Time	0		ns
$T_{BLC(1)}$	Byte Load Cycle Time	0.10	100	µs
$T_{BLCO(1)}$	Byte Load Cycle Time-out	200		µs

Note : (1) This parameter is measured only for initial qualification and after the design or the process change that could affect this parameter.

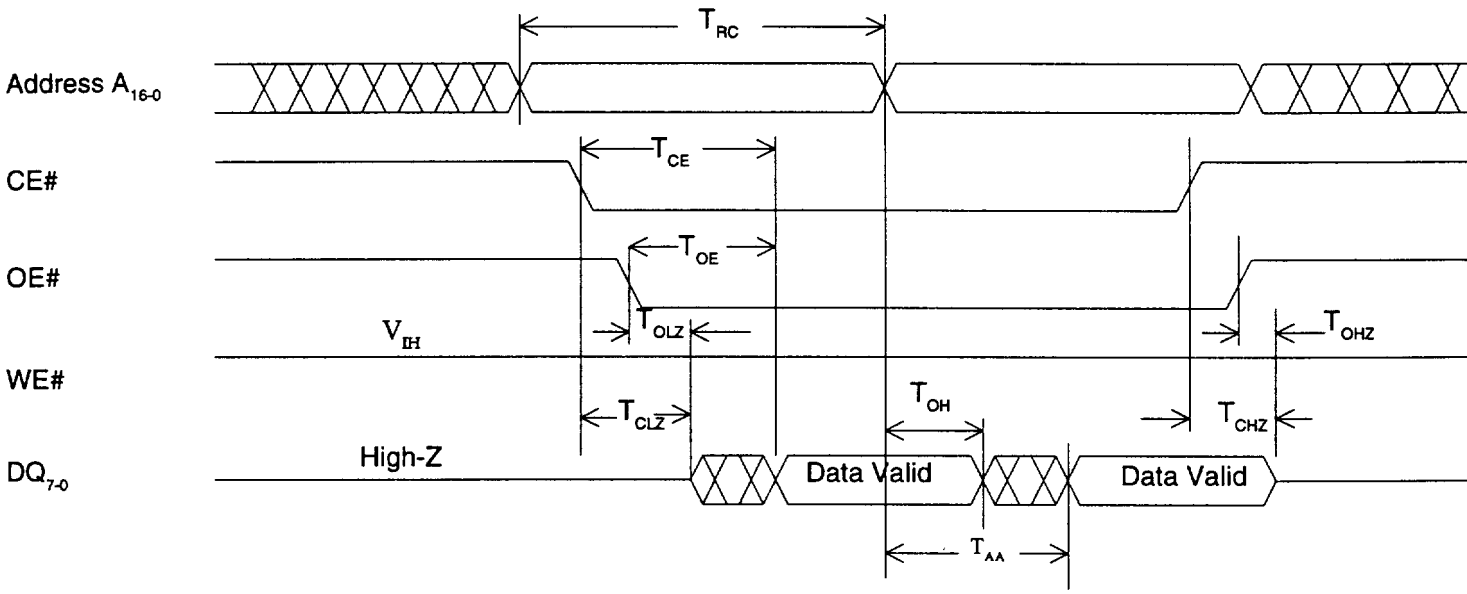


Figure 3: Read Cycle Timing Diagram

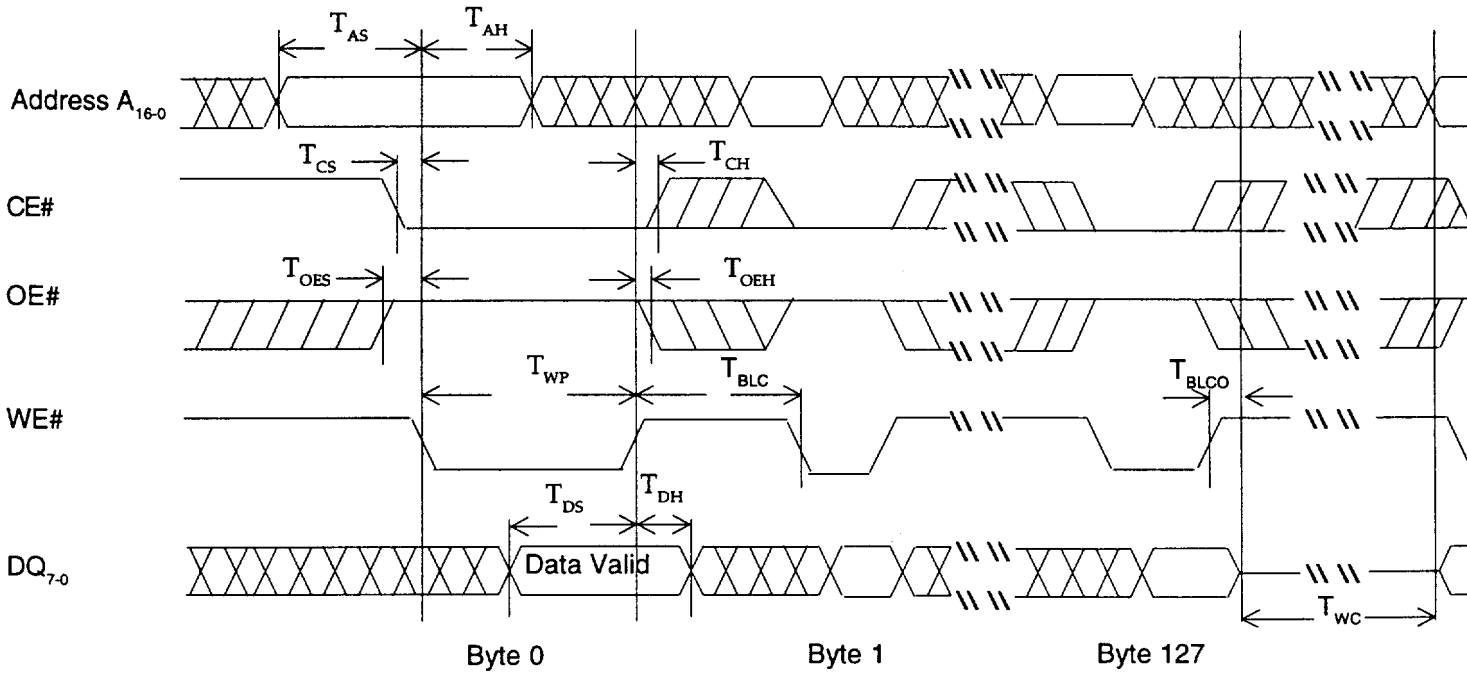


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

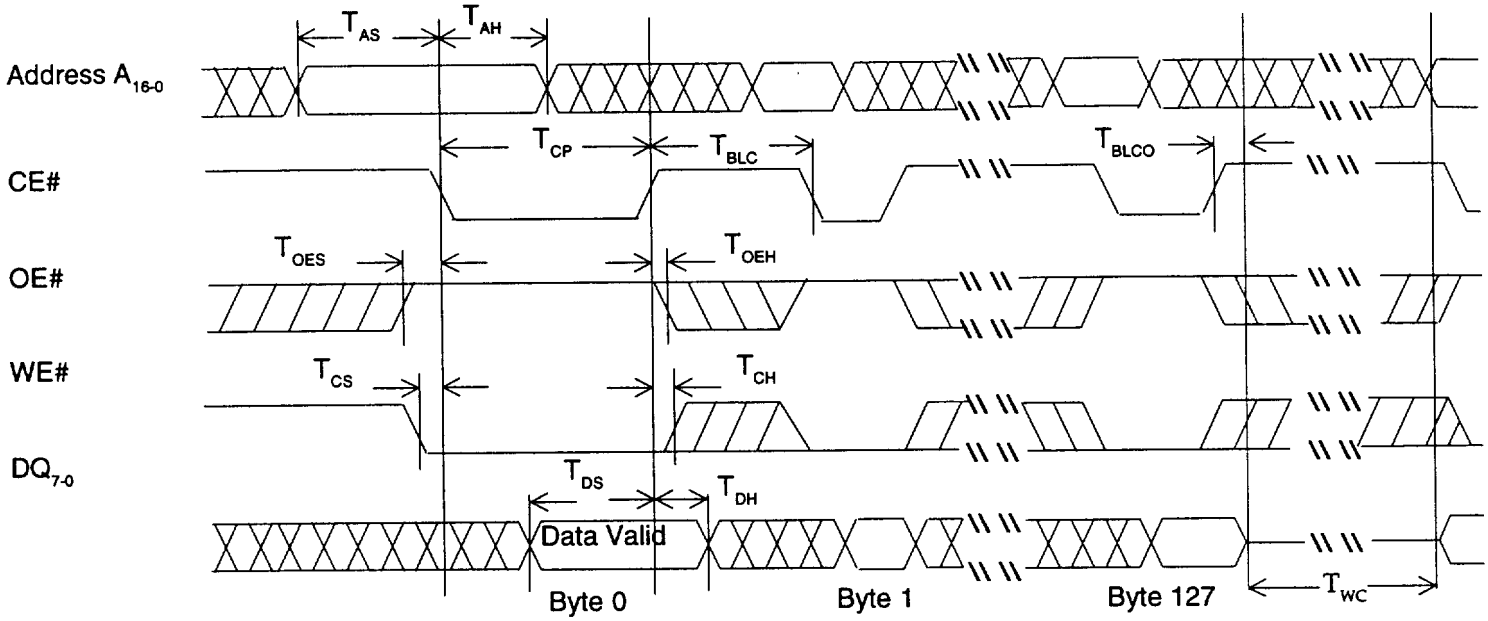


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

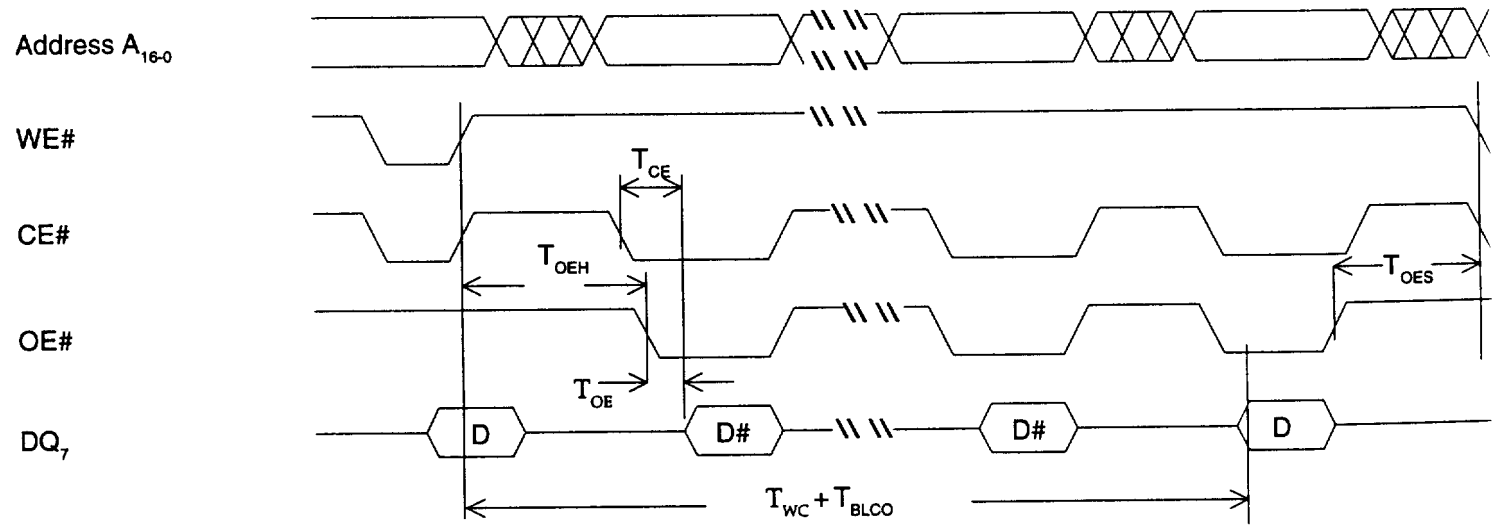


Figure 6: DATA# Polling Timing Diagram

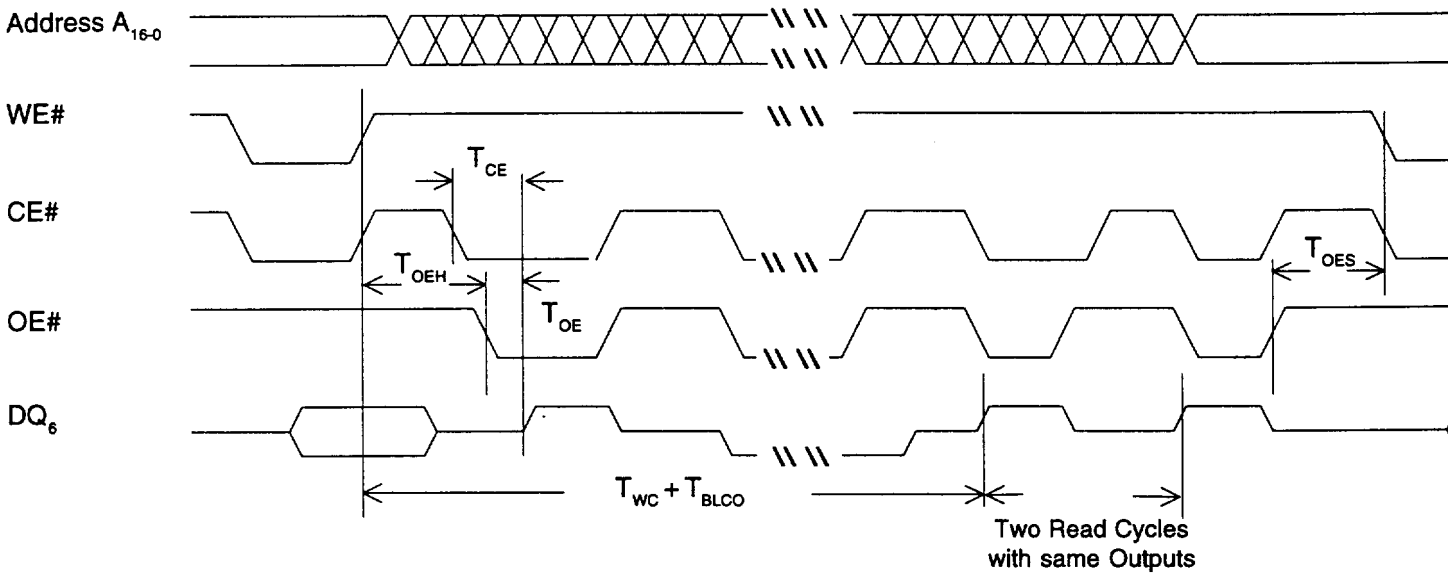
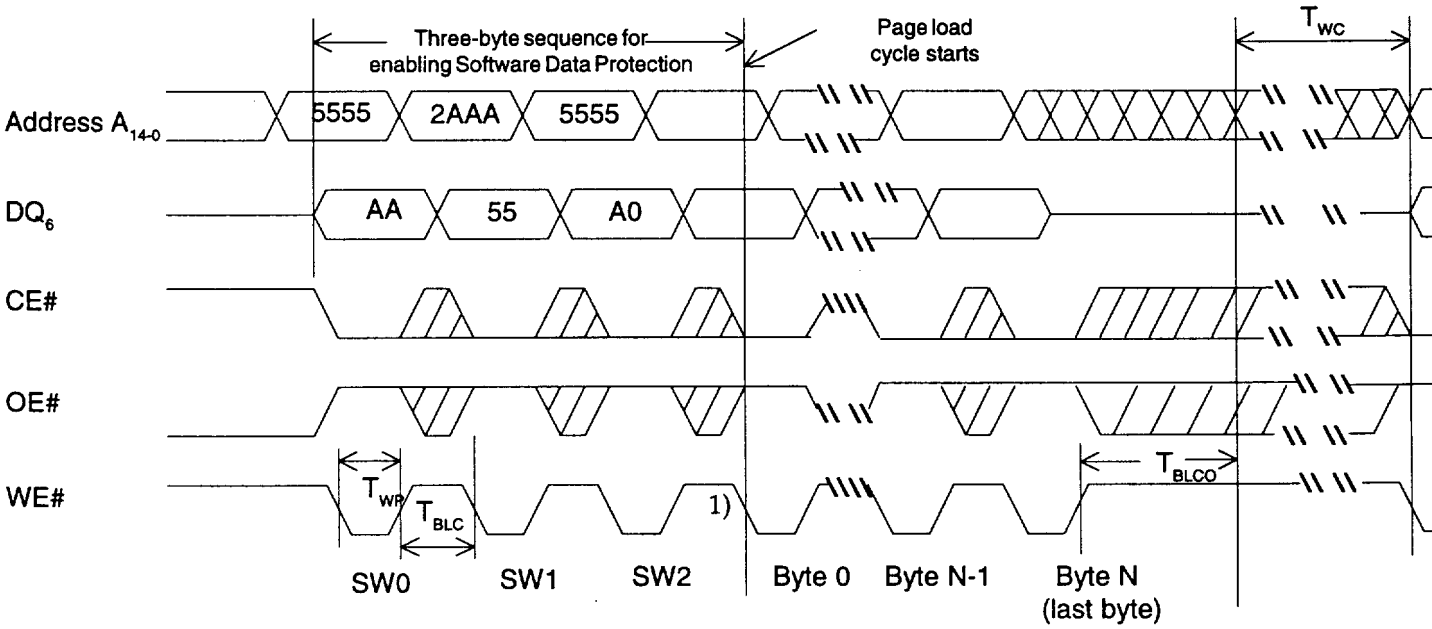


Figure 7: Toggle Bit Timing Diagram



Note 1): The time between enabling Software Data Protect and the page load must be less than T_{BLCO}

Figure 8: Enable Software Data Protection Page Write Timing Diagram

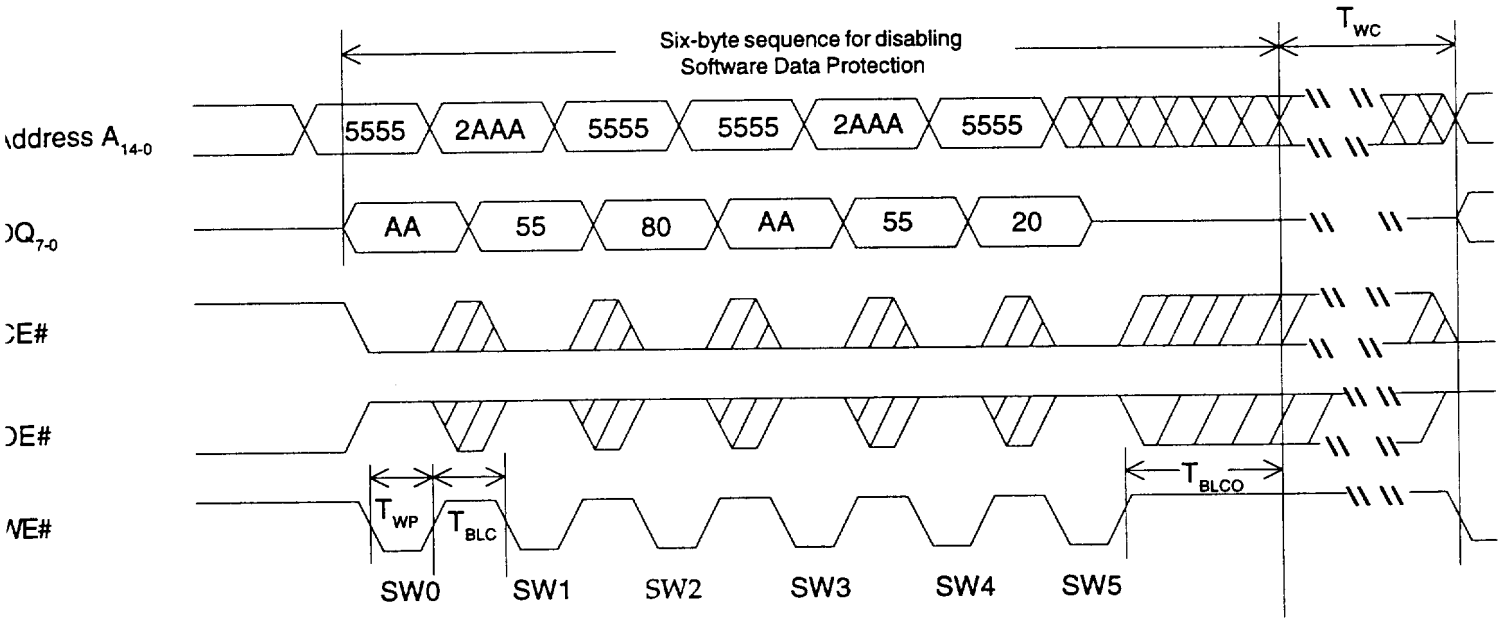


Figure 9: Disable Software Data Protection Timing Diagram

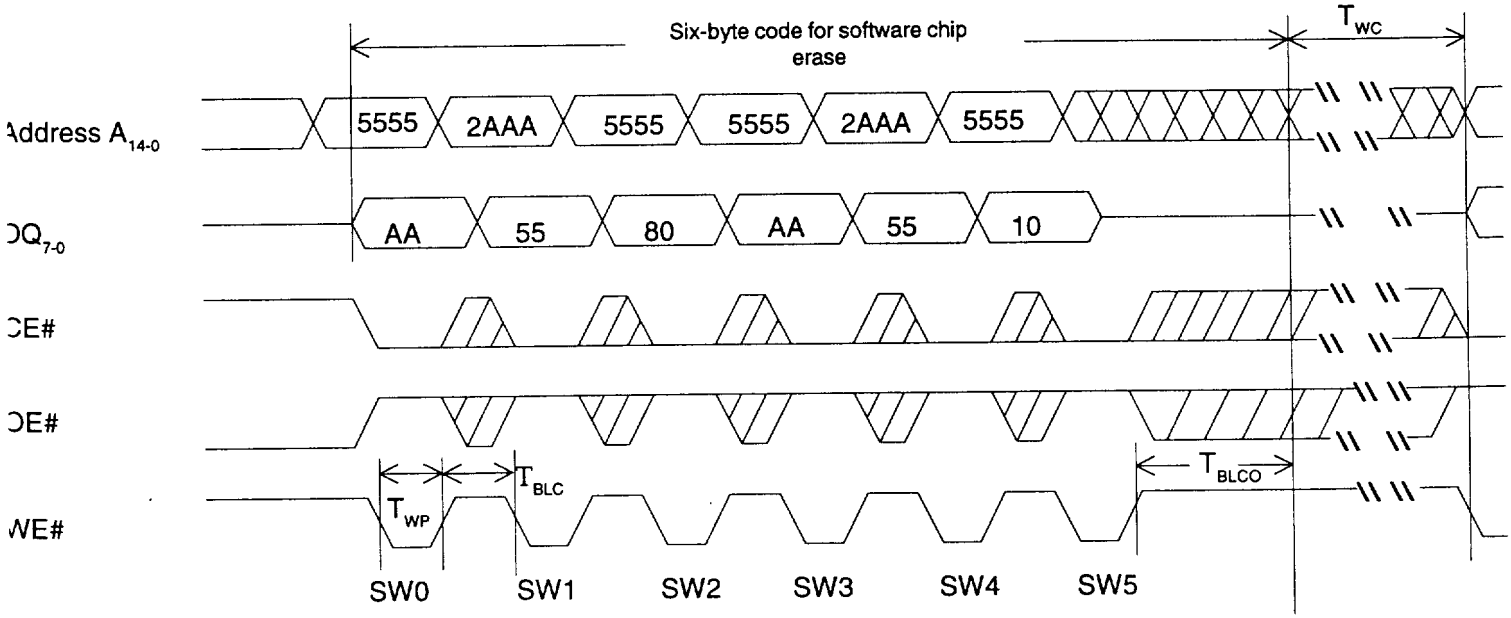
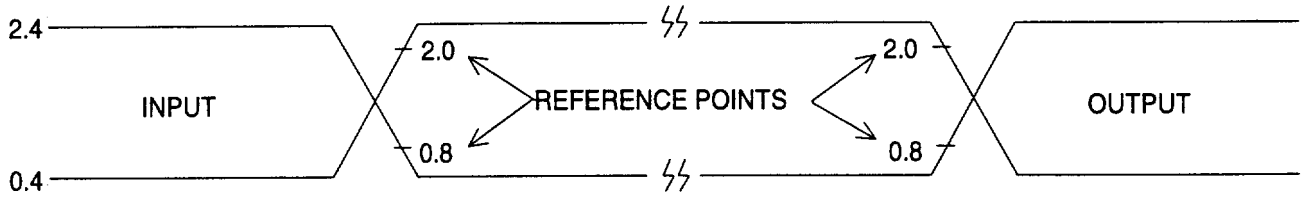


Figure 10: Software Chip Erase Timing Diagram



AC test inputs are driven at V_{OH} ($2.4V_{TTL}$) for a logic "1" and V_{OL} ($0.4V_{TTL}$) for a logic "0". Measurement reference points for inputs and outputs are at V_{IH} ($2.0V_{TTL}$) and V_{IL} ($0.8V_{TTL}$). Input rise and fall times (10% ↔ 90%) are < 10 ns.

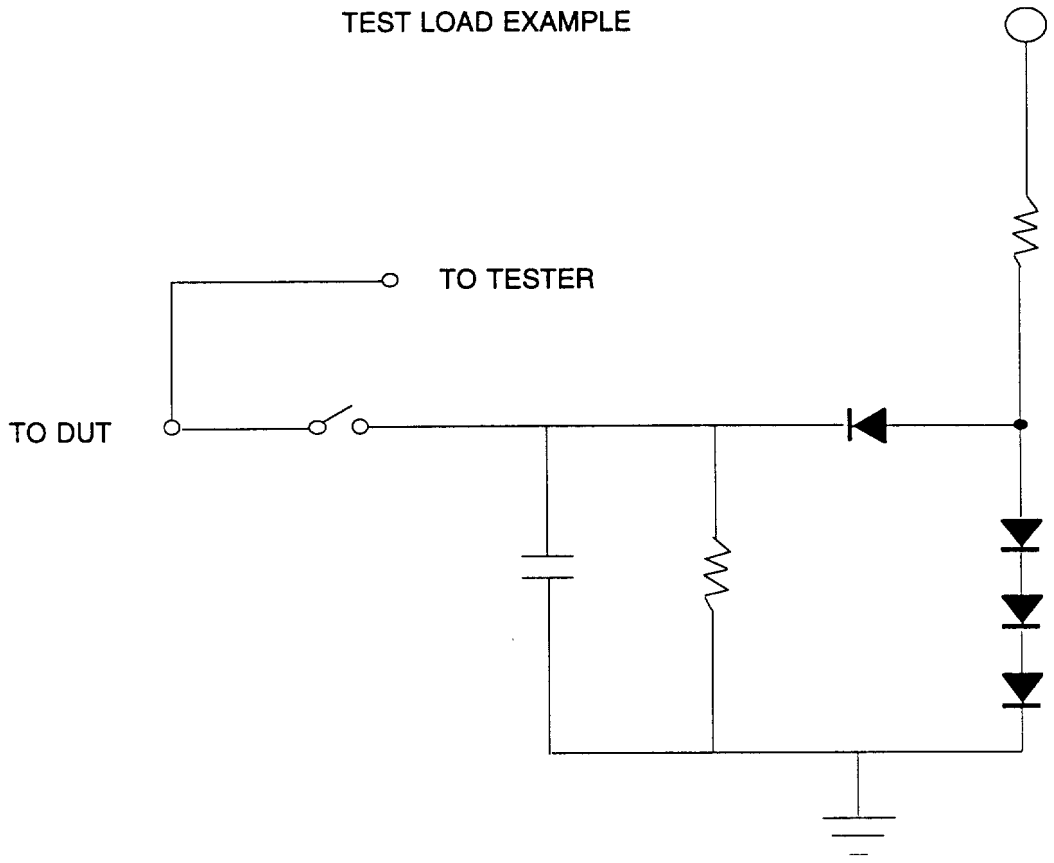


Figure 11: AC Input/Output Reference Waveform

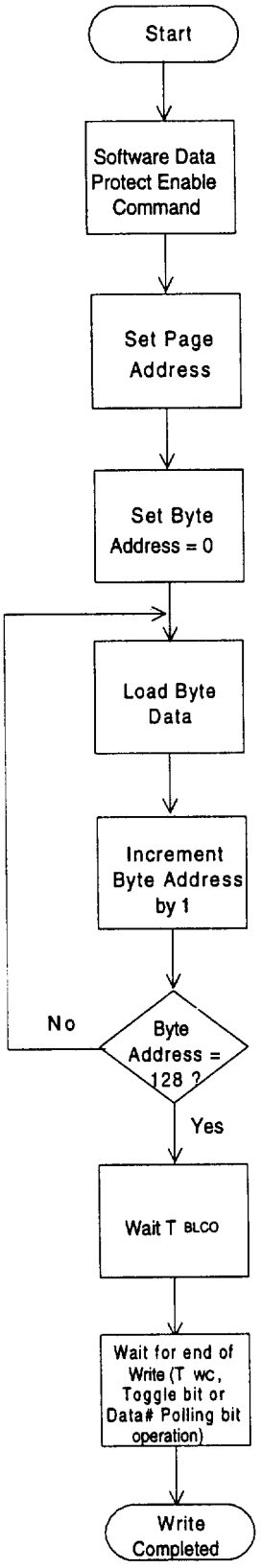


Figure 12 : Write Algorithm

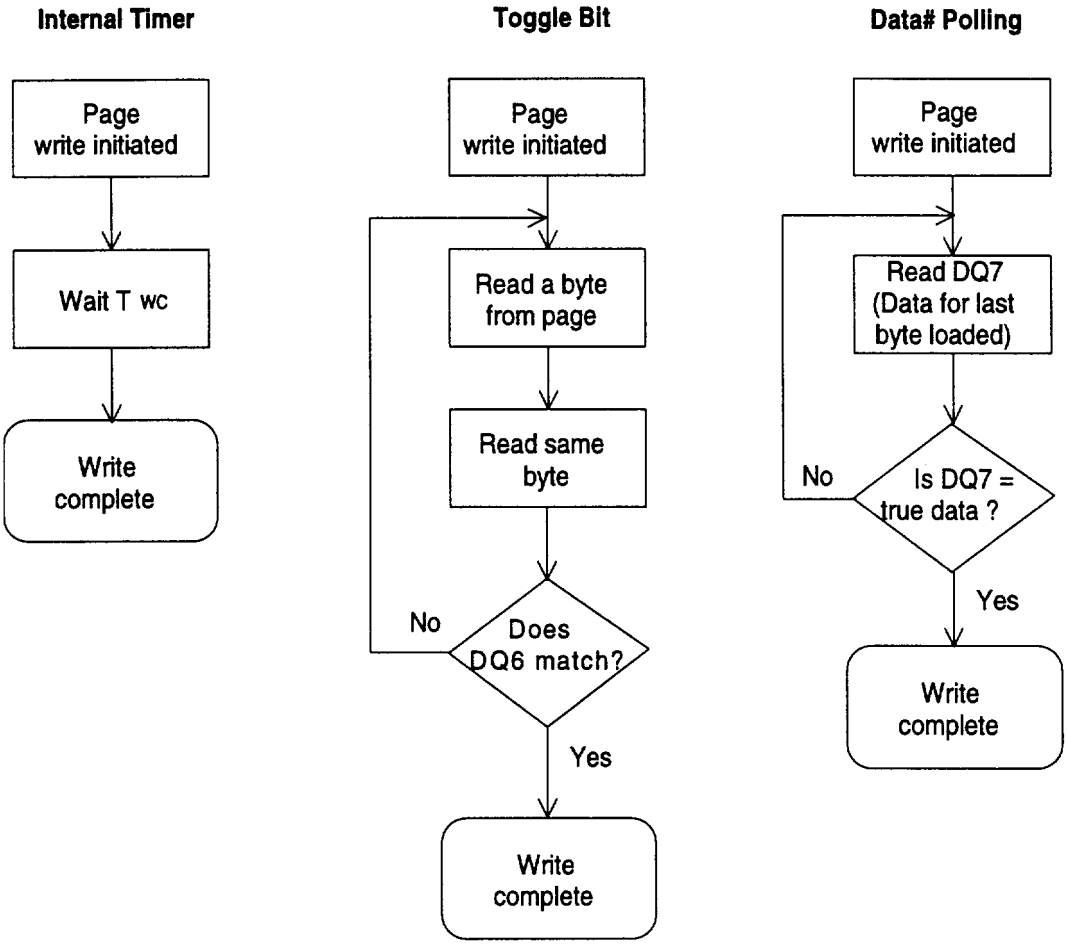


Figure 13 : Write Wait Options

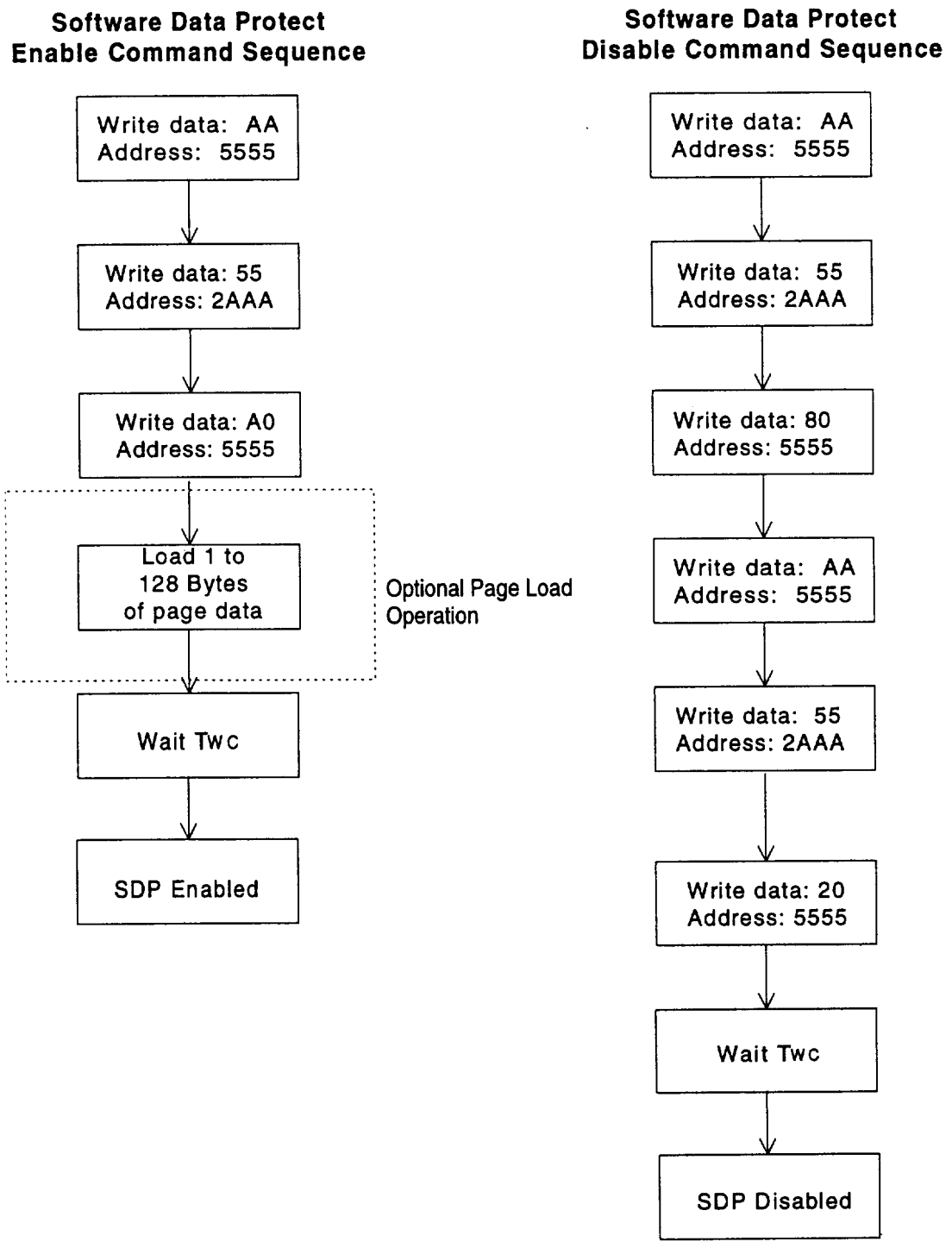
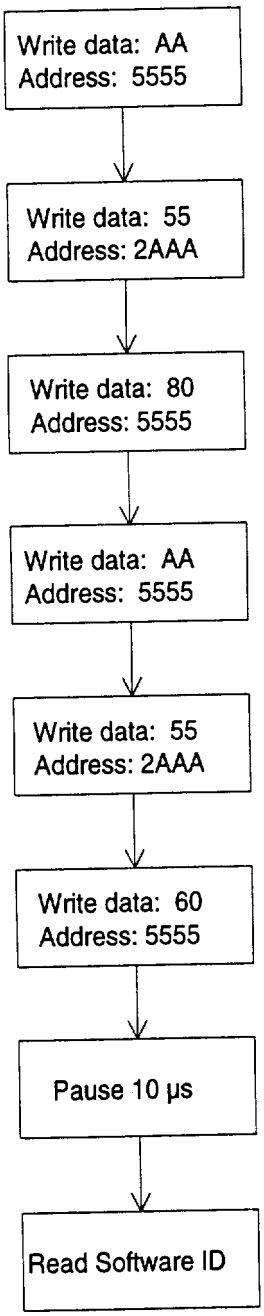
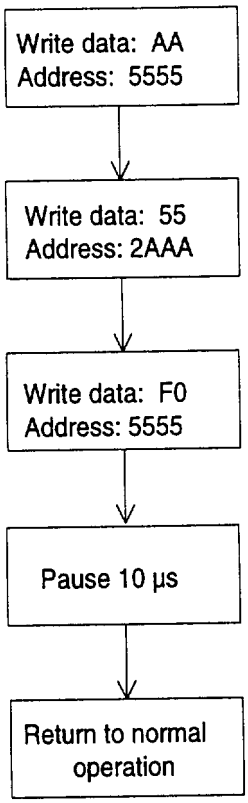


Figure 14: Software Data Protection Flowcharts

Software Product ID Entry Command Sequence



Software Product ID Exit Command Sequence



Software Product Chip-Erase Command Sequence

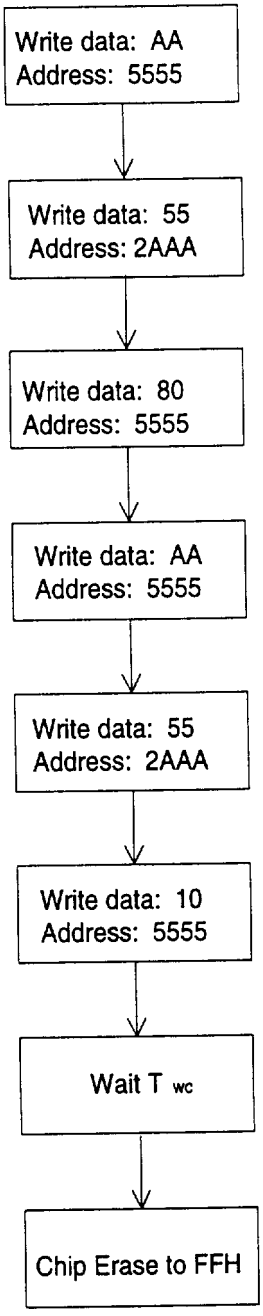


Fig 15 : Software Product Command Codes

Product Ordering Information

Prefix	Device	Speed	Suffix
X X	29LE010	XXX	X X X

V_{CC} Voltage Range
T = 3.0 to 3.6 V

Temperature Range
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
250 = 250 ns
200 = 200 ns
150 = 150 ns

Package Modifier
H = 32 leads
Blank = die

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
F = TSOP (die down)
U = Unencapsulated die

Valid combinations

EH 29LE010-150-4CT	FH 29LE010-150-4CT	NH 29LE010-150-4CT	PH 29LE010-150-4CT
EH 29LE010-200-4CT	FH 29LE010-200-4CT	NH 29LE010-200-4CT	PH 29LE010-200-4CT
EH 29LE010-250-4CT	FH 29LE010-250-4CT	NH 29LE010-250-4CT	PH 29LE010-250-4CT
EH 29LE010-150-3CT	FH 29LE010-150-3CT	NH 29LE010-150-3CT	PH 29LE010-150-3CT
EH 29LE010-200-3CT	FH 29LE010-200-3CT	NH 29LE010-200-3CT	PH 29LE010-200-3CT
EH 29LE010-250-3CT	FH 29LE010-250-3CT	NH 29LE010-250-3CT	PH 29LE010-250-3CT
EH 29LE010-150-4IT	FH 29LE010-150-4IT	NH 29LE010-150-4IT	U 29LE010-250-4CT
EH 29LE010-200-4IT	FH 29LE010-200-4IT	NH 29LE010-200-4IT	
EH 29LE010-250-4IT	FH 29LE010-250-4IT	NH 29LE010-250-4IT	
EH 29LE010-150-3IT	FH 29LE010-150-3IT	NH 29LE010-150-3IT	U 29LE010-250-3CT
EH 29LE010-200-3IT	FH 29LE010-200-3IT	NH 29LE010-200-3IT	
EH 29LE010-250-3IT	FH 29LE010-250-3IT	NH 29LE010-250-3IT	

Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.