Description

The μPD7002 is a high performance, low power, 10-bit CMOS analog-to-digital converter Using the integrating technique the 7002 offers the designer full microprocessor interface, four multiplexed analog inputs, and low power CMOS construction

Features

- ☐ 8- or 10-bit resolution (selectable)
- ☐ 4 channel multiplexed analog input
- ☐ Auto zero and full scale correction without external components
- ☐ High input impedance — 1000 MΩ
- ☐ Internal status register can be accessed by host controller
- ☐ Operates from single +5 V supply
- ☐ Interfaces to most 8-bit microprocessors
- ☐ Low power operation (CMOS)
- ☐ 5 ms conversion speed (10 bits with f_{CK} = 2 MHz)
- ☐ Available in two performance ranges:
  Conversion accuracy (maximum with T_A = 0 to +50°C):
  μPD7002C-1 ..... 0.1% FSR
  μPD7002C ..... 0.2% FSR

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7002C	Plastic DIP	−20°C to +70°C

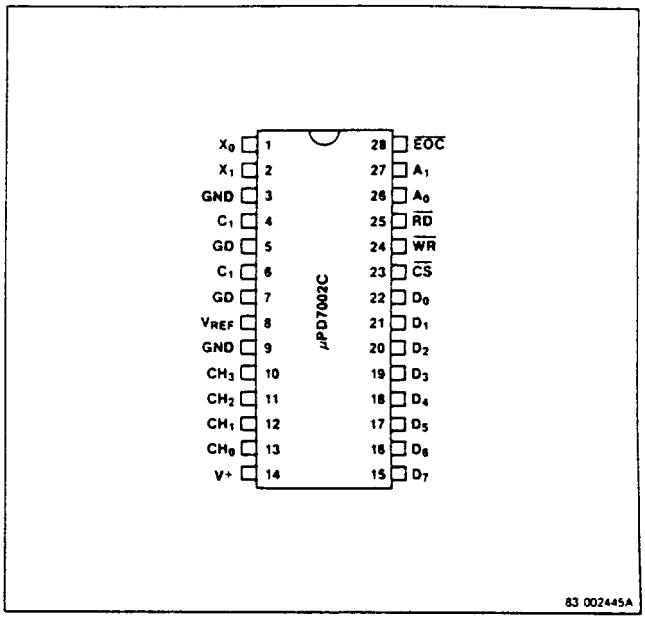
Absolute Maximum Ratings

T_A = +25°C

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage	−0.3 V to +7.0 V
All Input Voltages	−0.3 V to V+ 0.3 V
Power Dissipation	300 mW
Analog GND Voltage	± 0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

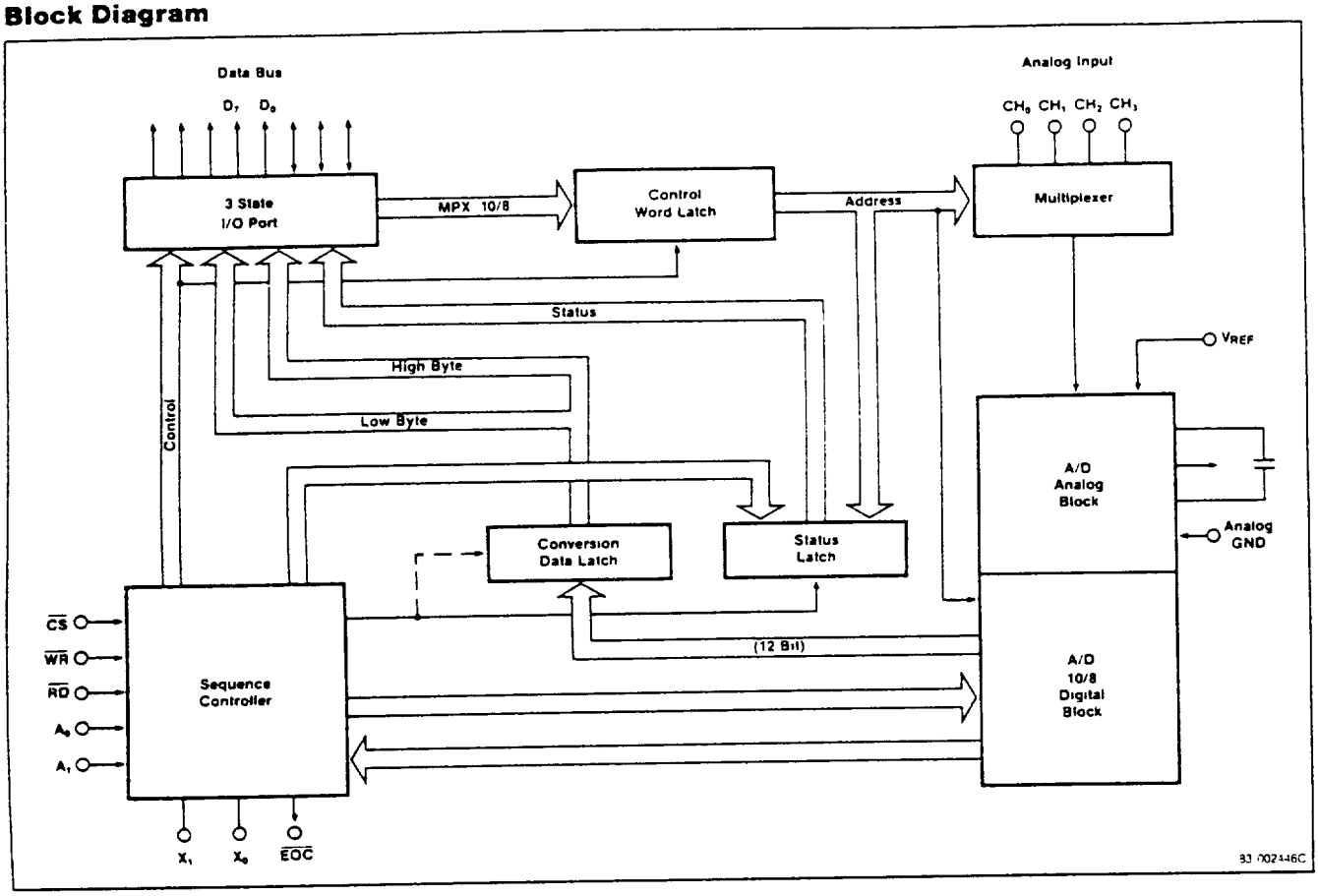
Pin Configuration



Pin Identification

Pin	Name	Function
1, 2	X_0, X_1	External clock input
3	GND	TTL ground
4, 6	CI	Integrating capacitor
5, 7	GD	Guard
8	V_{REF}	Reference voltage input
9	GND	Analog ground
10	CH_3	Analog channel 3
11	CH_2	Analog channel 2
12	CH_1	Analog channel 1
13	CH_0	Analog channel 0
14	V+	Voltage (+5 V)
15-22	D_7-D_0	Data bus
23	$\overline{CS}$	Chip select
24, 25	$\overline{WR}$, $\overline{RD}$	Control bus
26, 27	A_0, A_1	Address bus
28	$\overline{EOC}$	End of conversion interrupt

Block Diagram



Digital I/O Pin Function

Pin	Symbol	Name	I/O	Function
1, 2	X_0, X_1	Xtal	—	Xtal OSC. X_1 can be used as the input of external clock.
15–22	D_7–D_0	Data Bus	Three-state (1 TTL) I/O)	A/D conversion data (High and Low Byte) and internal status output to 8-bit Data Bus. MPY Address, 8/10 select and flag data input from bus. High impedance when μPD7002 is not enabled ($\overline{CS}$ = High).
23	$\overline{CS}$	Chip Select	Input	Low level of $\overline{CS}$ makes other input pins ($\overline{WR}$, $\overline{RD}$, A_0, A_1) enable and data transmission and receiving are possible through data bus pins.
24	$\overline{WR}$	Write	Input	When $\overline{WR}$ = Low, μPD7002 receives new data from data bus.
25	$\overline{RD}$	Read	Input	When $\overline{RD}$ = Low, μPD7002 transmits conversion data and internal status to data bus.
26, 27	A_0, A_1	Address	Input	A_0, A_1 designate the data in data bus (High, Low, Status Byte).
28	$\overline{EOC}$	End of Conversion	Output (1 TTL)	$\overline{EOC}$ indicates the end of conversion to external chips. Read mode operation (high byte output) resetable $\overline{EOC}$.

DC Characteristics

T_A = 0°C to +50°C, V+ = +5 V ± 0.25 V
V_{REF} = +2.50 V, f_{clk} = 1 MHz, C_{INT} = 0.033 μF, 10-Bit Mode

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution, 7002C-1		10	11	12	Bits	
Resolution, 7002C		9	11	12	Bits	
Nonlinearity, 7002C-1			0.05	0.1	%FSR	
Nonlinearity, 7002C			0.1	0.2	%FSR	
Full Scale Error, 7002C-1			0.05	0.1	%FSR	
Full Scale Error, 7002C			0.1	0.2	%FSR	
Zero Scale Error, 7002C-1			0.05	0.1	%FSR	
Zero Scale Error, 7002C			0.1	0.2	%FSR	
Full Scale Temperature Coefficient			10		ppm/°	
Zero Scale Temperature Coefficient			10		ppm/°C	
Analog Input Resistance	R_{IN}		1000		MΩ	V_{IN} = 0 to V+
Total Unadjusted Error 1, 7002C-1	TUE1		0.05	0.1	%FSR	
Total Unadjusted Error 1, 7002C	TUE1		0.1	0.2	%FSR	
Total Unadjusted Error 2, 7002C-1	TUE2		0.05	0.1	%FSR	
Total Unadjusted Error 2, 7002C	TUE2		0.1	0.2	%FSR	
Clock Input Current	I_{clk}		5	50	μA	X_I pin can be used as an external CMOS level clock input. When external clock is applied, X_O pin should be left open.
High Level Output Voltage	V_{OH}	V+ − 1.5			V	I_O = −1.6 mA, T_A = −20 to +70°C
Low Level Output Voltage	V_{OL}			0.45	V	I_O = 1.6 mA, T_A = −20 to +70°C
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0 \leq V_{IN} \leq V+$
Output Leakage Current	I_{OLK}		1	10	μA	$0 \leq V_{IN} \leq V+$
Power Dissipation	P_D		15	25	mW	

AC Characteristics

T_A = +25°C, V+ = +5 V ± 0.25 V, V_{REF} = +2.5 V, f_{clk} = 1 MHz, C_{INT} = 0.033 μF

Parameter	Symbol	Limits Min	Typ.	Max.	Unit	Test Conditions
Conversion Speed (10 bit)	t_{CONV}	8.5	10	15	ms	
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	
Address Setup Time $\overline{CS}$, A_0, A_{11} to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A11 to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to $\overline{CS}$, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to $\overline{CS}$, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	Note 1
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

Note: 1 TTL load + 100 pF

Recommended Operating Conditions

T_A = +25°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.75	5.00	5.25	V	
Reference Voltage	V_{REF}	2.25	2.50	2.75	V	
Analog Input Voltage	V_{IN}	0		V_{REF}	V	Note 1
Clock Frequency	f_{clk}	0.5	1	3	MHz	Note 2
Integrating Capacitor	C_{INT}	0.029	0.033		μF	
High Level Input	V_{IH}	2.2			V	Note 3
Low Level Input	V_{IL}			0.8	V	Note 3
High Level Clock Input	V_{XHL}	V+ − 1.4			V	Note 3
Low Level Clock Input	V_{XLL}			1.4	V	Note 3

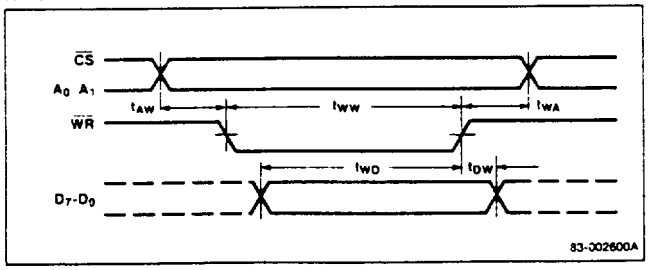
Notes: 1. Negative voltage input (< −0.2 V) decreases the input impedance. Furthermore, conversion error for the input through another MPX channel also increases

Notes [Cont.]:

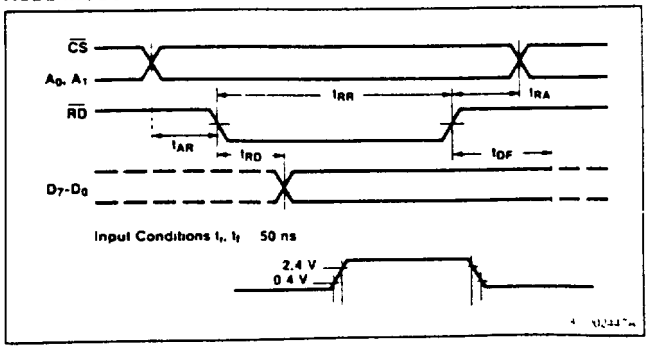
2. Integrating capacitor C_{INT} depends on clock frequency and can be obtained as follows $C_{INT}(\mu F) = 0.033/f_{clk}$ (MHz). Note that conversion time is inversely proportional to the clock frequency
3. T_A = −20°C to +70°C, V+ = +5 V ± 0.25 V

Timing Waveforms

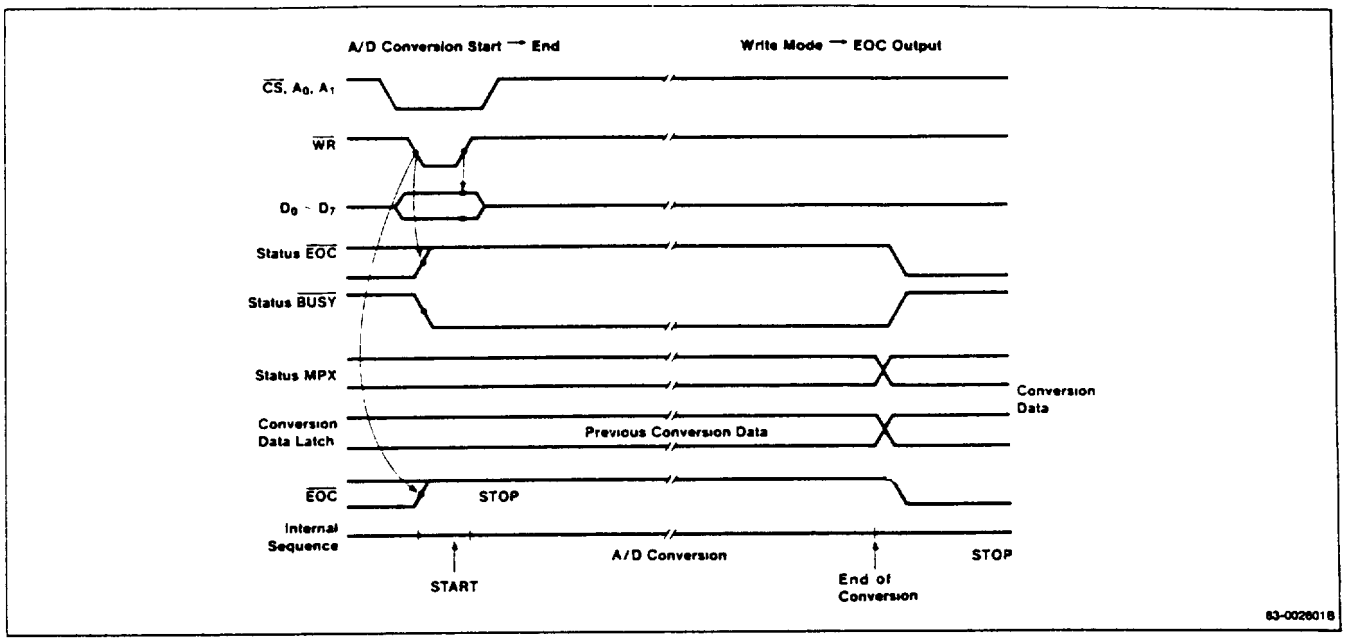
Write Mode



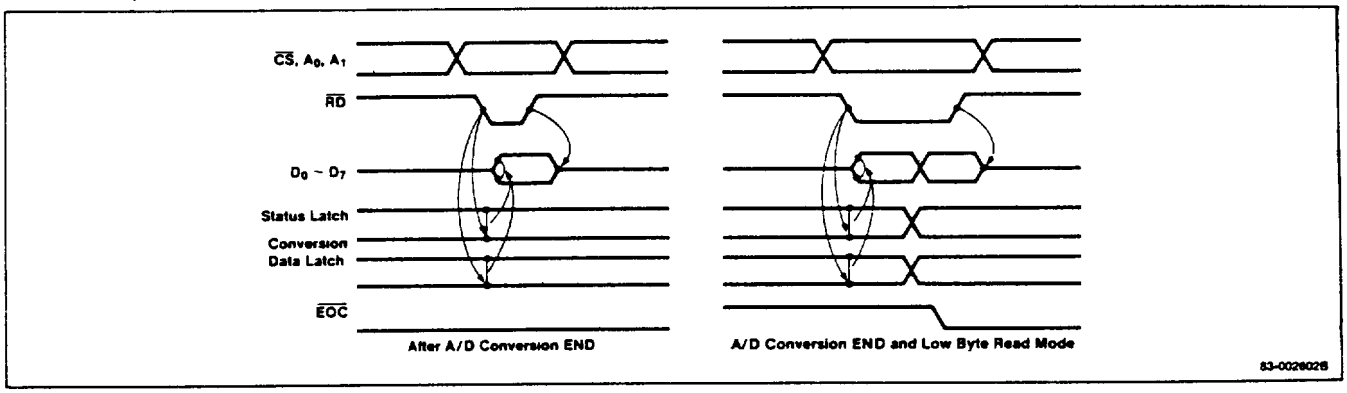
Read Mode



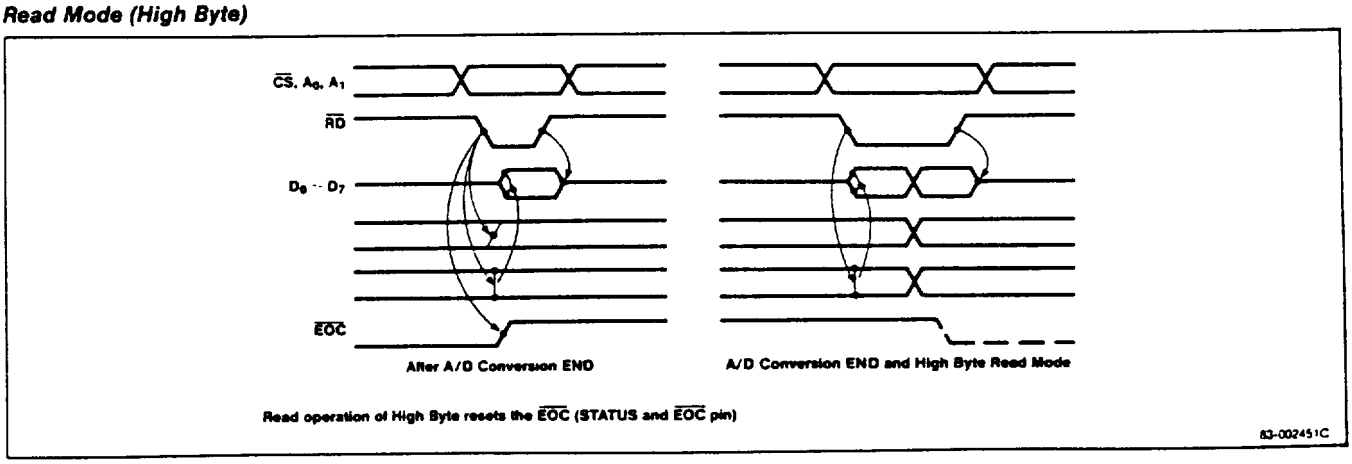
Timing Waveforms (Cont.)



Read Mode (Status, Low Byte)



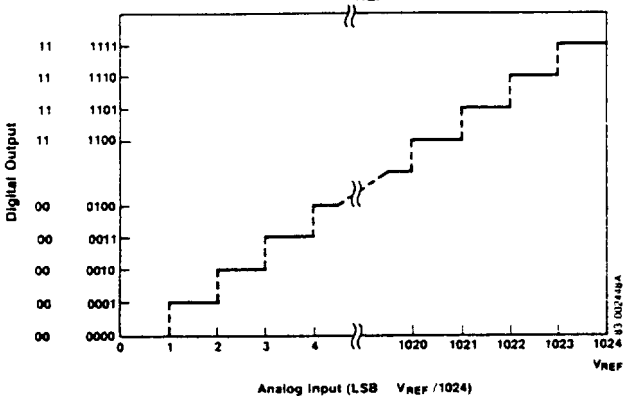
Read Mode (High Byte)



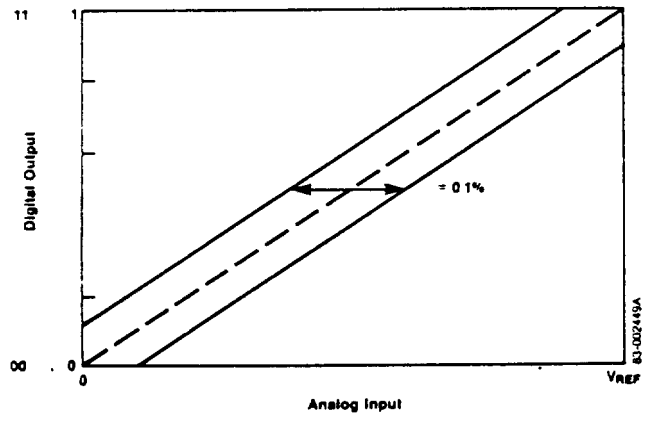
There is some uncertainty whether $\overline{EOC}$ is set or not, when data read operation is made simultaneously with the end of A/D conversion. Furthermore, the reading error occurs at this time, so in this case a dual read operation is recommended.

Operating Characteristics

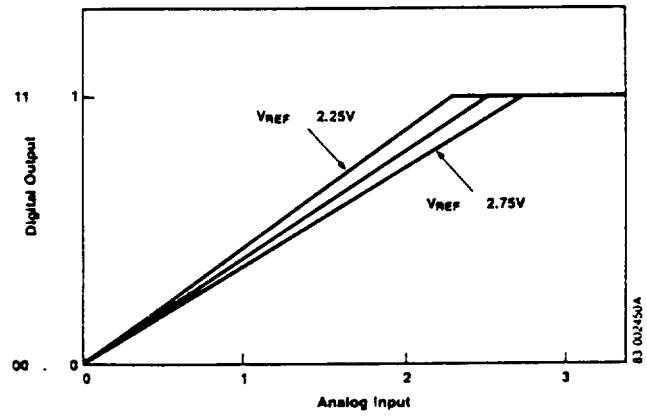
Full Scale vs V_{REF}



Total Unadjusted Error



Transfer Characteristics with Respect to V_{REF}



Addressing the Inputs

One of the four analog inputs is selected by initiating a write mode from the external controller with the control signals as follows. $\overline{CS}$ (pin 23) = "low," $\overline{RD}$ (pin 25) = "high," $\overline{WR}$ (pin 24) = "low," A1 (pin 27) and A0 (pin 26) = "low."

The analog input select data is presented to D0 (pin 22) and D1 (pin 21) and the desired channel (1 to 4) is selected. The conversion resolution mode is also selected during "write" mode by presenting a "high" for 10-bit mode or "low" for 8-bit mode, to D3 at pin 19.

Sequence

- ☐ Initiate "write" mode ($\overline{CS} = 0$, $\overline{RD} = 1$, $\overline{WR} = 0$, A1/A2 = 0).
- ☐ Present data for analog channel select to D0, D1.

	D0	D1
CH0 =	L	L
CH1 =	H	L
CH2 =	L	H
CH3 =	H	H

- ☐ Present conversion resolution data to D3.

10 BIT = H
8 BIT = L

During the write mode the only available function of the μPD7002 is data input from the controlling system. When the write function is terminated the A/D conversion process starts.

The Conversion Process

During the "write" mode the internal sequence controller is initialized and ready to take control of the conversion process on the rising edge of the write pulse. All conversion functions take place with the μPD7002 in the "not selected" mode with the control signals set at: $\overline{CS}$ = "low," $\overline{RD}$ and $\overline{WR}$ "high . . . A0" and A1 "don't care." In the A/D section the analog signal is input via the multiplexer and compared to V_{REF} at pin 8 (V_{REF} sets the maximum full-scale input signal which can be converted). At this point the internal sample and hold for auto zero function and full scale correction are accomplished.

The processed analog signal is then passed to the analog section where the integrating capacitor is charged for a given time period controlled by the clock. In this case the period is 8192 clock periods. The capacitor is then terminated to ground and the falling slope is measured by the number of clock cycles to the zero crossing point. The number of clock cycles from peak to zero (falling slope) is proportional to the value of V_{IN}. The integrator is then set up for the next conversion cycle.

The digital section converts the pulses from the analog section to 12-bit code and sends the converted code to the conversion data register where the data is latched and ready for "reading" by the controlling device The data is then "read" in two bytes by addressing A0 and A1 while in the read mode. A1 = "low" A0 = "high" reads the high data byte (D0 to D7), and A1 = "high" A0 = "either" reads the low data byte (D7 to D4). During the low data byte read D0 to D3 are low and the data on D4 and D5 (bits 11 and 12) may not be accurate data

The internal status can also be checked while in the read mode by setting A0 and A1 both "low."

Operation of Individual Sections

Sequence Controller (See Sequence Chart)

The Sequence Controller controls the internal sequence of A/D conversion and the operation of the three-state I/O buffer. It is initialized by the write mode operation (analog MPX address and 10-/8-bit choice). After the write mode operation, the Sequence Controller starts the A/D conversion, and outputs an $\overline{EOC}$ signal when the conversion is completed. There is no power-on-reset circuitry.

A/D Conversion Block

In the A/D section, an analog signal is input through the MPX and is compared to V_{REF}, after which it is converted to a digital output signal. Full scale analog input is equal to V_{REF}. GND as an analog input is equal to zero scale. A/D conversion time depends on both analog input voltage and conversion mode (10/8 bit).

Three-State I/O Port Section

The three-state I/O port section is controlled by the Sequence Controller. It accepts the MPX address input and conversion mode input (10-/8-bit choice). The three-state I/O port section outputs the internal status and conversion data high/low bytes.

Conversion Data Latch

After the end of conversion, the A/D section outputs new data to the Data Latch. The output of the Data Latch is connected to the three-state I/O ports, and the data can be read at any time. When Data Read occurs simultaneously with an internal data transfer, a read error occurs Therefore, two read operations should be made, unless Data Read occurs after the end of conversion.

Status Latch

The status latch stores the status data internal to the chip, and the internal operation state can be referenced by the status data Status includes the following:

$\overline{BUSY}$, $\overline{EOC}$: Internal sequence state of μPD7002. Write mode operation sets $\overline{BUSY}$, and this is reset at the end of conversion. $\overline{EOC}$ is set at the end of conversion, and High Byte Read Operation resets $\overline{EOC}$.

MSB, 2nd; 10-/8-Bit Flag MPX

The data stored in the conversion Data Latch when the status reading operation is made can be output. Therefore, the data is refreshed at the end of conversion.

Access to the μPD7002 from the CPU can be made by both interrupt and polling methods In the interrupt method use $\overline{EOC}$ as an interrupt signal. In the polling method, use $\overline{EOC}$ and $\overline{BUSY}$ in Status Byte.

After the A/D conversion, the data in the conversion Data Latch does not change, and can be read repeatedly. Therefore, fundamental instructions like Load, Store, Move, etc. can be used to access data (by placing the address of the μPD7002 in memory area). Note that the access time (t_{RD}) and the data setup time (t_{DW}) of the μPD7002 are longer than that of the 8080 and 8085. The following program example shows the accessing of the μPD7002 by polling method in an 8080-based system.

MPX Channel Address Functions

MPX Address Bit	Analog Input Channel			
	CH0	CH1	CH2	CH3
D_1	L	L	H	H
D_0	L	H	L	H

Control Terminal Functions

Control Terminals					Mode	Internal Function	Data I/O Terminals
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_7			
H	x	x	x	x	Not selected	—	High impedance
L	H	H	x	x	Not selected		
L	H	L	L	L	Write mode	Data latch A/D start	Input status. D_1, D_0 = MPX address D_3 = 8-bit/10-bit conversion designation. Note 1. D_7 = Flag input.
L	H	L	L	H	Not selected	—	High impedance
L	H	L	H	L	Not selected		
L	H	L	H	H	Test mode	Test status	Input status. Note 2
L	L	H	L	L	Read mode	Internal status	$D_7 = \overline{EOC}$. D_6 = BUSY. D_5 = MSB. D_4 = 2nd MSB. D_3 = 8/10. D_2 = Flag Output. D_1 = MPX. D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7–D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7–D_0 = 9th – 10th bit
L	L	H	H	H	Read mode	Low data byte	D_3–D_0 = L

Notes: 1 Designation of number of conversion bits 8 bit = L, 10 bit = H
2 Test Mode used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter Therefore, the A/D conversion data read out after this is meaningless.

Bit Function

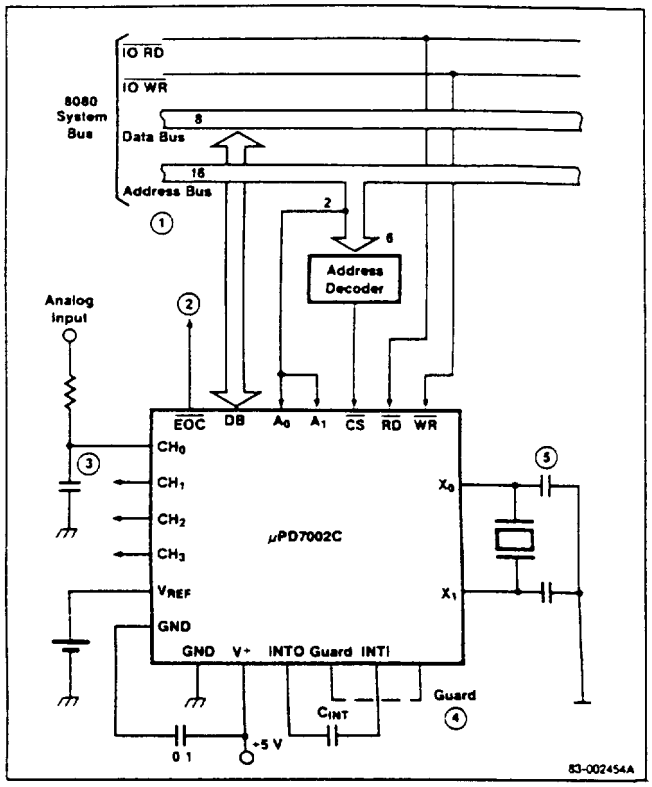
		Write Mode	Read Mode				
		Function	Status Output	High Byte Output		Low Byte Output	
Bit	I/O			10-Bit Note 2	8-Bit	10-Bit Note 2	8-Bit
D7	Output		EOC	MSB	MSB	9th	Note 3
D6	Output		Busy	2nd	2nd	LSB	Note 3
D5	Output		MSB Note 1	3rd	3rd	Q_{11}	Note 3
D4	Output		2nd Bit Note 1	4th	4th	Q_{12}	Note 3
D3	I/O	10/8-Bit	10/8-Bit Note 1	5th	5th	Low	Low
D2	I/O	Flag input	Flag Output Note 1	6th	6th	Low	Low
D1	I/O	MPX Address	MPX Note 1	7th	7th	Low	Low
D0	I/O	MPX Address	MPX Note 1	8th	8th	Low	Low

Notes: 1 Previous conversion data
2 In 10-bit mode, the μPD7002 operates as a 12-bit converter Therefore, 11th and 12th bit data appear at Q_{11} and Q_{12}, and the output of Q_{11} and Q_{12} varies with analog input; however, the data contain internal noise and are meaningless
3. Not to be determined

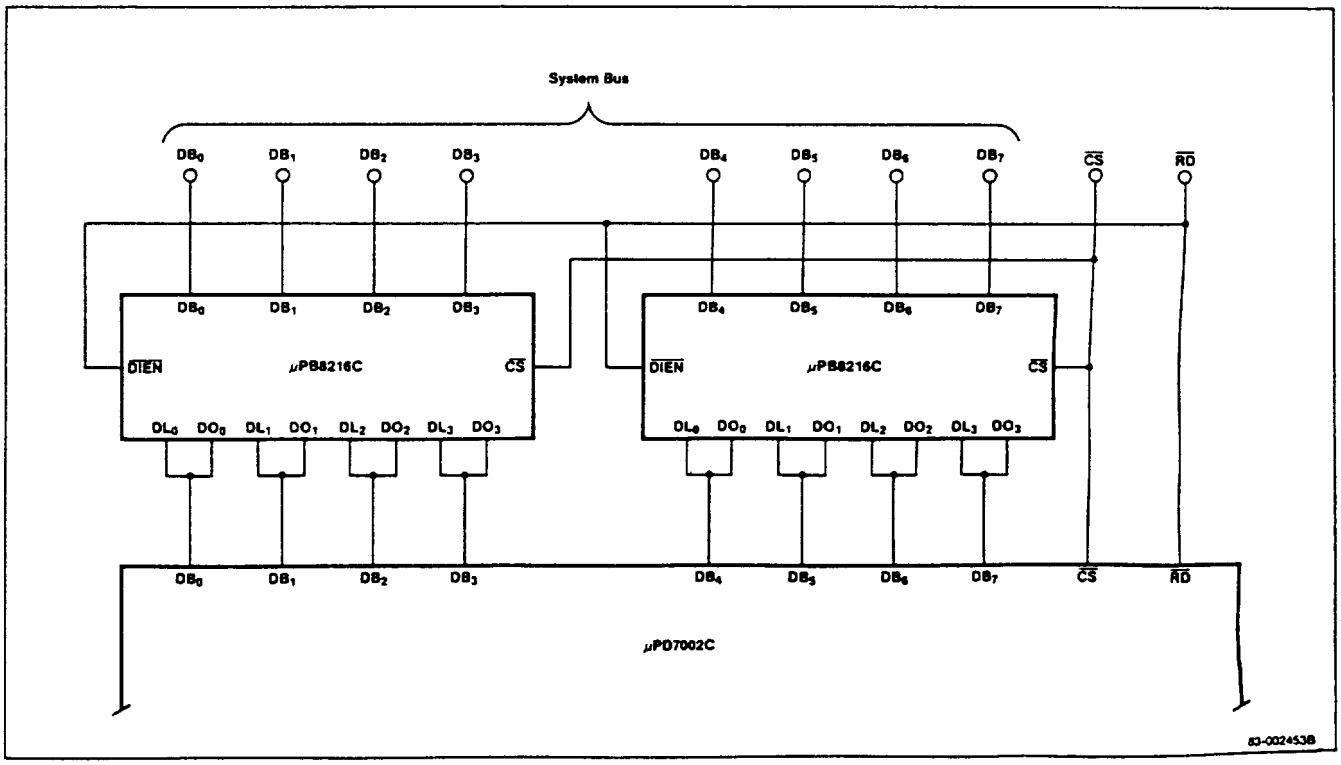
Typical Applications

1. The high level input voltage of the μPD7002C is 2.2 V In a minimum component system configuration, tying 50 kΩ resistors to DB_0-DB_7, A_0, A_1, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ is recommended. The fan-out of DB_0-DB_7 is 1 TTL level. In larger systems, use bus drivers as shown here.
2. Use $\overline{EOC}$ as an interrupt signal if you have an interrupt-driven system.
3. Use a 100 Hz low pass filter to decrease the conversion error Using the diode protection circuit shown here is effective protection against high voltage surges.
4. The μPD7002 uses the integration technique for A/D conversion, and it operates at a very low current level. The external integrating capacitor (C_{INT}) is directly connected to the internal integrator. Using the guard pattern as shown below makes the operation less sensitive to leakage current.
5. Capacitors are tied to the X and X_0 pins to stabilize the oscillation, use a ceramic capacitor about 50 pF. About 50 ms is required for stable oscillation after initial power-on. Therefore, the first Write Mode Operation should occur after this interval.

Typical Microprocessor Interface

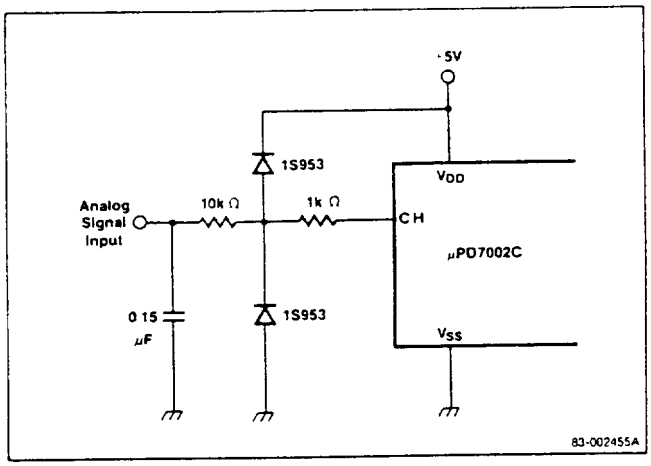


Use of Bus Drivers

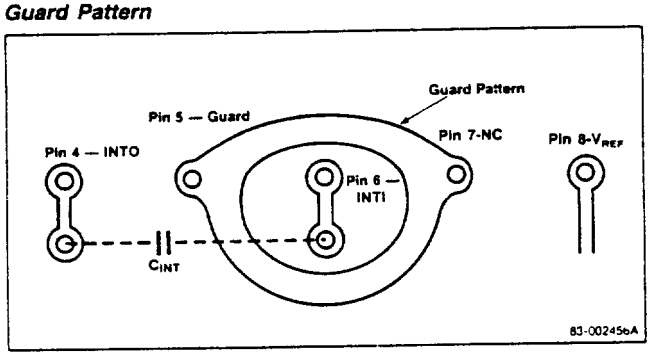


Typical Applications (Cont.)

Diode Protection Circuit



Guard Pattern

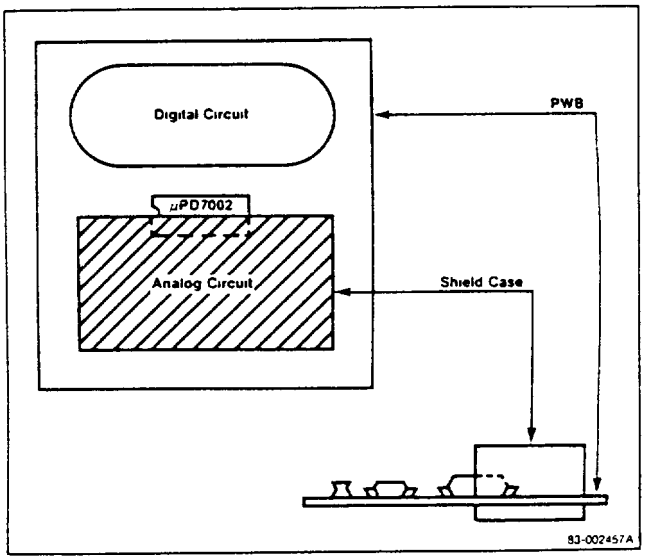


Noise Reduction

The μPD7002 is an integrating A/D converter, however, it operates at a relatively high speed and the normal mode noise rejection cannot be expected. Observance of the following points will minimize noise induction to the input of the analog circuit.

- ☐ Use lower impedance in GND connection
- ☐ Place the bypass capacitors for supply voltage and V_{REF} and analog input close to the μPD7002 (one point GND is also effective)
- ☐ Isolate analog circuitry from digital circuitry.
  - — Component layout
  - — GND wire layout
  - — Shielding of analog circuitry (pin configuration of the μPD7002 is suitable for the layout shown in the next figure)

Shield for Analog Circuitry



APPLICATION HINTS

1. EXTERNAL CLOCK

IF EXTERNAL CLOCK IS USED XI (PIN 2) SHOULD BE USED FOR CLOCK INPUT. XO (PIN 1) SHOULD BE LEFT OPEN.

2. D 2 FLAG INPUT/OUTPUT

D 2 FLAG INPUT DURING WRITE MODE CAN FREELY BE SET OR RESET WITHOUT ANY INFLUENCE TO THE A/D CONVERTER ITSELF. D 2 FLAG OUTPUT DURING STATUS READ WILL HAVE THE CONTENTS AS PROGRAMMED DURING D 2 INPUT.

3. RESOLUTION

INTERNAL RESOLUTION IS 12 BIT BUT 11TH AND 12TH BIT DATA CONTAINS THE INTERNAL NOISE ONLY, ALLTHOUGH THEY VARY WITH ANALOG INPUT. TO INTRODUCE THE 7002 AS A 10 BIT A/D CONVERTER SHOULD BE BETTER AND WILL STOP CONFUSION ON THIS MATTER.

4. GUARD PINS

TO MAKE THE 7002 LESS SENSITIVE AGAINST LEAKAGE CURRENT THE GUARD PIN (PIN 5 AND 7) SHOULD BE USED IN THE WAY SHOWN ON THE PAGE 20.