APCI-ADADIO

Introduction

The APCI-ADADIO is a 32-bit PCI Local Bus board which provides 8 differential (APCI-ADADIOCD) or 16 single-ended (APCI-ADADIOCS) multiplexed analogue inputs, two analogue outputs, 16 digital I/O lines and three counter/timer channels. All I/O signals are routed to a 50 way D-Type socket which conforms to Arcoms standard signal conditioning system (SCS).

Features

- 8 differential or 16 single ended, multiplexed 12-bit ADC channels.
  - 10KHz channel-to-channel acquisition rate.
  - 100KHz repeat rate.
  - 10uS typical conversion rate.
  - +/- 5V, +/-10V,0-5V,0-10V selectable input ranges.
- Two 12-bit(+/-1 bit accuracy) analogue output channels.
  - +/- 5V, +/-10V,0-5V,0-10V selectable input ranges.
  - 10uS settling time to 12-bit accuracy.
- 16 TTL nibble-configurable I/O lines.
  - Output 24mA at 0.45V, sources from 1K resistor at +5V.
  - Selectable power-up states.
- 8254-compatible 3-channel Counter/timer.
  - 1 ADC Timer, 1 Interrupt timer, 1 general purpose timer.
  - 1MHz master operating frequency.
- I/O connector conforms to Arcoms signal conditioning system (SCS).
- Board Access LED (RED).
- User LED (GREEN).
- 32-bit PCI 2.1 Compatible Bus Interface.
- Plug and Play Software compatible.
- CE compliant design.
- Operating Temperature range, 0°C to 70°C.
- Power consumption 180mA @ +5V, 280mA @ +12V.
- MTBF: 220,426 hours (using generic figures from MIL-HDBK-217F at ground benign).

Getting Started

- Power down your PC system.
- Install the board in a spare PCI Slot (See Installation for CE compliance).
- Power up system with MSDOS.
- Run APCI.EXE (supplied on the utility disk), this will search for the board and check I/O access. If this fails, check board is correctly located.

Warning

This board contains CMOS devices which may be damaged by static electricity. Please ensure anti-static precautions are taken at all times when handling this board. If for any reason this board is returned to Arcom control systems, please ensure it is adequately packed, to prevent damage occurring during shipment.

Operation

PCI Bus Interface

The PCI bus is a high speed alternative to ISA bus, it has been designed to overcome some of the limitations of ISA bus, and provide faster throughput for I/O intensive peripheral devices. PCI bus also supports Plug and Play configuration which allows the system software to allocate resources during initialisation helping to overcome address conflicts, which might exist in a system.

The APCI-ADADIO uses a single chip PCI bus slave controller which is designed and manufactured by PLX Technology. This device has been designed to fully support the PCI 2.1 specification and provides plug and play software capabilities. During power-up initialisation the PCI BIOS will detect the card and assign a unique I/O address location and interrupt line. This ensures that there are no resource conflicts on the PCI bus. Multiple cards are supported through this mechanism without the need for address decode links.

The PLX device contains a standard type 00H configuration space header. The table below shows the registers within this header which are required for configuration of the APCI-ADADIO.

Configuration Space Header

Offset	Register Name	Description	Value
00-01H	Vendor ID	ID of PCI device manufacturer	10B5H (PLX Technology)
02-03H	Device ID	ID of PCI device	9050H
18-1BH	Base Address Register	I/O base address assigned to card	0000xxxx
2C-2DH	Subsystem Vendor ID	ID of board manufacturer	13ABH (ARCOM)
2E-2FH	Subsystem ID	ID of Board	0605H (APCI-ADADIO)
3CH	Interrupt Line	Interrupt line assigned to device	0x

These registers can be accessed using PCI BIOS function calls.

I/O Map

The APCI-ADADIO uses an indexed addressing scheme to access the on-board devices and special function registers. Two consecutive I/O locations are required to implement this scheme, the BASE address is used to set the index value and the BASE+1 address is used to access the device. ADC and DAC data is accessed via a dedicated pair of registers which are not part of the indexing scheme.

The I/O base address is set by the PCI BIOS during initialisation (refer to the PCI Bus section of this manual for details). A PCI BIOS function call may be used to determine the base address once the system has been initialised. Multiple boards may be used in a system as each will be given a unique I/O base address.

I/O Address	Function	Read/Write
Base	Index register	Write
Base+1	Control/Status	Read/Write
Base+2	ADC/DAC LSB Data	Read/Write
Base+3	ADC/DAC MSB Data	Read/Write

Index Registers

Index	Register Name	Read/Write	Bit Function
00	Status	Read Base +1	Bit 0 ADC Ready 0 = Conversion completed since last read of ADC Data High byte Bit 1 Counter/Timer Ready 0 = OUT1 has transitioned low-high since Clear CTC Ready was last accessed
00	ADC Start Conversion	Write Base +1	Bit 0-7 Any data starts conversion
00	ADC Data 0-3	Read Base +2	Bit 0-3 ADC 0-3 data
00	ADC Data 4-11	Read Base +3	Bit 0-7 ADC 4-11 data
01	Multiplexer Channel Select	Write Base +1	Bit 0-3 Mux Channel address
02	DACA Register bit 0-3	Write Base +2	Bit 4-7 DACA 0-3 low data
02	DACA Register bit 4-11	Write Base +3	Bit 0-7 DACA 4-11 high data
03	DACB Register bit 0-3	Write Base +2	Bit 4-7 DACB 0-3 low data
03	DACB Register bit 4-11	Write Base +3	Bit 0-7 DACB 4-11 high data
04	Counter/Timer Channel 0	Read/Write Base +1	Counter 0 Value
05	Counter/Timer Channel 1	Read/Write Base +1	Counter 1 Value
06	Counter/Timer Channel 2	Read/Write Base +1	Counter 2 Value
07	Counter/Timer Control	Write Base +1	Control
08	Clear Counter/Timer Interrupt	Write Base +1	Any data clears Interrupt and sets status to 1
09	Digital I/O Configuration	Write Base +1	Bit 0-3 0 = Nibble Output 1 = Nibble Input
0A	Digital I/O 0-7	Read/Write Base +1	Bit 0-7 0 = Input Low 1 = Input High
0B	Digital I/O 8-15	Read/Write Base +1	Bit 0-7 0 = Input Low 1 = Input High
0C-7F	Not Used	N/A	N/A

Special Function Registers

Index	Register Name	Read/Write	Bit Function
80	User LED	Write Base +1	Bit 0 0 = LED Off 1 = LED On
81	Board ID	Read Base +1	Always returns 2DH

Interrupts

The APCI-ADADIO has one interrupt output signal which is routed to an IRQ line during the PCI BIOS initialisation. This interrupt line is expanded on board to provide two interrupt sources. One of these interrupts is connected to the ADC conversion complete signal and the other is connected to the output of counter/timer channel 1.

If a counter/timer interrupt is generated a write sequence to Index register 8 must be executed in order to clear the pending interrupt. The ADC Interrupt is cleared when the high byte data is accessed.

A PCI BIOS call can be used to determine the IRQ signal assigned to this board.

Analogue to Digital Convertor

The APCI-ADADIO contains a single 12-bit successive approximation analogue to digital convertor. The input to this device is connected to a 8 way (APCI-ADADIOCD) or 16 way Multiplexer (APCI-ADADIOCS). Prior to an AD conversion the appropriate channel can be selected by writing to the Multiplexer Channel Select register (Index 1).

The ADC may be triggered from three different sources, selected by links LK9-11. Only one of these links should be fitted at any time to ensure correct operation. The three sources are:-

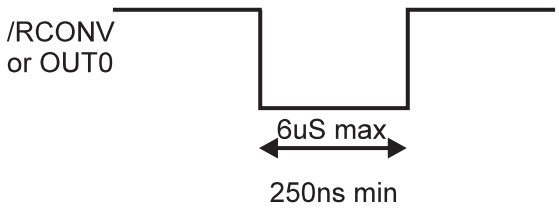
1. Software trigger, initiated by an I/O write sequence.
2. Hardware trigger from an external TTL input (/RCONV), approximately 1-2 uS low pulse.
3. Periodic timer, programmed from the on-board counter/timer channel 0.

The following sequence can be used to perform an A/D conversion when using the software trigger mode.

1. Write 01H to the BASE address.
2. Write to BASE+1 with the Multiplexer value for the appropriate channel.
3. Wait for approximately 50uSec for the input to settle.
4. Write 00H to the BASE address.
5. Write to BASE+1 (any value) to start conversion.
6. Wait for approximately 20uSec for the conversion to complete.
7. Read BASE+1 and check bit 0 is at logic '0' i.e. conversion completed.
8. Read BASE+2 ADC data low nibble (bits 0-3).
9. Read BASE+3 ADC data high byte (bits 4-11).

The hardware trigger mode uses /RCONV on PL1 and the periodic timer mode uses counter/timer channel 0 output to trigger the ADC. Conversion is initiated from these sources when /RCONV or OUT0 are low. To ensure that the ADC does not perform multiple conversions the hardware and timer pulses must be greater than 250nS and less than 6uS.

Maximum data throughput can be obtained by triggering a new conversion before data has been read from the last conversion. To ensure that the ADC data registers contain the data from the last conversion they must be read within 6uS of triggering a new conversion.



Digital to Analogue Convertor

The APCI-ADADIO contains two 12-bit digital to analogue convertors. On-board links can be used to select between three possible output ranges +/- 5V, 0-5V and 0-10V. The DAC values are updated by

writing to the data register at BASE+2 (Low nibble bits 0-3) and BASE + 3 (High byte bits 4-11). Prior to this the DAC channel must be selected by writing a value of 02H to the Index register for DAC A and 03H for DAC B.

Digital I/O

The APCI-ADADIO provides 16 digital I/O lines, these are grouped into four nibbles. Each nibble has a power-up/reset state link and can be programmed as either input or output via the Digital I/O configuration register.

Access to the individual I/O lines is via Index registers 0AH and 0BH. Reading these registers will provide the status of all I/O lines regardless of whether they are configured as input or output. It is possible to use these lines as bi-directional with some careful programming ensuring that a conflict does not exist on any of these lines.

Note:- If a nibble is to be used as an input the reset state link must be set to the high position, otherwise the lines will be driven low as outputs which may cause damage.

Counter/Timer

The APCI-ADADIO contains an 8254 compatible counter/timer, which provides three 16-bit counter/timers. Channel 0 can be used to trigger an A/D conversion and channel 1 can cause an interrupt request sequence to be initiated.

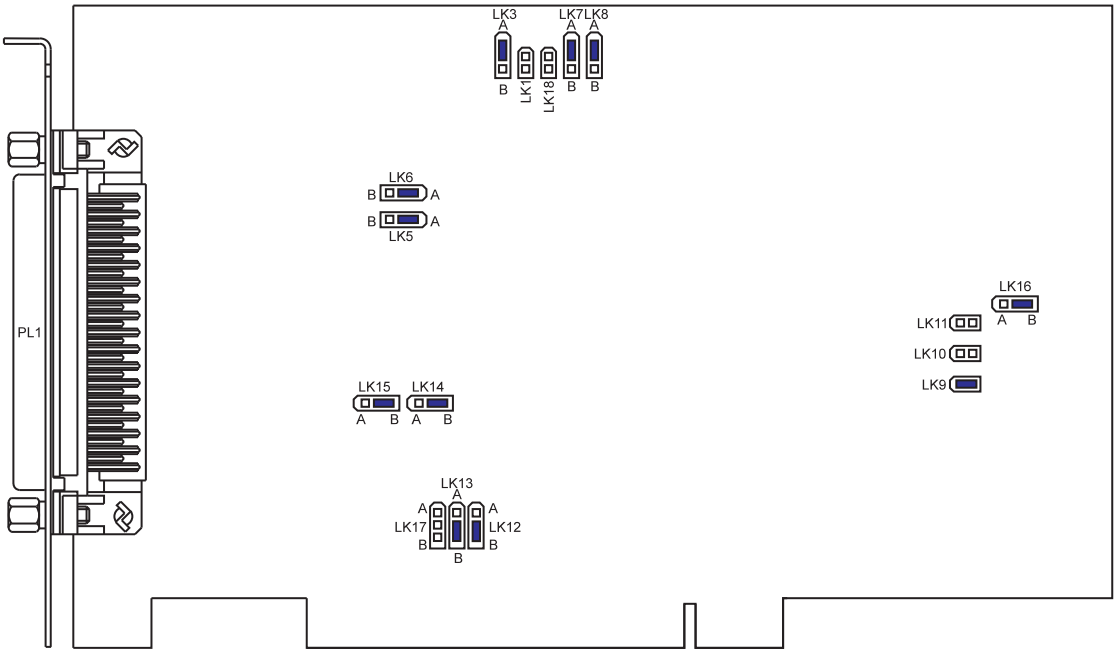
A external connector (PL3) has been provided to allow internal or external signals to be used as clock sources. The connector has been arranged to allow the on-board 1Mhz clock to be connected to the clock input on channel 1 and 2 via links. The outputs of these timers can also be cascaded to provide longer timing sequences.

Counter 0 should always be programmed in mode 2 which ensures that the output signal is only active for a single clock cycle (i.e. 1uS when connected to the 1MHz clock). When the output from counter 2 is used as the clock source the time between rising edges must not exceed 6 uS or be less than 250nS.

Links

Throughout this section a '+' indicates the default link position.

Default Link Position Diagram



LK1: Psedo Differential Ground Connection

Fit	APCI-ADADIOCS, fit only if inputs are isolated from oVA
Omit	APCI-ADADIOCD, Differential inputs

LK3: Differential/Single-Ended Input selection

A	Differential - APCI-ADADIOCD
B	Single Ended - APCI-ADADIOCS

LK5-6: DAC Output range

LK5 and LK6 are used to select the output range for DAC1 and DACo respectively. The range settings are as below:

+A	-5V to +5V
B	oV to +5V
None	oV to +10V

LK7-8 and LK18 ADC Input Ranges

These links are used to select the ADC input range. The range settings are as below:

LK7	LK8	LK18	Range
+A	+A	+Omit	-5V to +5V
A	B	Omit	oV to +10V
B	A	Omit	-10V to +10V
A	B	Fit	oV to +5V

Note:- Both links should not be fitted in position B on LK7 and LK8.

LK9-11 ADC Trigger Sources

These links are used to select between the three different ADC trigger sources. Each trigger source is enabled when the link is fitted. To ensure correct operation only one link should be fitted.

+LK9	Enable Software trigger
LK10	Enable Hardware trigger
LK11	Enable Counter/timer channel o trigger

LK12-15 Digital I/O Reset State

These links select the state of the digital I/O lines at reset in nibble (4 bit) groups.

The link associated with each nibble is shown below:

LK15 Digital I/O lines 0-3
LK14 Digital I/O lines 4-7
LK13 Digital I/O lines 8-11
LK12 Digital I/O lines 12-15

A	Sets output low
+B	Sets output high

Note: If a nibble is to be used as an Input the corresponding link should be placed in position B to ensure damage is not caused to the card or external circuitry.

LK16 Counter/Timer Channel o clock source

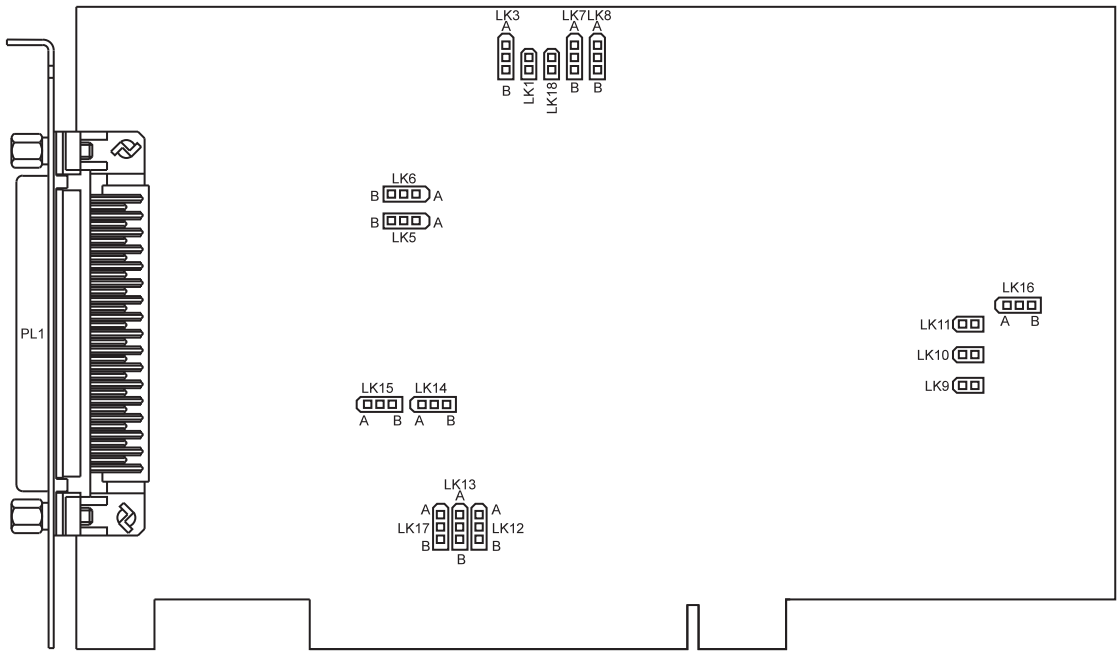
This link selects the clock source for counter timer channel o.

LK16A	Clocked by output from Counter/timer channel 2
+LK16B	1MHZ Clock

LK17 Digital I/O Reset Test Link

Used for automated board testing of the digital I/O lines , to ensure they reset into the correct states and should be left in position A.

User Configuration Record Diagram



Pseduo Differential Ground	LK1	
Differential/Single Ended Input	LK3	
DAC Output range	LK5	
	LK6	
ADC Input Ranges	LK7	
	LK8	
	LK18	
ADC Trigger Sources	LK9	
	LK10	
	LK11	
Digital I/O Reset State	LK12	
	LK13	
	LK14	
	LK15	
Counter/Timer Channel o Clock Source	LK16	
Digital I/O Reset Test Link	LK17	

Utility Disk

A demonstration program has been provided on the utility disk ADADIO.EXE.

This can be used to aid calibration and as source code is provided it will help demonstrate the method used for accessing devices.

ADADIO.EXE
This program will display the ADC inputs, scroll an active bit along the digital I/O and allows setting of the DAC's. These will work with standard link settings. Decrementing counter/timer counts and incrementing interrupt counts are also displayed, but a link must be fitted between pins 9 and 10 on PL3.

ADADIO.INI
This is a text file which is used by the ADADIO program to select the number of channels, ADC and DAC ranges etc. This file can be edited to reflect any changes in the board settings.

Calibration

Calibrating the ADC

In order to calibrate the ADC it is necessary to use a precision digital voltmeter (DVM) with at least 5 digit resolution and a high stability low noise DC signal source. During calibration it is necessary to continually read and display the ADC data. A program ADADIO.EXE has been provided on the utility disk to enable this.

Two trim adjusters, VR7 and VR1 , are provided for trimming the zero offset and gain respectively. These trims are for fine-adjusting the standard ranges.

Unipolar Calibration

Set the necessary links for unipolar operation and the required voltage range. Run the ADADIO.EXE program.

Zero Offset Adjust
1) Set the input voltage to 0.0000V.
2) Adjust VR7 to give 000 to 001 hex.

Full Scale Gain Adjust
1) Set the input voltage to full scale minus 1 LSB
+4.9985 for the 5V range.
+9.9975 for the 10V range.
2)Adjust VR1 to give FFE to FFF.

Bipolar Calibration

Set the necessary links for bipolar operation and the required voltage range. Run the ADADIO.EXE program.

Bipolar Offset Adjust
1) Set the input voltage to full scale negative plus 1 LSB
-4.9975 for the 5V range.
-9.9950 for the 10V range.
2) Adjust VR7 to give 000 to 001 hex.

Full scale Gain Adjust

1) Set the input voltage to full scale positive minus 1 LSB
   +4.9975 for the 5V range.
   +9.9950 for the 10V range.
2) Adjust VR1 to give FFE to FFF.

Calibrating the DACs

In order to calibrate the DACs it is necessary to have a DVM with at least 5 digit resolution. On the utility disk there is a

A single trimmer (VR2) is provided to adjust the reference voltage used by the DACs

Set the necessary links for the required mode and voltage ranges. Run the ADADIO.EXE program . Measure the voltage between VREF (TP3) and AGND (TP9)and adjust VR2 until the reading is +5.02V.

Note:- If the gain adjust trimmers (VR3-4) have insufficient range , adjust VR2 to read 5.01V, and repeat the calibration procedure.

Unipolar Calibration - DAC Channel A

Zero Offset Adjust

1) Set DAC A output to 000 hex.
2) Measure the voltage between DAC A output and analogue ground and adjust VR5 to give 0.000V.

Full Scale Gain Adjust

1) Set DAC A output to 800 hex,
2) Measure the voltage between DAC A output and analogue ground and adjust VR3 to exactly half scale output.
   2.500V for the 0-5V range.
   5.000V for the 0-10V range.
3) Set DAC A output to FFF hex and check output voltage is:-
   4.9985 for the 0-5V range.
   9.9975 for the 0-10V range.
4) Adjust VR3 if necessary.

Repeat for DAC B replacing VR5 with VR6, and VR3 with VR4.

Bipolar Calibration - DAC Channel A

Zero Offset Adjust

1) Set DAC A output to 000 hex.
2) Measure the voltage between DAC A output and analogue ground and adjust VR5 to give full scale negative i.e -5.000V.

Full Scale Gain Adjust

1) Set the DAC A output to 800 hex.
2) Measure the voltage between DAC A output and analogue ground and adjust VR3 to give half scale output i.e 0.000V.
3) Set DAC A to FFF hex and check full scale is 4.9975V.

Repeat for DAC channel B replacing VR5 with VR6, and VR3 with VR4.

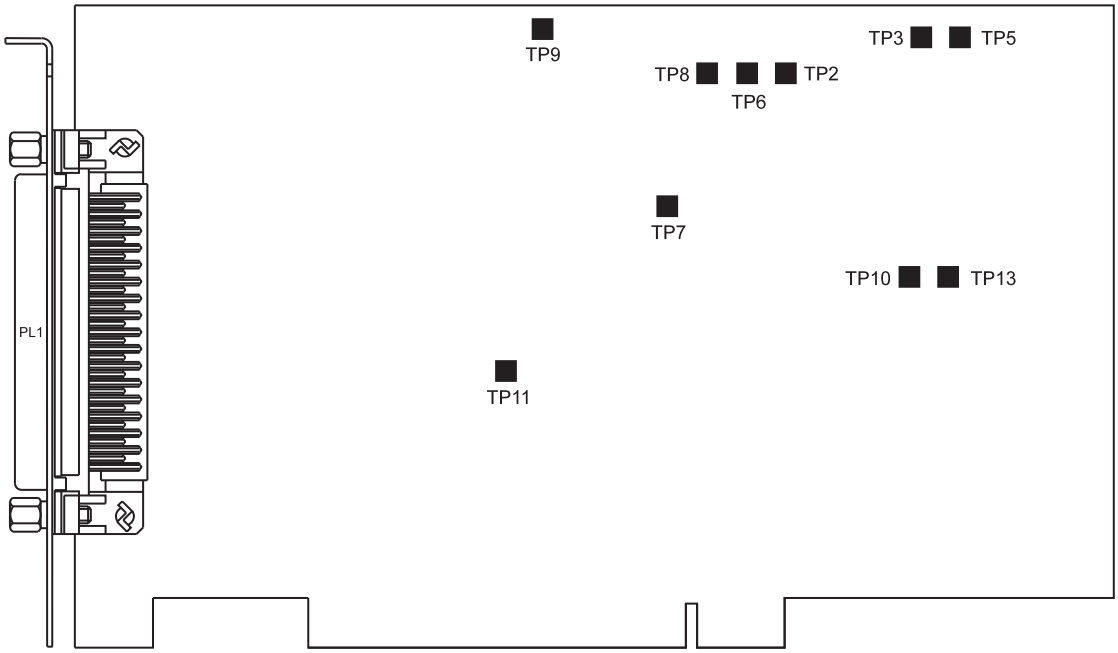
Test Point Locations

Test Point	Description
TP2	DAC +5V Voltage Reference.
TP3	+5V Analogue supply voltage.
TP5	+15V Analogue supply voltage.
TP6	-15V Analogue supply voltage.
TP7	ADC Chip enable signal.
TP8	ADC Status Signal.
TP9	Analogue ground.
TP10	Digital ground.
TP11	Active low reset signal.
TP13	+5V digital supply.

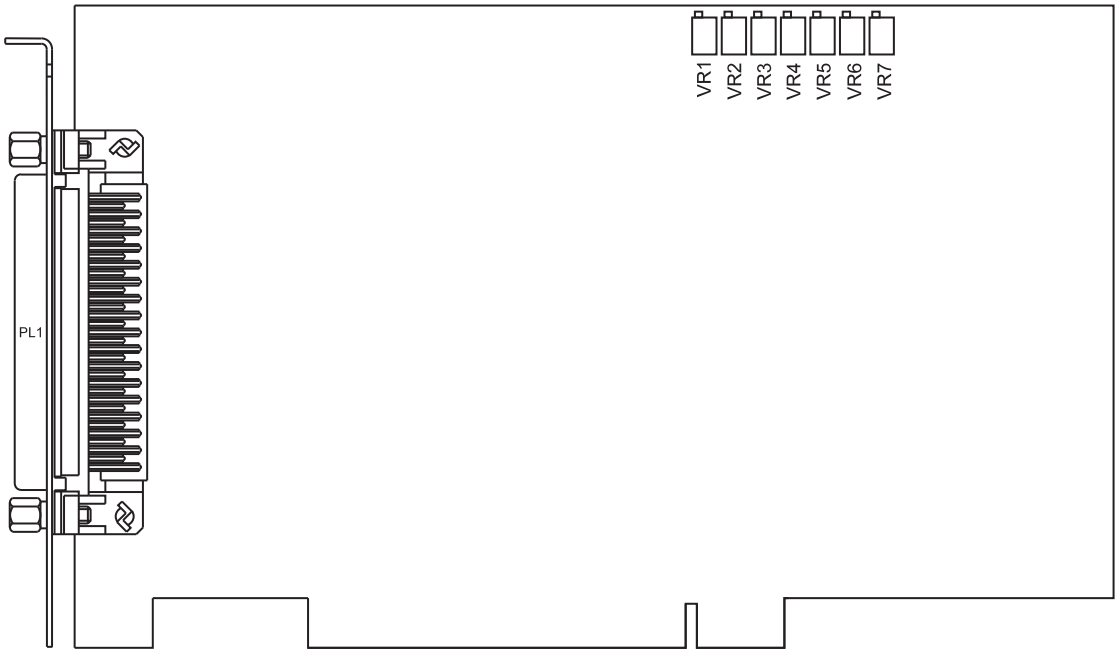
Trimmer Locations

Trimmer	Function
VR1	ADC Gain
VR2	DAC Reference Voltage
VR3	DAC Channel A Gain
VR4	DAC Channel B Gain
VR5	DAC Channel A zero Offset
VR6	DAC Channel B zero Offset
VR7	ADC zero Offset

Test Point Location Diagram



Trimmer Location Diagram



D-50 I/O Connector (PL1) Pin Assignments

The pin assignments are listed with the pin number of the D-50 connector and also the pin number when a 50-way IDC ribbon cable is connected to the D-50. The pin assignments conform to the Arcom signal conditioning system (SCS) and may be connected to an external signal conditioning board.

Ribbon Cable Pin No.	D-Type Pin No.	Signal Name
1	1	ANALOGUE GROUND
2	34	PDIFF
3	18	CH0+
4	2	CH0-/CH8+
5	35	CH1+
6	19	CH1-/CH9+
7	3	CH2+
8	36	CH2-/CH10+
9	20	CH3+
10	4	CH3-/CH11+
11	37	ANALOGUE GROUND
12	21	PDIFF
13	5	CH4+
14	38	CH4-/CH12+
15	22	CH5+
16	6	CH5-/CH13+
17	39	CH6+
18	23	CH6-/CH14+
19	7	CH7+
20	40	CH7-/CH15+
21	24	GND
22	8	PDIFF
23	41	DIGITAL I/O 0
24	25	DIGITAL I/O 1
25	9	DIGITAL I/O 2

Ribbon Cable Pin No.	D-Type Pin No.	Signal Name
26	42	DIGITAL I/O 3
27	26	DIGITAL I/O 4
28	10	DIGITAL I/O 5
29	43	DIGITAL I/O 6
30	27	DIGITAL I/O 7
31	11	GND
32	44	/RCONV
33	28	DIGITAL I/O 8
34	12	DIGITAL I/O 9
35	45	DIGITAL I/O 10
36	29	DIGITAL I/O 11
37	13	DIGITAL I/O 12
38	46	DIGITAL I/O 13
39	30	DIGITAL I/O 14
40	14	DIGITAL I/O 15
41	47	ANALOGUE GROUND
42	31	RESERVED
43	15	DACA
44	48	DACB
45	32	N/C
46	16	N/C
47	49	-12V
48	33	+12V
49	17	+5V
50	50	+5V

10-way IDC Header (PL3)

PL3 is used for connecting external signals to buffered versions of the Counter/timer inputs and outputs for channels 1 and 2. For maximum flexibility the connections have been arranged to allow clock inputs to be linked to the standard 1MHz clock or other channel outputs using jumper links.

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	+5V
3	CLK2	4	CLK1M
5	OUT1	6	GATE2
7	GATE1	8	OUT2
9	CLK1M	10	CLK1

Installation for CE Compliance

To maintain compliance with the requirements of the EMC directive (89/336/EEC), this product must be correctly installed. The PC system in which the board is housed must be CE compliant as declared by the manufacturer. The external I/O cable should be the Arcom CAB50CE, or a fully screened cable to the same pattern.

1. Remove the cover of the PC observing any additional instructions of the PC manufacturer.
2. Locate the board in a spare PCI slot and press gently but firmly into place.
3. Ensure that the metal bracket attached to the board is fully seated.
4. Fit the bracket clamping screw and firmly tighten this on the bracket.

Note:- Good contact of the bracket to the chassis is essential.

5. Replace the cover of the PC observing any additional instructions of the PC manufacturer.

The following standards have been applied to this product:

BS EN50081-1 : 1992 Generic Emissions Standard, Residential, Commercial, Light Industry
BS EN50082-1 : 1992 Generic Immunity Standard, Residential, Commercial, Light Industry
BS EN55022 : 1995 ITE Emissions, Class B, Limits and Methods.

Revision History

Manual	PCB	Comments	
Issue A	V1 Iss 1	980512	First released in this format.

Product Information

Full information about other Arcom products is available via the **Fax-on-Demand System**, (Telephone Numbers are listed below), or by contacting our **WebSite** in the UK at: **www.arcom.co.uk** or in the US at: **www.arcomcontrols.com**

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