

MM74HC4514 4-to-16 Line Decoder with Latch

General Description

The MM74HC4514 utilizes advanced silicon-gate CMOS technology, which is well suited to memory address decoding or data routing application. It possesses high noise immunity and low power dissipation usually associated with CMOS circuitry, yet speeds comparable to low power Schottky TTL circuits. It can drive up to 10 LS-TTL loads.

The MM74HC4514 contain a 4-to-16 line decoder and a 4-bit latch. The latch can store the data on the select inputs, thus allowing a selected output to remain HIGH even though the select data has changed. When the LATCH ENABLE input to the latches is HIGH the outputs will change with the inputs. When LATCH ENABLE goes LOW the data on the select inputs is stored in the latches. The four select inputs determine which output will go HIGH provided the INHIBIT input is LOW. If the INHIBIT input is HIGH all outputs are held LOW thus disabling the decoder.

The MM74HC4514 is functionally and pinout equivalent to the CD4514BC and the MC1451BC. All inputs are protected against damage due to static discharge diodes from V_{CC} and ground.

Features

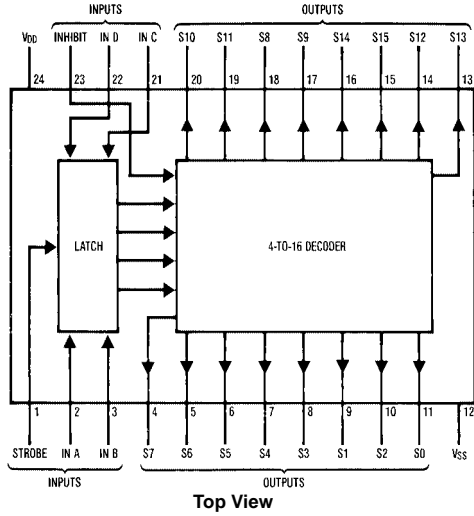
- Typical propagation delay: 18 ns
- Low quiescent power: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads (74HC Series)

Ordering Code:

| Order Number | Package Number | Package Description |
|---------------|----------------|---|
| MM74HC4514WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74HC4514MTC | MTC24 | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC4514N | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

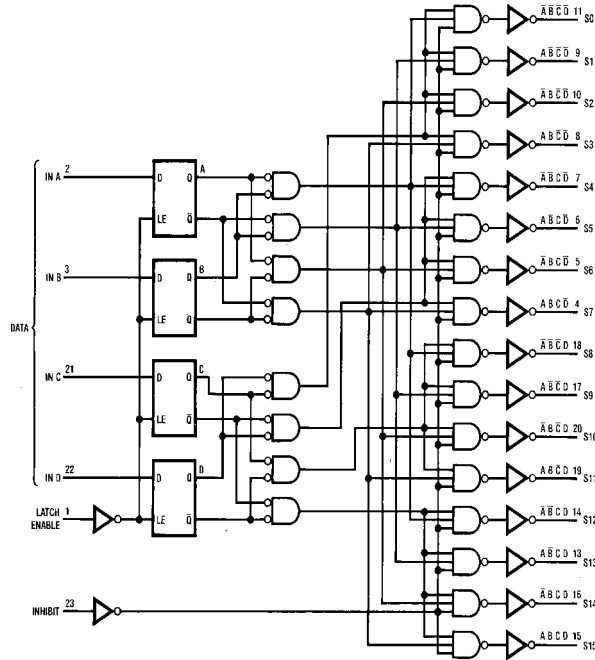
Connection Diagram



Truth Table

| LE | Inhibit | Data Inputs | | | | Selected Output High |
|----|---------|-------------|---|---|---|----------------------|
| | | D | C | B | A | |
| H | L | L | L | L | L | S0 |
| H | L | L | L | L | H | S1 |
| H | L | L | L | H | L | S2 |
| H | L | L | L | H | H | S3 |
| H | L | L | H | L | L | S4 |
| H | L | L | H | L | H | S5 |
| H | L | L | H | H | L | S6 |
| H | L | L | H | H | H | S7 |
| H | L | H | L | L | L | S8 |
| H | L | H | L | L | H | S9 |
| H | L | H | L | H | L | S10 |
| H | L | H | L | H | H | S11 |
| H | L | H | H | L | L | S12 |
| H | L | H | H | L | H | S13 |
| H | L | H | H | H | L | S14 |
| H | L | H | H | H | H | S15 |
| X | H | X | X | X | X | All Outputs = 0 |
| L | L | X | X | X | X | Latched Data |

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|--|-------------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering 10 seconds) | 260°C |

Recommended Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | -40 | +85 | °C |
| Input Rise or Fall Times (t_r, t_f) | | | |
| $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ\text{C}$ | | $T_A = -40$ to 85°C | $T_A = -55$ to 125°C | Units | | |
|---|-----------------------------------|---|----------|----------------------------------|--|-----------------------------------|------------------------------------|---------------|-----|-----|
| | | | | Typ | Guaranteed Limits | | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V | | |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | | | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | | 2.0V | | 0.5 | 0.5 | 0.5 | V | | |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | | | |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu\text{A}$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V | | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | | | |
| | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | | | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V | | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | | | |
| | | | V_{OL} | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu\text{A}$ | 2.0V | 0 | | 0.1 | 0.1 |
| 4.5V | 0 | | | | | 0.1 | 0.1 | | 0.1 | |
| 6.0V | 0 | 0.1 | 0.1 | 0.1 | | | | | | |
| $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V | | | | |
| | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | | | | | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA | | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$ | 6.0V | | 8.0 | 80 | 160 | μA | | |

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

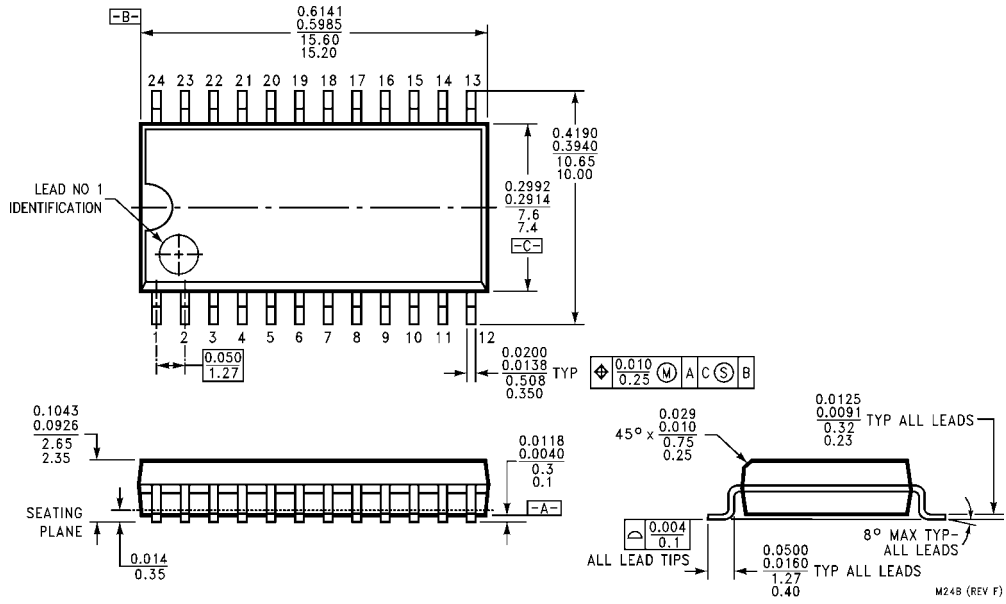
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|-----------------------|---|------------|-----|------------------|-------|
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | | 18 | 30 | ns |
| t_{PHL} | Maximum Propagation Delay LE to Output | | 18 | 30 | ns |
| t_{PLH} | Maximum Propagation Delay LE to Output | | 24 | 40 | ns |
| t_{PHL} | Maximum Propagation Delay Inhibit to Output | | 16 | 30 | ns |
| t_{PLH} | Maximum Propagation Delay Inhibit to Output | | 24 | 40 | ns |
| t_s | Minimum Setup Time, Data to LE | | | 20 | ns |
| t_H | Minimum Hold Time, LE to Data | | | 5 | ns |
| t_W | Minimum Pulse Width, Latch Enable | | | 16 | ns |

AC Electrical Characteristics $V_{CC} = 2.0V - 6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | $T_A = -40$ to $85^\circ C$ | $T_A = -55$ to $125^\circ C$ | Units |
|-----------------------|---|------------|----------|--------------------|-------------------|-----------------------------|------------------------------|-------|
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | | 2.0V | 80 | 175 | 220 | 263 | ns |
| | | | 4.5V | 18 | 35 | 44 | 53 | |
| | | | 6.0V | 16 | 30 | 38 | 45 | |
| t_{PHL} | Maximum Propagation Delay LE to Output | | 2.0V | 80 | 175 | 220 | 263 | ns |
| | | | 4.5V | 19 | 35 | 44 | 53 | |
| | | | 6.0V | 17 | 30 | 38 | 45 | |
| t_{PLH} | Maximum Propagation Delay LE to Output | | 2.0V | 120 | 230 | 290 | 343 | ns |
| | | | 4.5V | 27 | 46 | 58 | 69 | |
| | | | 6.0V | 22 | 39 | 49 | 58 | |
| t_{PHL} | Maximum Propagation Delay Inhibit to Output | | 2.0V | 70 | 175 | 220 | 263 | ns |
| | | | 4.5V | 18 | 35 | 44 | 53 | |
| | | | 6.0V | 16 | 30 | 38 | 45 | |
| t_{PLH} | Maximum Propagation Delay Inhibit to Output | | 2.0V | 120 | 230 | 290 | 343 | ns |
| | | | 4.5V | 27 | 46 | 58 | 69 | |
| | | | 6.0V | 22 | 39 | 49 | 58 | |
| t_s | Minimum Setup Time, Data to LE | | 2.0V | | 100 | 125 | 150 | ns |
| | | | 4.5V | | 20 | 25 | 30 | |
| | | | 6.0V | | 17 | 21 | 25 | |
| t_H | Minimum Hold Time, LE to Data | | 2.0V | | 5 | 5 | 5 | ns |
| | | | 4.5V | | 5 | 5 | 5 | |
| | | | 6.0V | | 5 | 5 | 5 | |
| t_W | Minimum Pulse Width, Latch Enable | | 2.0V | | 80 | 100 | 120 | ns |
| | | | 4.5V | | 16 | 20 | 24 | |
| | | | 6.0V | | 14 | 17 | 20 | |
| C_{PD} | Power Dissipation Capacitance (Note 5) | | | 290 | | | | pF |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

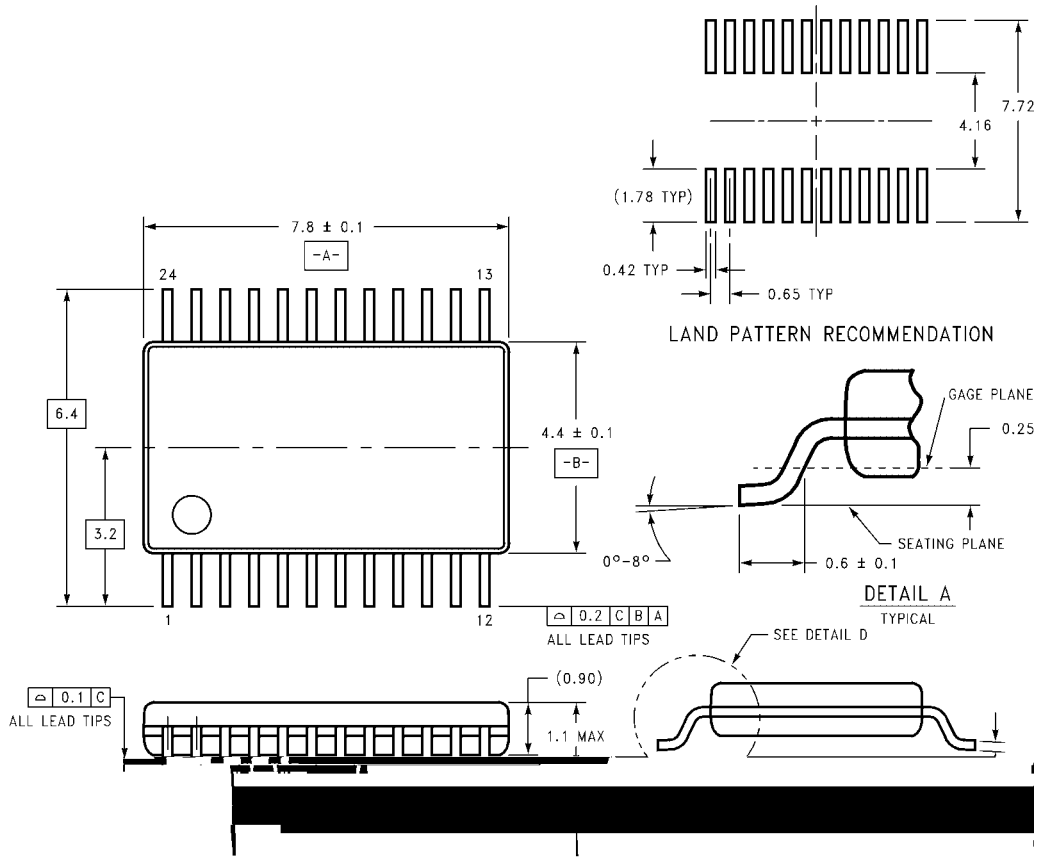
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted



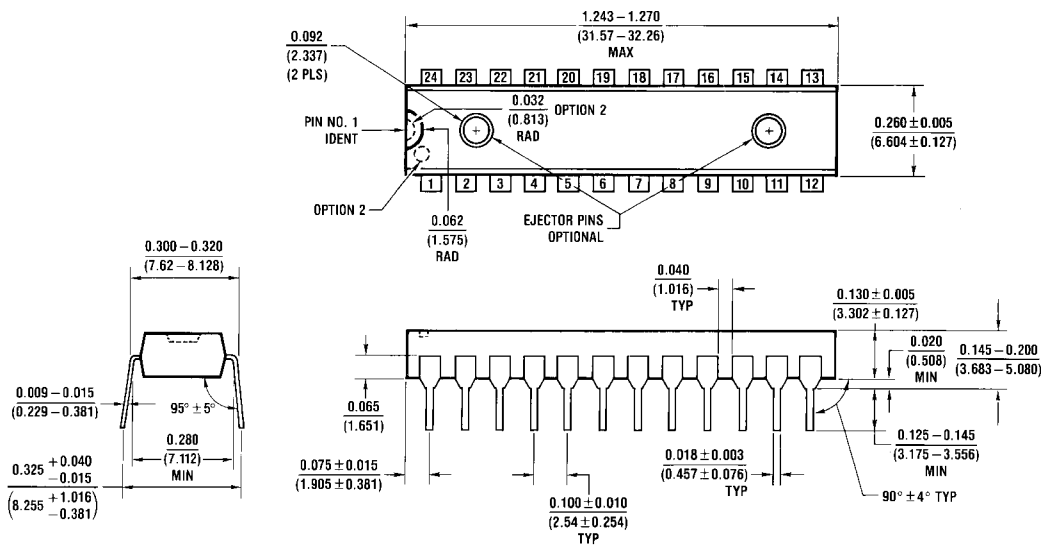
**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
 Package Number N24C**

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