Application Notes for Ceramic Chip Capacitors

General

Ceramic chip capacitors exhibit excellent reliability characteristics providing that proper circuit design techniques and controlled assembly processes are utilized. Due to the ceramic capacitor's crystalline micro-structure these components are susceptible when exposed to excessive thermal or mechanical shock during circuit processing. It should be noted that micro-cracks in ceramic can be difficult to detect with normal post assembly visual and electrical testing and can pose a significant threat to reliable field operation. For this reason it is recommended that the assembly qualification process employ suitable testing to expose the presence of micro-cracking conditions.

Chip Capacitor Attachment

LASERtrim® CAPACITORS - Offered with gold flashed nickel-barrier terminations only. Due to the unique internal construction of the LASERtrim® it is recommended that a conservative reflow temperature profile be used (Fig. 1). Wave soldering is discouraged.

HIGH FREQUENCY CAPACITORS & INDUCTORS - Offered with standard tin plated nickel-barrier terminations compatible with solder flow and reflow processes.

MICROWAVE SINGLE LAYER CAPACITORS - Offered with Titanium-Tungsten/Gold and Titanium-Tungsten/Nickel/Gold thin-film termination as well as legacy Platinum/Palladium/Gold terminations. Please refer to the attachment compatibility table (page 31) specific to these devices.

Soldering Iron

Ceramic capacitor attachment with a soldering iron is discouraged due to the inherent limitations on precisely controlling soldering temperature, heat transfer rate, and time. In the event that a soldering iron must be employed the following precautions are recommended.

- Preheat circuit and capacitors to 150°C
- Never contact the ceramic with the iron tip
- 30 watt iron output (max)
- 280°C tip temperature (max)
- 3.0 mm tip diameter (max)
- Limit soldering time to 5 sec.

Solder Pre-Heat Cycle

Proper preheating is essential to prevent thermal shock cracking of the capacitor. The circuit assembly should be preheated as shown in the recommended profiles at a rate of 1.0 to 2.0°C per second to within 65 to 100°C of the maximum soldering temperature.

SMT Soldering Temperatures

Solders typically utilized in SMT have melting points between 179°C and 188°C. Activation of rosin fluxes occurs at about 200°C. Based on these facts a minimum peak reflow temperature of 205°C to 210°C should be established. A maximum peak reflow temperature of 225°C should be adequate in most circumstances. Many reflow process profiles have peaks ranging from 240°C to 260°C and while ceramic capacitors can withstand soldering temperatures in this range for short durations they should be minimized or avoided whenever possible. Use of PCB mounted multiple thermocouple M.O.L.E. profiling is advised for accurate characterization of circuit heat absorption and maximum temperature conditions.

Reflow Solder

The general term "reflow" refers to several methods used in heating the circuit so that solder paste reflows, or "wetting" of the ceramic capacitor and PCB contacts occurs. These methods include infra-red, convection and radiant heating. The size of the solder fillet may be controlled by varying the amount of solder paste that is screened onto the circuit. Recommended temperature limits for solder reflow are shown in Figure 1 for LASERtrim® and in Figure 2 for standard capacitors.

Vapor Phase

A typical vapor phase soldering process consists of several temperature zones created by saturated vapor from a boiling liquid. As the circuit passes through the zone the vapor condenses on the solder paste, pad, and termination resulting in heat transfer and reflow of the solder paste. Vapor phase reflow produces consistent circuit heating with reflow occurring at a relatively lower temperature that is determined by the known boiling point of the liquid used, typically 215°C. Recommended temperature limits for vapor phase reflow are shown in Figure 3.

Application Notes for Ceramic Chip Capacitors

Solder Wave

Wave soldering is perhaps the most rigorous of surface mount soldering processes due to the steep rise in temperature seen by the circuit as it is immersed in the molten solder wave, typically at 240°C. Recommended temperature limits for wave soldering are shown in Fig. 4.

Cool Down Cycle

After the solder reflows properly the assembly should be allowed to cool gradually at room ambient conditions. Attempts to speed this cooling process or immediate exposure of the circuit to cold cleaning solutions may result in thermal shock cracking of the ceramic capacitor.

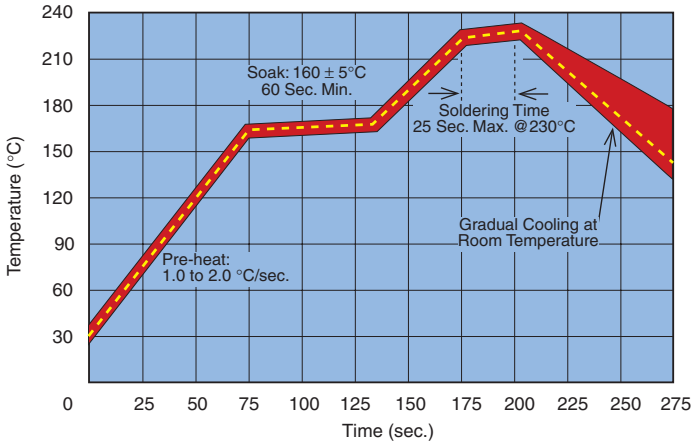

Figure 1: Solder Reflow Profile for LASERtrims®

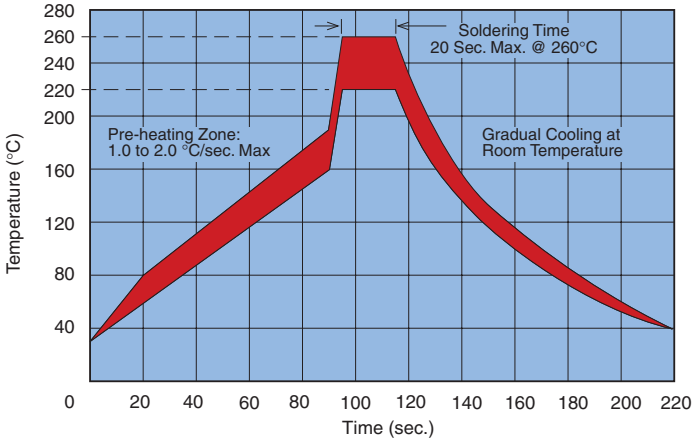

Figure 2: Solder Reflow Profile for MLCCs

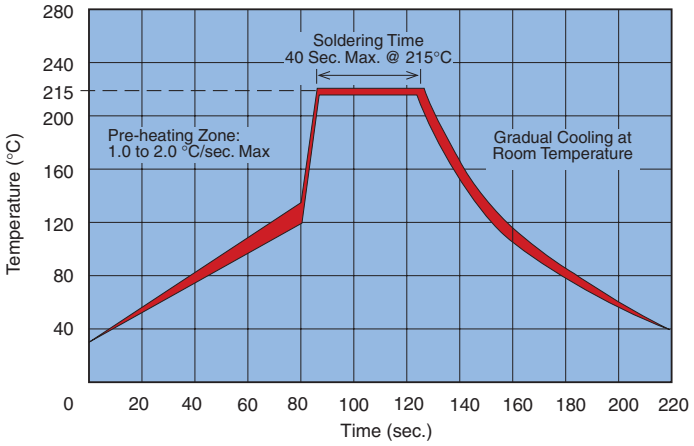

Figure 3: Vapor Phase Profile for MLCCs

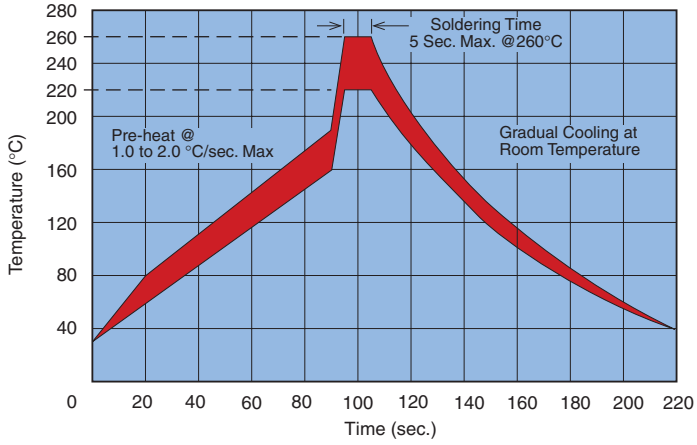

Figure 4: Wave Solder Profile for MLCCs

Please refer to our web site for solder profile information for other component types.

Application Notes for Ceramic Chip Capacitors

Board Layout & Pad Design

Solder pad design, solder application, and component placement are important elements of the soldering process. Excessive transfer of thermal or mechanical stresses to the MLC can result from oversized solder fillets. Nominal pad designs for solder reflow process are listed in Table 1. These guidelines represent a starting point in Printed Circuit Board (PCB) design.

Further information is the Institute for Interconnecting and Packaging Electronic Circuits (www.ipc.org) has developed and published IPC-SM-782A "Surface Mount Design and Land Pattern Standard".

CHIP SIZE		(L) LENGTH		(S) SEPARATION		(W) WIDTH	
		min	max	min	max	min	max
0201	IN	0.008	0.014	0.008	0.012	0.008	0.016
0603	mm	0.20	0.35	0.20	0.30	0.20	0.40
0402	IN	0.014	0.018	0.012	0.020	0.016	0.024
1005	mm	0.35	0.45	0.30	0.50	0.40	0.60
0603	IN	0.024	0.028	0.024	0.031	0.024	0.031
1608	mm	0.60	0.70	0.60	0.80	0.60	0.80
0805	IN	0.024	0.028	0.039	0.047	0.031	0.043
2012	mm	0.60	0.70	1.00	1.20	0.80	1.10
1210	IN	0.039	0.047	0.079	0.094	0.071	0.091
3225	mm	1.00	1.20	2.00	2.40	1.80	2.30

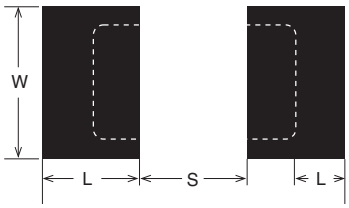

Table 1 Reflow Pad Dimensions

Solder Fillets

To avoid detrimental effects of thermal and mechanical stress it is essential that the solder fillet be limited to 2/3rds of the overall height of the MLC termination as illustrated in the figure below. The solder fillet can be controlled by solder paste deposition and pad design in reflow and vapor phase processes and by pad design and use of hot air knives in the wave process.

Tomb Stoning / Chip Movement

Tomb-stoning or draw bridging is illustrated in the figure below. Tomb-stoning or other undesirable chip movements may result if unequal surface tension forces exist as the molten solder wets the MLC terminations and mounting pads. This tendency can be minimized by insuring that all factors at both solder joints are equal, namely; pad size, solder mass, termination size, component position and heating. Tomb-stoning is easily avoided through proper design, material selection and proofing of the process.