

Ceramic Disc Capacitor, CH



Mechanical

Available lead code: (Unit : mm)

Lead Type	P/N (13-17) Digits	Pitch (F)	Lead Length (L)	Available Rated Voltage	Packing	Lead Configuration
Lead Style : B Straight Long Lead	B20C7	7.5 ± 1	20 Min.	1 KV	Bulk	

※ Lead diameter : $\phi = 0.6 \pm 0.06$ mm

※ e (Coating extension on leads):

For straight lead style: 2 mm maximum when the rated voltage is 1 KV V dc

Capacitance Value vs. Rate Voltage, Product Diameter :

TC	CH (Class I, Temperature : -25°C to +85°C, TCC: 0 ±60 ppm/°C)
Rate Voltage	1 KV
D ϕ	050
D Maximum (mm)	6
T Maximum (mm)	4.5
10	100

Packaging

Packaging Style

Bulk : 1,000 pieces / bag

Specification and Test Method :

Scope : This specification applies to temperature compensating ceramic disc capacitor

Test conditions : Unless otherwise specified, all tests shall be operated at the standard test conditions of temperature 5°C to 35°C and relative humidity 45% to 85%. When fails a test, retest be operated at the conditions of temperature 25°C ± 2°C, relative humidity of 60% to 70% and barometric pressure 860 to 1,060 mbar

Handle procedure : To avoid unexpected testing results from occurring, the tested capacitor must be kept at room temperature for at least 30 minutes and completely discharged

Ceramic Disc Capacitor, CH



Test Items:

Item	Post-Test Requirements		Testing Procedure
Appearance Structure Size	No Abnormalities		As section 3
Withstand Voltage	Between Terminals : No Abnormalities		1 KV and Above : 200% Rated Voltage With 50 mA Maximum Charging Current for 1 to 5 s
	Between Terminal and Enclosure : No Abnormalities		Small Metallic Balls With 1 mm Diameters Shall be Put on a Vessel and The Test Capacitor Shall be Submerged Except 2 mm From The Top of its Component Body. The Test Voltage Shall be Applied Between The Short-Circuited Terminals And The Metallic Balls. (Apply 1.3 KV dc of Rated Voltage Between Terminals and Enclosure for 1 to 5 s)
Insulation Resistance	10,000 M Ω Min.		Insulation Resistance Shall be Measured at 60 \pm 5 Seconds After Applied Voltage (Rated) Rated Voltage : 500 V and Above = 500 V
Capacitance	Tolerance : J : \pm 5%		Testing Frequency : 1 MHz \pm 20% Testing Voltage : 1 V rms
Operating Temperature Range	-25°C to +125°C		
Q Factor	30 pF and Above	Q \geq 1,000	As Above Stipulation of Capacitance
	Below 30 pF	Q \geq 400 + 20 \times C	
Temperature Characteristic	Temperature Coefficient : CH : 0 \pm 60 PPM/ $^{\circ}$ C		According to Step 1 to 5 In Order, Measured Capacitance When Temperature Reach Balance and Temperature Coefficient Shall be Calculated on The Following Formula : PPM/ $^{\circ}$ C = (C2 - C1) \times 10E6 / C1 (T2-T1) STEP 1, 3, 5 : 25°C STEP 2 : -25°C STEP 4 : 85°C Note : C1 = Capacitance as Step 3 C2 = Capacitance as Step 2 or 4 T1 = Temperature as Step 3 T2 = Temperature as Step 2 or 4
	Capacitance Tolerance : Within \pm 0.2% or \pm 0.05 pF, Whichever is Large		According to Above Step 1,3 and 5, Capacitance Tolerance Shall be Calculated on the Following Formula : Δ C% = (G - S) / C1 Note : G = Greatest Capacitance as Testing Result of Step 1,3 and 5 S = Least Capacitance as Testing Result of Step 1, 3 and 5 C1 = Capacitance as Step 3
Terminal Strength	Tensile Strength : No Breakdown		Wire Diameter 0.5 mm Loading Weight 0.5 Kgs, for 10 \pm 1 s Wire Diameter .0.6 mm Loading Weight 1 Kgs, for 10 \pm 1 s
	Bending Strength : No Breakdown		Wire Diameter 0.5 mm, Loading Weight 0.25 Kgs Wire Diameter 0.6 mm, Loading Weight 0.5 Kgs (Bending Back and Forth 90° Twice)

Ceramic Disc Capacitor, CH



Test Items:

Item	Post-Test Requirements	Testing Procedure
Soldering Heat Resistance	Appearance : No Abnormalities	Lead Wire or Terminals Shall be Immersed Up to 2 mm from Body (A) Body Diameter ≥ 5 mm : Into The Molten Solder of Which Temperature : $260 (+ 5 / - 0)^{\circ}\text{C}$ for 3 ± 0.5 s (B) Body Diameter ≥ 5 mm: Into The Molten Solder of Which Temperature $260 (+5 / -0)^{\circ}\text{C}$ for 5 to 10 s Then Leave at Standard Test Conditions for 1 to 2 Hours, Then Measured * When Soldering Capacitor With a Soldering Iron, it Should be Performed in Following Conditions. Temperature of Iron-Tip : 350 to 400°C Soldering Iron Wattage : 50 W Maximum Soldering Time : 3.5 seconds Maximum
	Capacitance Change : Within $\pm 2.5\%$ or ± 0.25 pF, Whichever is Large	
	Withstand Voltage : (Between Terminals) No Abnormalities	
Humidity Characteristic	Appearance : No Abnormalities	Capacitors Shall be Subjected to a Relative Humidity of 90 to 95% at $40 \pm 2^{\circ}\text{C}$ for 500 (+ 24 / - 0) Hours, Then Dried for 1 to 2 Hours and Measured
	Capacitance Change : CH : Within $\pm 5\%$ or ± 0.5 pF, Whichever is Large	
	Q Factor : CH : Less than 10 pF = $> Q \geq 200 + 10 \times C$ More than 10 pF and Less than 30 pF = $> Q \geq 275 + 5 \times C/2$ More than 30 pF = $> Q \geq 350$	
	Insulation Resistance : 1,000 M Ω Min.	
Humidity Loading	Appearance : No Abnormalities	Capacitors Shall be Subjected to a Relative Humidity of 90 to 95% at $40 \pm 2^{\circ}\text{C}$ for 500 (+24 / -0) Hours with Rated Voltage Applied (Less than 50 mA), then Dried for 1 to 2 Hours and Measured
	Capacitance Change : CH : Within $\pm 7.5\%$ or ± 0.75 pF, Whichever is Large	
	Q Factor :CH : Less than 30 pF = $> Q \geq 100 + 10 \times C/3$ More than 30 pF = $> Q \geq 200$	
	Insulation Resistance : 500 M Ω Min.	
High Temperature Loading	Appearance : No Abnormalities	Capacitors Shall be Subjected to a Test of : (A) Below 1 KV: 200% Rated Voltage with 50 mA Maximum (B) 1 KV and above: 150% Rated Voltage with 50 mA Maximum for 1,000 (+48 / -0) Hours at $85^{\circ}\text{C} \pm 2^{\circ}\text{C}$ (for CH and SL) and then Dried for 1 to 2 Hours and Measured
	Capacitance Change : CH : Within $\pm 3\%$ or ± 0.3 pF, Whichever is Large	
	Q Factor : CH : Less than 10 pF = $> Q \geq 200 + 10 \times C$ More than 10 pF and Less than 30 pF = $> Q \geq 275 + 5 \times C/2$ More than 30 pF = $> Q \geq 350$	
	Insulation Resistance : 1,000 M Ω Min.	
Temperature Cycling	Appearance : No Abnormalities	Capacitors Shall be Subjected to: $-25 \pm 3^{\circ}\text{C}$ (30 ± 3 min) $\rightarrow 25^{\circ}\text{C}$ (3 min) $\rightarrow 85 \pm 3^{\circ}\text{C}$ (30 ± 3 min) $\rightarrow 25^{\circ}\text{C}$ (3 min) for 5 Cycle
	Capacitance Change : Within $\pm 5\%$ or ± 0.5 pF, Whichever is Large	
	DF C < 30 pF : $Q \geq 275 + (5/2) C$ C ≥ 30 pF : $Q \geq 350$	
	Insulation Resistance : 1,000 M Ω Min.	

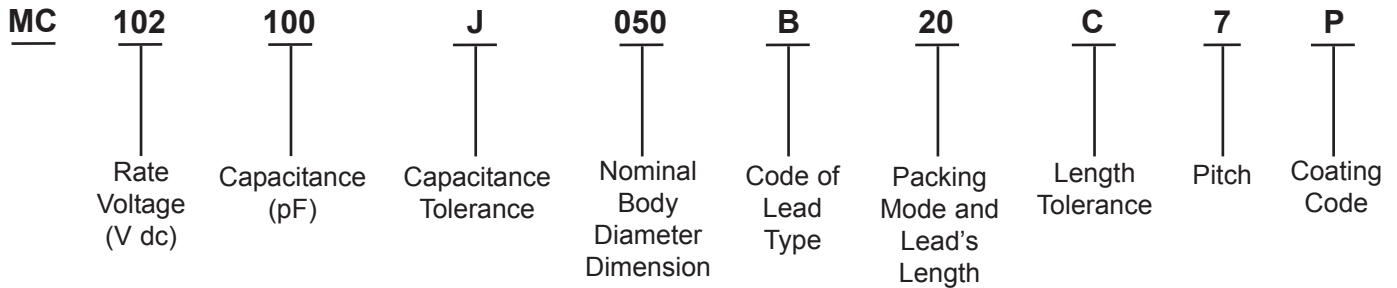
Ceramic Disc Capacitor, CH



Part Number Table

Description	Part Number
Ceramic Disc Capacitor, CH	MC102100J050B20C7P

Part Number Explanation:



Rated Voltage (V dc)	: 102 = 1,000 V
Capacitance (pF)	: 100 = 100
Capacitance Tolerance	: J = $\pm 5\%$ (for above 10pF)
Nominal Body Diameter Dimension	: 050 = 5
Code of Lead Type	: Refer to Mechanical
Packing Mode and Lead's Length L	: 20 = 20 mm
Length Tolerance	: C = Min.
Pitch	: 7 = 7.5 ± 1 mm
Coating Code	: P = Phenolic resin -Pb free, voltage ≤ 1 kV

Important Notice : This data sheet and its contents (the "Information") belong to the members of the Premier Farnell group of companies (the "Group") or are licensed to it. No licence is granted for the use of it other than for information purposes in connection with the products to which it relates. No licence of any intellectual property rights is granted. The Information is subject to change without notice and replaces all data sheets previously supplied. The Information supplied is believed to be accurate but the Group assumes no responsibility for its accuracy or completeness, any error in or omission from it or for any use made of it. Users of this data sheet should check for themselves the Information and the suitability of the products for their purpose and not make any assumptions based on information included or omitted. Liability for loss or damage resulting from any reliance on the Information or use of it (including liability resulting from negligence or where the Group was aware of the possibility of such loss or damage arising) is excluded. This will not operate to limit or restrict the Group's liability for death or personal injury resulting from its negligence. Multicomp is the registered trademark of the Group. © Premier Farnell plc 2011.