

Specification

BTHQ 21605VSS-SRE (IC-ST7066)

Doc. No.: BTHQ 21605VSS-19

Version April 2008

Supplied by:

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DOCUMENT REVISION HISTORY 1:

REVISION FROM TO	DATE		CHANGED BY	CHECKED BY
A	2008.04.14	First Release Based on a.) VL-QUA-012A, REV. S, 2008.02.18. (According to VL-QUA-012A, LCD size is small because Unit Per Laminate=35 which is more than 6pcs/Laminate.)	CHEN HUI JUAN	FENG NAN

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**Specification
of
LCD Module Type
Item No.: BTHQ 21605VSS-19**

1. General Description

- 16 characters (5 x 8 dots) x 2 lines STN Positive Yellow Reflective LCD Character Module.
- Viewing Angle: 6 o'clock direction.
- Driving scheme: 1/16 duty, 1/5 bias.
- 'SITRONIX' ST7066U-0A (Die form) LCD Controller & Driver or equivalent.
- 'SITRONIX' ST7065C (Die form) LCD Segment Drivers or equivalent.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	84.0(W) x 44.0(H) x 10.0 MAX.(D)	mm
Viewing area	61.0(W) x 15.8(H)	mm
Display format	16 characters x 2 lines	-
Character size	2.95(W) x 5.55(H) (5 x 8 dots)	mm
Character spacing	0.60(W) x 0.40(H)	mm
Character pitch	3.55(W) x 5.95(H)	mm
Dot size	0.578(W) x 0.681(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.593(W) x 0.696(H)	mm
Weight	Approx.: 32.5	grams

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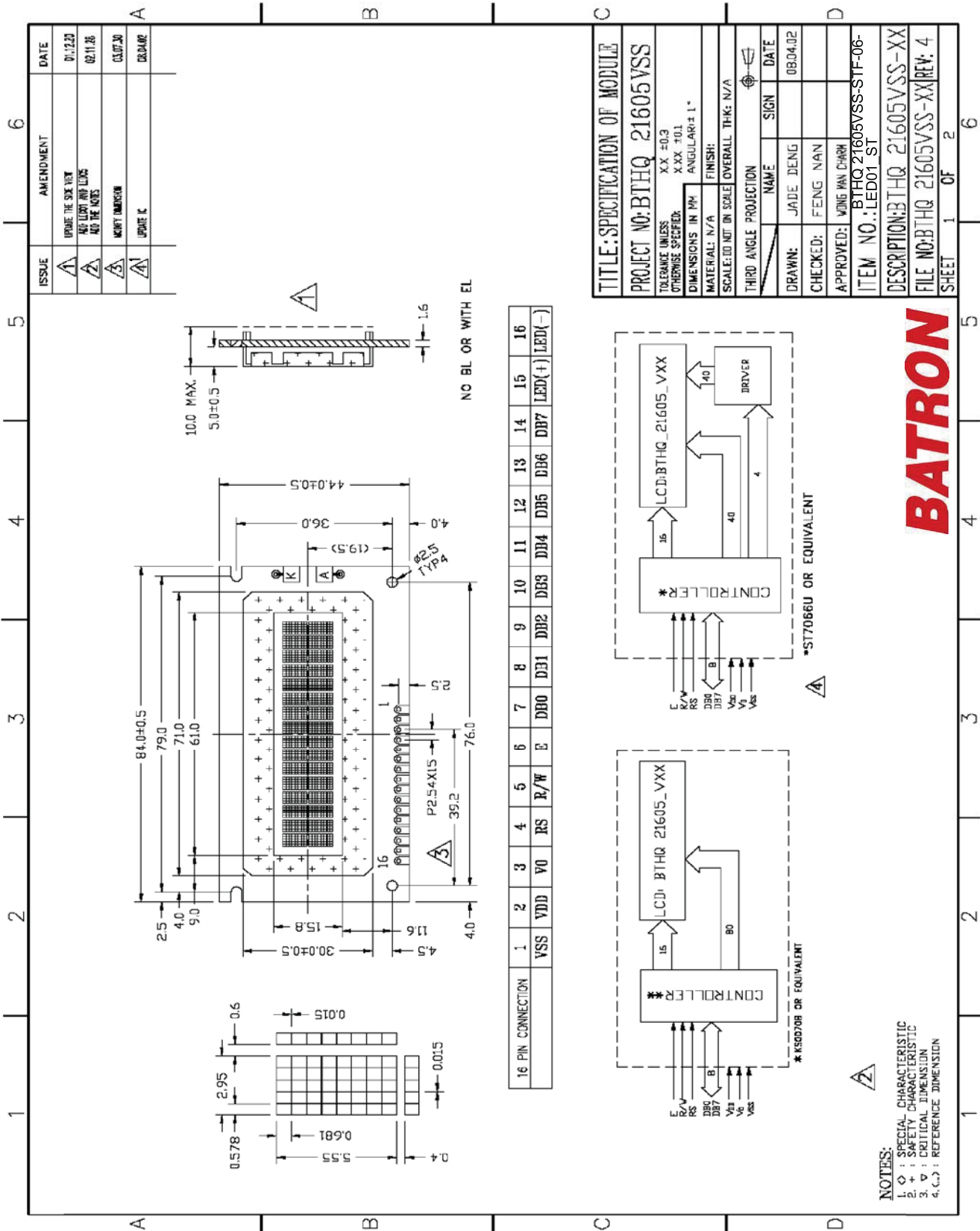
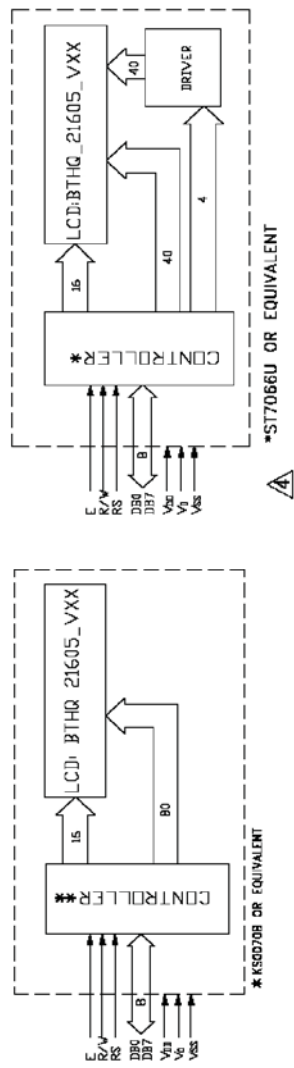


Figure 1: Outline Drawing

ISSUE		AMENDMENT		DATE	
1	UPDATE THE SIZE VIEW			01.220	
2	ADD FLUORESCENT MARKS AND TO THE NOTES			02.11.26	
3	MARKET DIMENSION			03.07.20	
4	UPDATE IC			08.04.02	

TITLE: SPECIFICATION OF MODULE					
PROJECT NO: BTHQ 21605VSS					
TOLERANCE UNLESS OTHERWISE SPECIFIED:	XX ±0.3				
	XX FULL				
DIMENSIONS IN MM:	ANGULAR ±1°				
MATERIAL:	N/A	FINISH:			
SCALE: 1:1 NOT IN SCALE OVERALL THK: N/A					
THIRD ANGLE PROJECTION		NAME		SIGN	DATE
		JADE DENG			08.04.02
DRAWN:		FENG NAN			
CHECKED:		WONG HAN CHAM			
APPROVED:		ITEM NO.: BTHQ 21605VSS-STF-06-			
		DESCRIPTION: BTHQ 21605VSS-XX			
		FILE NO: BTHQ 21605VSS-XX REV: 4			
SHEET 1		OF 2		6	



- NOTES:
1. ◊ : SPECIAL CHARACTERISTIC
 2. + : SAFETY CHARACTERISTIC
 3. ∇ : CRITICAL DIMENSION
 4. (L) : REFERENCE DIMENSION

BATRON

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3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	VDD+0.3	VDD-10.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)(Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C <50%RH for 40°C <Ta ≤ Maximum operating temperature				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

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4. Interface signalsTable 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: “High” for Data register (for read and write) “Low” for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: “High” for Read mode. “Low” for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. These pins are not used during 4-bit operation.
8	DB1	
9	DB2	
10	DB3	
11	DB4	Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. DB7 can be used as a busy flag.
12	DB5	
13	DB6	
14	DB7	
15	LED(+)	No connection.
16	LED(-)	No connection.

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5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	Ta=0°C, Character mode, VDD =5.0V, Note 1	-	4.7	-	V
		Ta=+25°C, Character mode, VDD=5.0V, Note 1	4.1	4.6	5.1	V
		Ta=+50°C, Character mode, VDD =5.0V, Note 1	-	4.4	-	V
Input signal voltage for E,DB0-DB7,R/W,RS	V _{IHI}	“High” level	0.7 VDD	-	VDD	V
	V _{ILI}	“Low” level	-0.3	-	0.6	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.1	1.7	mA
		Checkerboard mode, Note 1		1.2	1.8	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.2	0.3	mA
		Checkerboard mode, Note 1	-	0.2	0.3	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

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5.2 Timing Specifications

At $T_a = 0\text{ }^{\circ}\text{C}$ To $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 6

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<i>Write Mode (Writing data from MPU to ST7066U)</i>						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
<i>Read Mode (Reading Data from ST7066U to MPU)</i>						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

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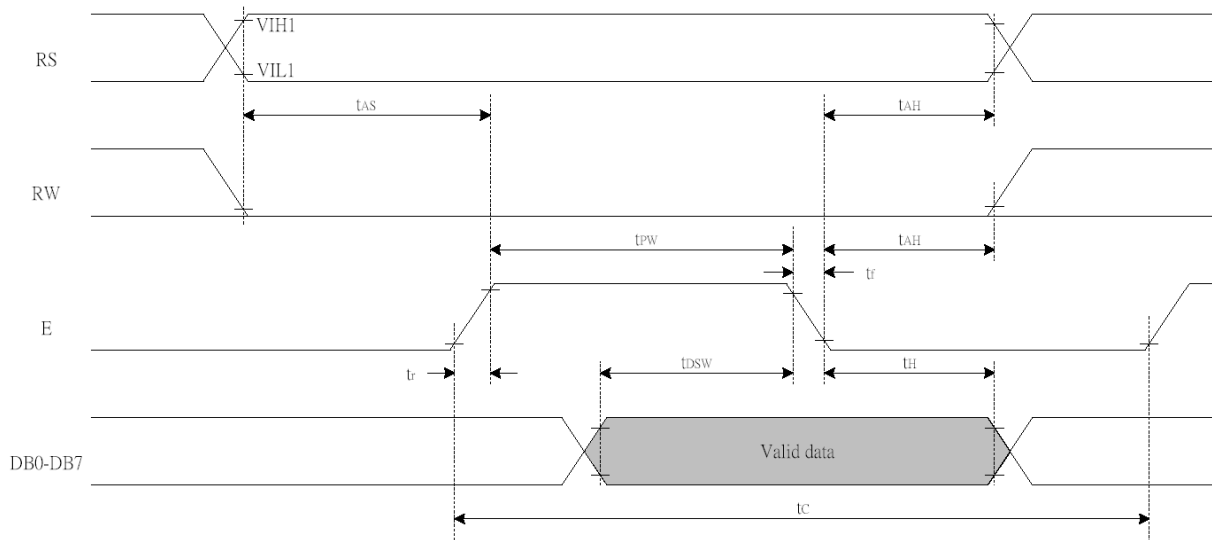


Figure 2: Writing data from MPU to ST7066U

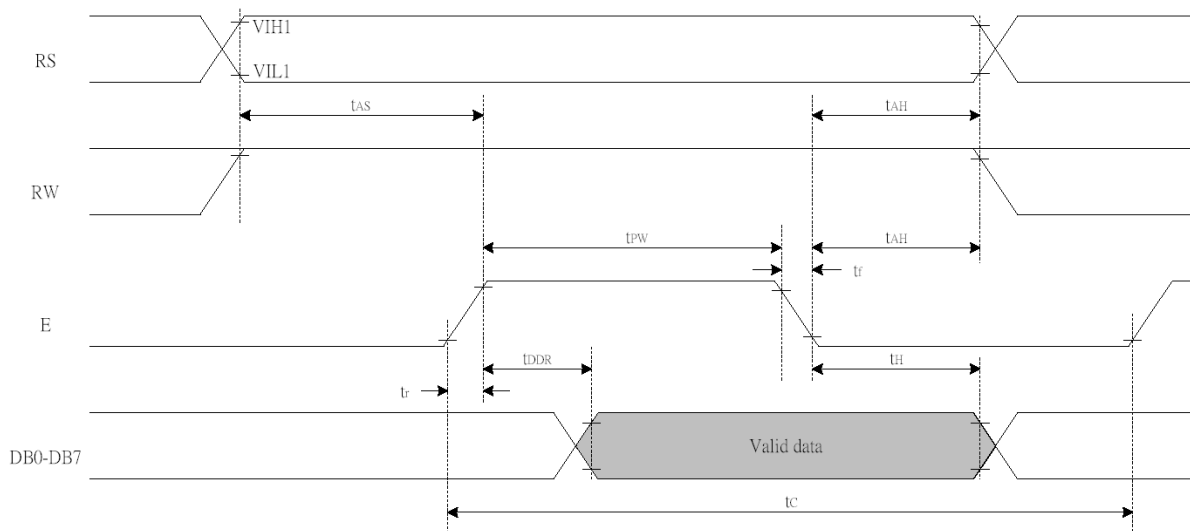


Figure 3: Reading data from ST7066U to MPU

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5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

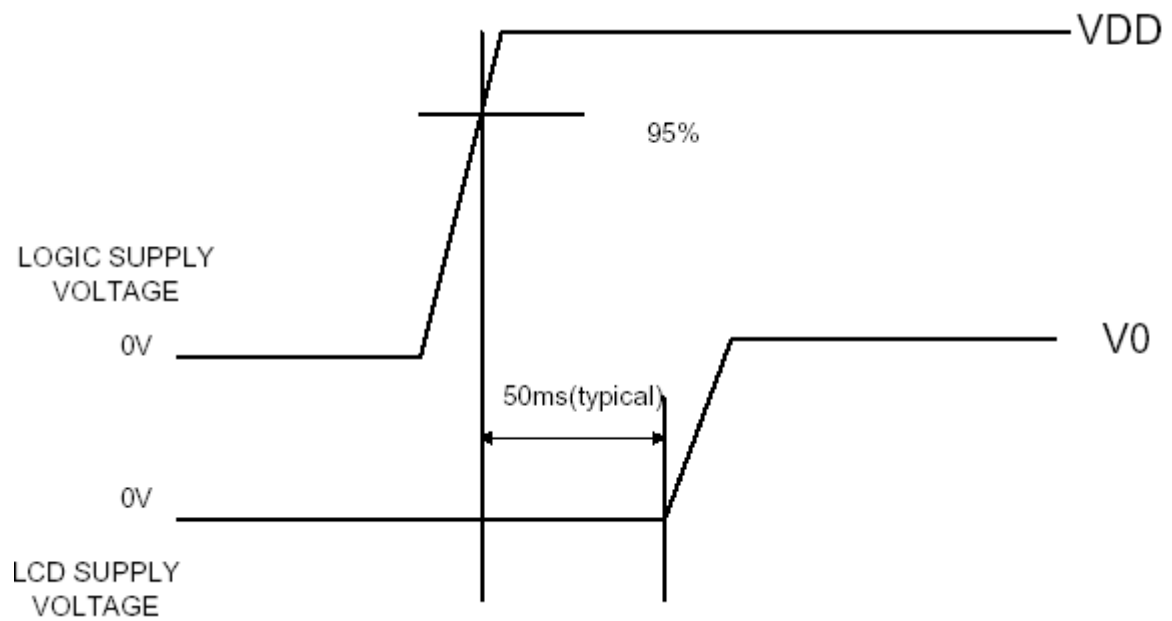


Figure 4: Timing diagram of VDD against V0.

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6. CGROM Character Code Table (ST7066U-0A)

NO. 7066-0A

b7-b4 b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)			0	1	2	3	4				5	6	7	8	9
0001	(2)	!	0	1	A	0	a	9			.	7	7	4	3	q
0010	(3)	"	2	B	R	b	r				7	7	7	7	p	8
0011	(4)	#	3	C	S	c	s				7	7	7	7	e	8
0100	(5)	*	4	D	T	d	t				7	7	7	7	p	8
0101	(6)	%	5	E	U	e	u				.	7	7	7	7	0
0110	(7)	&	6	F	V	f	v				7	7	7	7	p	8
0111	(8)	'	7	G	W	g	w				7	7	7	7	g	8
1000	(1)	(8	H	X	h	x				7	7	7	7	7	8
1001	(2))	9	I	Y	i	y				7	7	7	7	7	8
1010	(3)	*	:	J	Z	j	z				7	7	7	7	7	8
1011	(4)	+	;	K	0	k	0				7	7	7	7	7	8
1100	(5)	.	<	L	*	l	l				7	7	7	7	7	8
1101	(6)	-	=	M	7	m	7				7	7	7	7	7	8
1110	(7)	,	>	N	^	n	*				7	7	7	7	7	8
1111	(8)	/	?	O	_	o	*				7	7	7	7	7	8

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7. LCD Cosmetic Conditions

- a.) Reference document follow VL-QUA-012A.
- b.) LCD size of the product is small.

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