Preliminary Information

Four Channel Programmable DC-DC System Power Manager

FEATURES & APPLICATIONS

- **Digital programming of all major parameters via I^2C interface and non-volatile memory**
  - **Output voltage set point**
  - **Output power-up/down sequencing**
  - **Digital soft-start and output slew rate**
  - **Input/Battery voltage monitoring**
  - **UV/OV monitoring of all outputs**
  - **Enable/Disable outputs independently**
- **Four output channels**
  - **Three synchronous step-down (buck) channels**
  - **One step-up (boost) channel**
- **User friendly Graphical User Interface (GUI)**
- **+2.7V to +6.0V Input range**
- **Highly accurate output voltage (<0.5%) with Active DC Output Control (ADOC™) technology**
- **Undervoltage Lockout (UVLO) with hysteresis**
- **800 kHz operating frequency**
- **Four Phase PWM with Phase Locked Loop (PLL)**
- **100% Maximum Duty Cycle for Buck channels**
- **0% Duty Cycle option for boost controller**
- **96 bytes of user configurable nonvolatile memory**

Applications

- **Digital camcorders/still cameras**
- **Portable DVD/MP3/GPS**
- **Camera/smart phones**
- **TFT/LCD Displays/Monitors/TV's**
- **Mobile Computing/PDA's**
- **Consumer battery-operated equipment**

INTRODUCTION

The SMB111 is a highly integrated and flexible four-channel power manager designed for use in a wide range of portable applications. The built-in digital programmability allows system designers to custom tailor the device to suit almost any multi-channel power supply application from digital camcorders to mobile phones. Complete with a user friendly GUI, all programmable settings including output voltages and input/output voltage monitoring can be customized with ease.

The SMB111 integrates all the essential blocks required to implement a complete four-channel power subsystem including three synchronous step-down "buck" controllers and one step-up "boost" controller. Additionally sophisticated power control/monitoring functions required by complex systems are built-in. These include digitally programmable output voltage set point, power-up/down sequencing, enable/disable, margining and UV/OV/input/output monitoring on all channels.

The integration of features and built-in flexibility of the SMB111 allows the system designer to create a "platform solution" that can be easily modified via software without major hardware changes. Combined with the re-programmability of the SMB111 this facilitates rapid design cycles and proliferation from a base design to future generations of product.

The SMB111 is suited to battery-powered applications with an input range of +2.7V to +6.0V. Output voltages are extremely accurate (<0.5%) employing proprietary ADOC™ technology. Communication is via the industry standard I^2C bus. All user-programmed settings are stored in non-volatile EEPROM of which 96 bytes may be used for general-purpose memory applications. The commercial operating temperature range is 0°C to +70°C, and the industrial range is -40°C to 85°C. The available package is a lead-free, RoHS compliant, 5x5 32-pin QFN.

SIMPLIFIED APPLICATIONS DRAWING

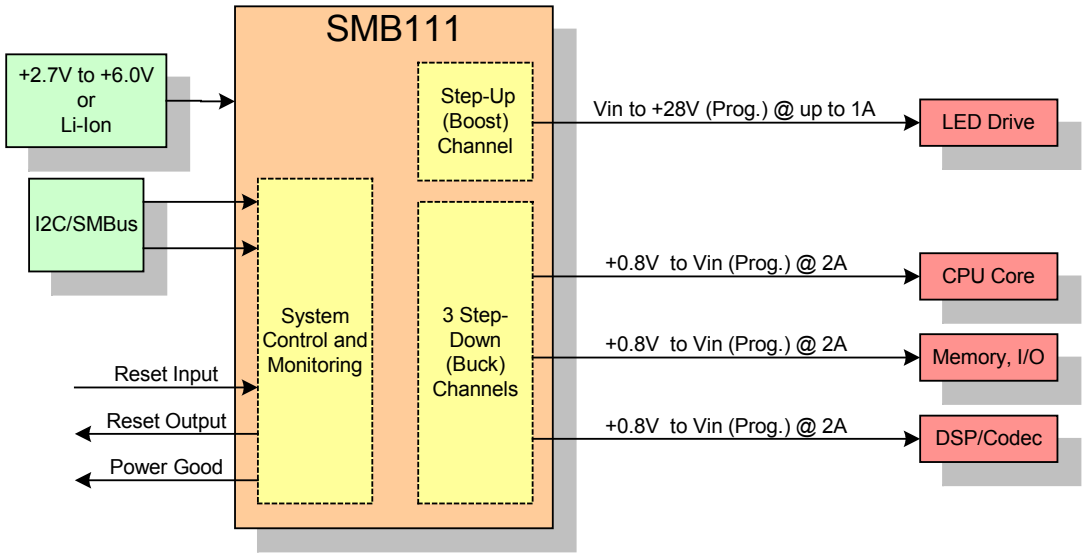

Figure 1: Applications schematic featuring the SMB111 four-channel, programmable DC-DC controller
Note: This is an applications example only. Some pins, components and values are not shown.

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GENERAL DESCRIPTION

The SMB111 is a fully programmable controller that monitors, margins, and cascade sequences. It has four voltage outputs, consisting of: three synchronous step-down “buck” controllers and one step-up “boost” controller.

The SMB111 is capable of power-on/off cascade sequencing where each channel can be assigned one of four unique sequence positions. During sequencing each channel in a given sequence position is guaranteed to reach its programmed output voltage before the channel(s) occupying the next sequence position initiate their respective soft-start sequence. A unique programmable delay exists between each power on/off sequence position. In addition to power on/off sequencing all supplies can be powered on/off individually through an I^2C command or by assertion of one of two enable pins.

Each output voltage is monitored for under-voltage and over-voltage (UV/OV) conditions, using a comparator-based circuit where the output voltage is compared against an internal programmable reference. An additional feature of the output voltage monitoring is a programmable glitch filter capable of digitally filtering a transient OV/UV fault condition from a true system error. When a fault is detected for a period in excess of the glitch filter, all supplies may be sequenced down or immediately disabled and one of two output status pins can be asserted. The current system status is always accessible via internal registers containing the status of all four channels.

The SMB111 possesses an Undervoltage Lockout (UVLO) circuit to ensure the SMB111 will not power up until the battery voltage has reached a safe operating voltage. The UVLO function exhibits hysteresis, ensuring that noise or a brown out voltage on the on the supply rail does not inadvertently a system failure.

The SMB111 uses a fixed 800kHz Pulse Width Modulation (PWM) control circuit. A type three voltage mode compensation network is used offering a cost effective solution without compromising the transient response. By utilizing external n and p–type MOSFET transistors the efficiency and load current can be customized to fit a wide array of system requirements.

The SMB111 contains three buck outputs capable of producing an output voltage less than the input voltage. Each buck output voltage is set by an internal resistor divider and a programmable voltage reference. The integrated resistor divider eliminates the cost and space necessary for external components and has several programmable values. Through the programmability of the reference and the resistor divider, practically any output voltage less than the battery can be produced without the need to change external components.

The SMB111 contains one boost output capable of producing an output voltage greater than the input voltage. The boost topology is asynchronous, using a rectifying Schottky diode and eliminating the need for an additional external MOSFET driver. An external p-channel sequencing MOSFET’s accompanies the boost channel in order to isolate the switching MOSFET from the battery when disabled.

The SMB111 provides margining control over all of its output voltages. Through an I^2C command, all outputs can be margined to any voltage setting within the nominal output voltage rage. Margining creates three pre-programmed settings that each channel can be set to via an I^2C command. Margining is ideal when used with the boost channel configured as an LED driver where margining provides three brightness settings.

In addition, each output is slew rate limited by soft-start circuitry that is user programmable and requires no external capacitors.

All programmable settings on the SMB111 are stored in non-volatile registers and are easily accessed and modified over an industry standard I^2C serial bus. For fastest prototype development times Summit offers an evaluation card and a Graphical User Interface (GUI).

TYPICAL APPLICATION

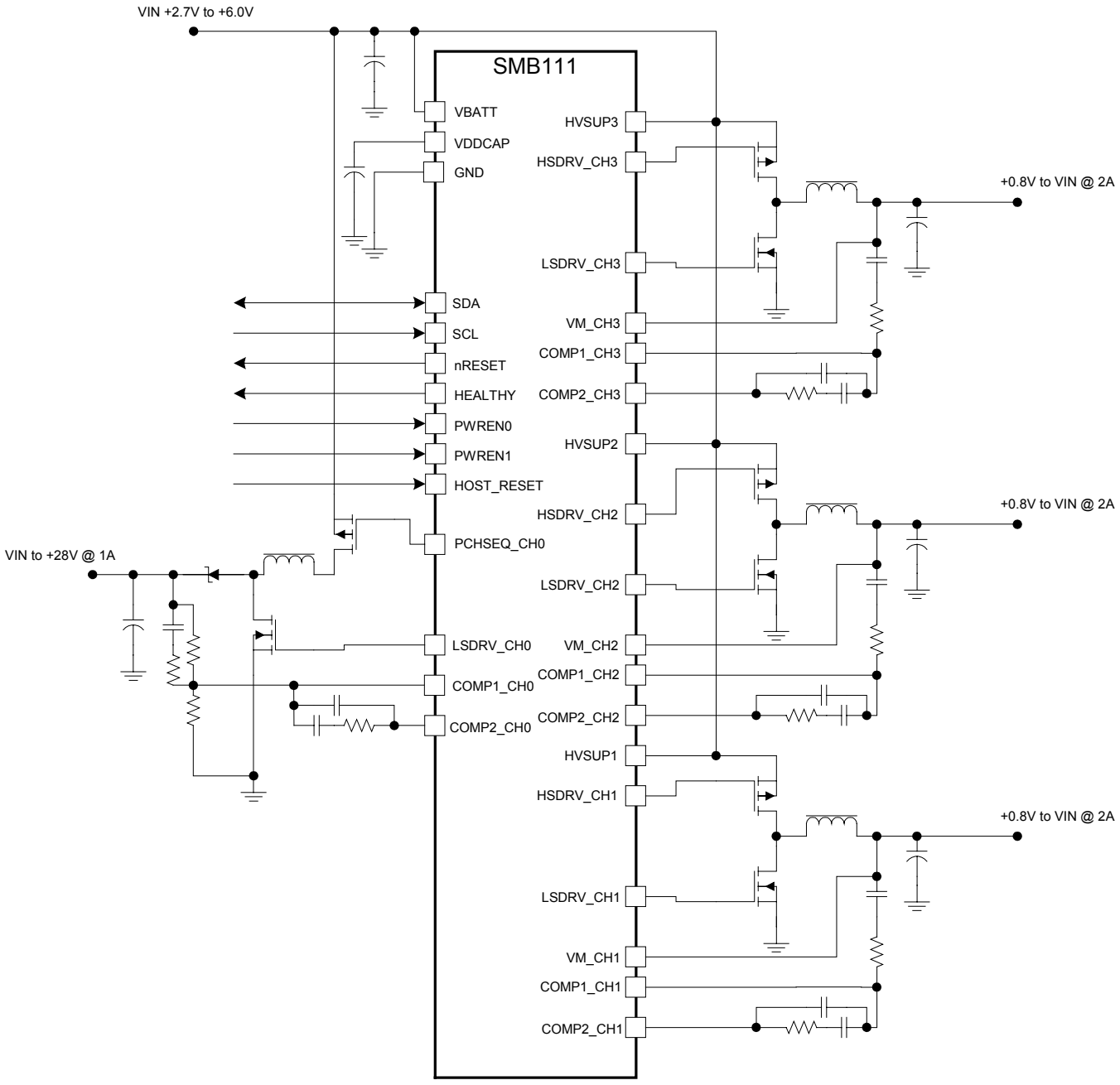
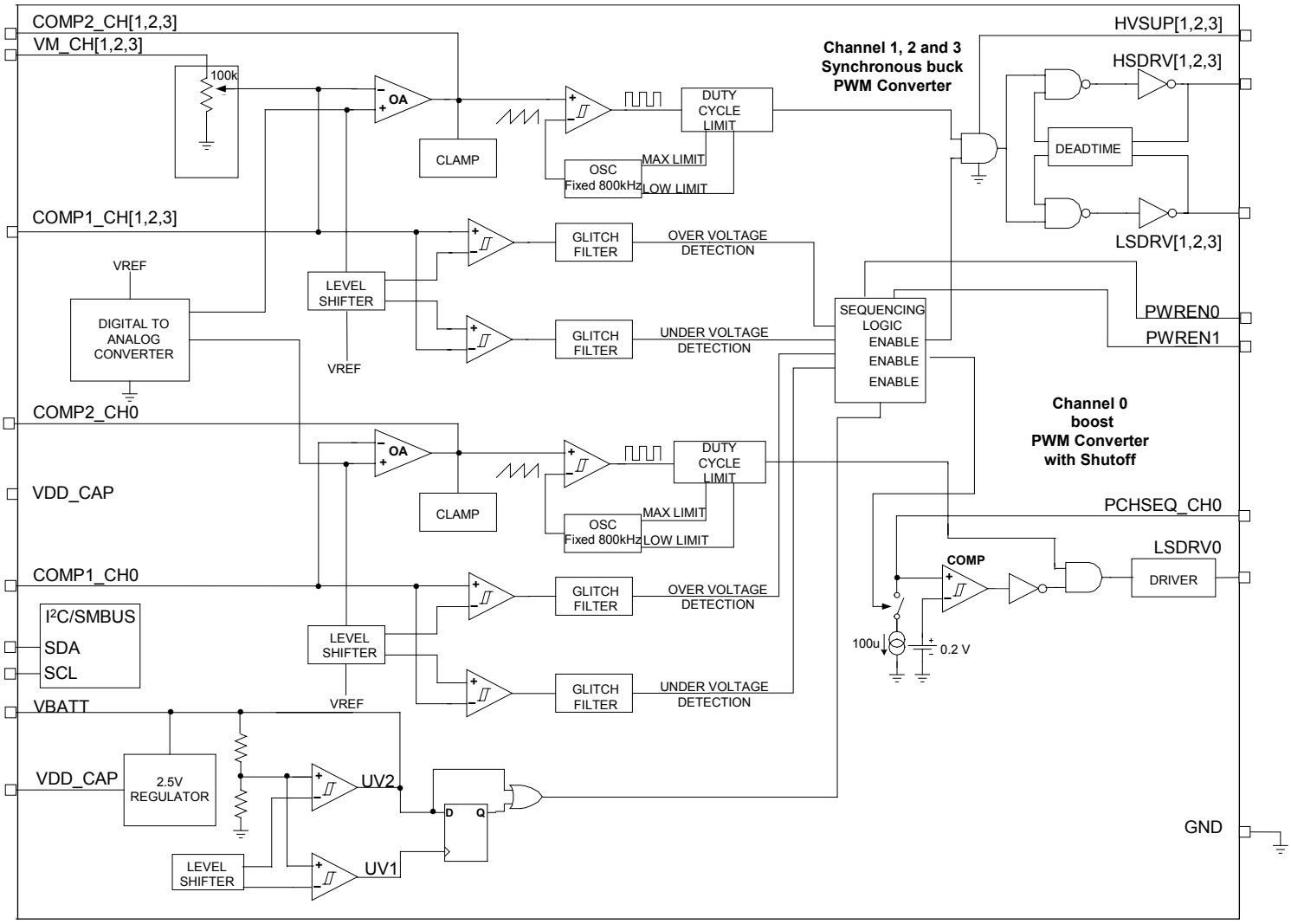


Figure 2 – Typical application schematic showing external circuitry necessary to configure the SMB111 channels as step-up and step-down outputs.

INTERNAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Number	Pin Type	Pin Name	Pin Description
1	OUT	LSDRV_CH3	The LSDRV_CH3 (Channel 3 Low-side Driver) pin is the lower switching node of the channel 3 synchronous buck controller. Attaches to the gate of n-channel MOSFET.
2	PWR	HVSUP3	Supply for Channel 3 buck driver.
3	OUT	HSDRV_CH3	The HSDRV_CH3 (Channel 3 High-side Driver) pin is the upper switching node of the channel 3 synchronous buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH3 and assertion of LSDRV_CH3 to prevent excessive current flow during switching.
4	OUT	HEALTHY	The HEALTHY pin is an open drain output. High when all enabled output supplies are within the programmed levels. HEALTHY will ignore any disabled supply. There is a programmable glitch filter on the under-voltage and over-voltage sensors so that short transients outside of the limits will be ignored by HEALTHY. When used this pin should be pulled high by an external pull-up resistor.
5	IN	COMP1_CH3	The COMP1_CH3 (Channel 3 primary Compensation) pin is the primary compensation input of the channel 3 buck controller. Each pin is internally connected to a programmable resistor divider.
6	IN	COMP2_CH3	The COMP2_CH3 (Channel 3 secondary Compensation) pin is the secondary compensation input of the channel 3 buck controller.
7	IN	VM_CH3	The VM_CH3 (Channel 3 Voltage Monitor) pin connects the channel 3 controller output. Internally the VM_CH3 pin connects to an internal programmable resistor divider.
8	I/O	SDA	SDA (Serial Data) is an open drain bi-directional pin used as the I^2C data line. SDA must be tied high through a pull-up resistor.
9	IN	SCL	SCL (Serial Clock) is an open drain input pin used as the I^2C clock line. SCL must be tied high through a pull-up resistor.
10	IN	HOST_RESET	The HOST_RESET pin is an active high reset input. When this pin is asserted high, the nRESET output will immediately go low. When HOST_RESET is brought low, nRESET will go high after a programmed reset delay.
11	CAP	VDD_CAP	The VDD_CAP (VBATT Capacitor) pin is an external capacitor input used to filter the internal supply.
12	PWR	VBATT	Power supply to part, 2.7V to 6.0V range.
13	OUT	PCHSEQ_CH0	The PCHSEQ_CH0 (Channel 0 Sequence) pin is attached to an external p-channel MOSFET and is used to enable the corresponding channel 0 boost controller. PCHSEQ_CH0 uses an internal 100μA current sink for sequencing. This pin should be pulled high through a parallel RC connection.
14	IN	COMP1_CH0	The COMP1_CH0 (Channel 0 primary Compensation) pin is the primary compensation input of the channel 0 boost controller.

PIN DESCRIPTIONS			
Pin Number	**Pin Type**	**Pin Name**	**Pin Description**
15	IN	COMP2_CH0	The COMP2_CH0 (Channel 0 secondary Compensation) pin is the second compensation input of the channel 0 boost controller.
16	OUT	nRESET	The nRESET (Reset) pin is an active low open drain output. Active when the SMB111 is powered up. Remains low for a user programmable period of 25, 50, 100, or 200 ms after all enabled supplies have exceeded their programmed thresholds. When used, this pin should be pulled high by an external pull up resistor.
17	OUT	LSDRV_CH0	The LSDRV_CH0 (Channel 0 Low-side Driver) pin is the lower switching node of the synchronous boost controller. This pin attaches to an external n-channel MOSFET
18	OUT	LSDRV_CH1	The LSDRV_CH1 (Channel 1 Low-side Driver) pin is the lower switching node of the channel 1 synchronous buck controller. Attaches to the gate of n-channel MOSFET.
19	PWR	HVSUP1	Channel 1 High Voltage Supply for Channel 1 buck driver.
20	OUT	HSDRV_CH1	The HSDRV_CH1 (Channel 1 High-side Driver) pin is the upper switching node of the channel 1 synchronous buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH1 and assertion of LSDRV_CH1 to prevent excessive current flow during switching.
21	IN	COMP2_CH1	The COMP2_CH1 (Channel 1 secondary Compensation) pin is the secondary compensation input of the channel 1 buck controller.
22	IN	COMP1_CH1	The COMP1_CH1 (Channel 1 primary Compensation) pin is the primary compensation input of the channel 1 buck controller. Each pin is internally connected to a programmable resistor divider.
23	IN	VM_CH1	The VM_CH1 (Channel 1 Voltage Monitor) pin connects the channel 6 controller output. Internally the VM_CH1 pin connects to an internal programmable resistor divider.
24	OUT	LSDRV_CH2	The LSDRV_CH2 (Channel 2 Low-side Driver) pin is the lower switching node of the channel 2 synchronous buck controller. Attaches to the gate of n-channel MOSFET.
25	PWR	HVSUP2	Channel 2 High Voltage Supply for Channel 2 buck driver.
26	OUT	HSDRV_CH2	The HSDRV_CH2 (Channel 2 High-side Driver) pin is the upper switching node of the channel 2 synchronous buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH2 and assertion of LSDRV_CH2 to prevent excessive current flow during switching.
27	IN	PWREN0	The PWREN0 (Power Enable 0) pin is a programmable input used to enable (disable) selected supplies. When unused this pin should be tied to a solid logic level.
28	IN	COMP2_CH2	The COMP2_CH2 (Channel 2 secondary Compensation) pin is the secondary compensation input of the channel 2 buck controller.

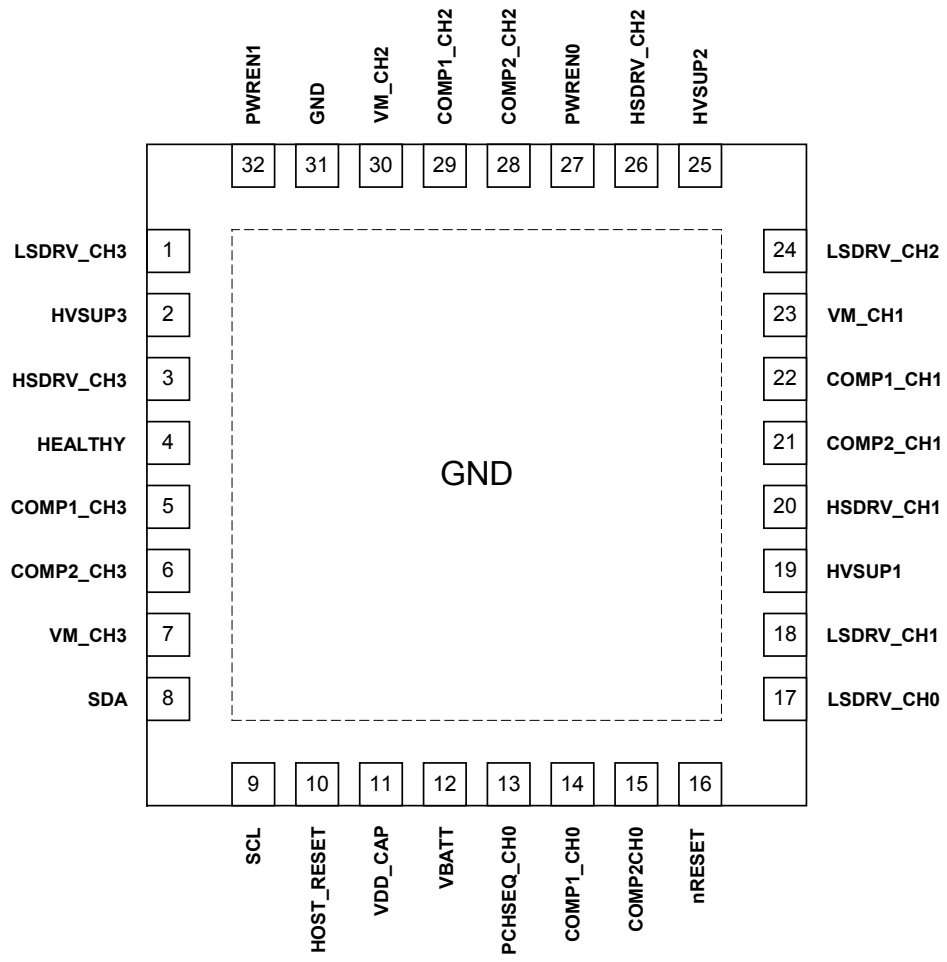
PIN DESCRIPTION

Pin Number	Pin Type	Pin Name	Pin Description
29	IN	COMP1_CH2	The COMP1_CH2 (Channel 2 primary Compensation) pin is the primary compensation input of the channel 2 buck controller. Each pin is internally connected to a programmable resistor divider.
30	IN	VM_CH2	The VM_CH2 (Channel 2 Voltage Monitor) pin connects the channel 2 controller output. Internally the VM_CH2 pin connects to an internal programmable resistor divider.
31	PWR	GND	Ground.
32	IN	PWREN1	The PWREN1 (Power Enable 1) pin is a programmable input used to enable or disable-selected supplies. User programmable settings allow control of the 4 switching regulators to by this pin. This pin may also be programmed as a power on pin used to begin power-on(off) sequencing. When used to enable power-on sequencing, this pin is de-bounced for a programmable period of 0, 25, 50, 100 ms period. When unused this pin should be tied to a solid logic level.
PAD	PWR	GND	The bottom slug (thermal pad) of the SMB111 should be attached to a ground pad.

PACKAGE AND PIN DESCRIPTION

Top view

SMB111
5mm x 5mm QFN-32



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Terminal Voltage with Respect to GND:
VBATT Supply Voltage ..... -0.3V to +6.5V
HVSUP Supply Voltage ..... -0.3V to +6.5V
All Other Pins ..... -0.3V to VBATT
Output Short Circuit Current 100mA
Reflow Solder Temperature (30 sec)..... +260°C
Junction Temperature..... +150°C
ESD Rating per JEDEC ..... +1500V
Latch-Up testing per JEDEC.....±100mA

RECOMMENDED OPERATING CONDITIONS

Commercial Temperature Range..... 0°C to +70°C
Industrial Temperature Range ..... -40°C to +85°C
VBATT Supply Voltage .....2.7V to +6.0V
HVSUP Supply Voltage.....2.7V to +6.0V
All Others.....GND to VBATT
Package Thermal Resistance (θ_{JA}), 32-Pad QFN (thermal pad connected to PCB)..... 37.2°C/W
Moisture Classification Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention ..... 100 Years
Endurance..... 100,000 Cycle

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BATT}	Input supply voltage	Input supply voltage (operational)	2.7		6.0	V
V_{HVSUP}	Buck driver supply voltage		2.7		6.0	V
V_{UVLO}	Undervoltage lockout	VBATT rising		2.2	2.3	V
		VBATT falling	1.9	2.0		
$I_{DD-MONITOR}$	Monitoring current	All voltage inputs monitored. No supplies switching, VBATT at 4.2V.		330	500	µA
I_S	Standby current	Current with 1 output enabled		1.2		mA
$I_{DD-ACTIVE}$	Total current all channels switching.	VBATT at 4.2V. No load.			5	mA
$V_{REF(INT)}$	Internal voltage reference	Commercial temperature range	0.995	1.0	1.005	V
		Industrial temperature range	0.975	1.0	1.025	V
VDD_CAP	Internal supply, present on VDD_CAP pin		2.4	2.5	2.6	V
Oscillator						
f_{OSC}	Oscillator frequency			800		kHz
Δf_{OSC}	Oscillator frequency accuracy	Commercial temperature range	-10		+10	%
		Industrial temperature range	-15		+15	%
O_{PP}	Oscillator peak-to-peak voltage			1.0		V
Δf_{SV}	Frequency stability for voltage			0.1		%/V

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
Δf_{ST}	Frequency stability for temperature	Commercial temperature range		1.0		kHz/°C
		Industrial temperature range		1.3		kHz/°C
Error Amplifier						
A_{VOL}	Open loop voltage Gain	At DC		60		dB
BW	Frequency bandwidth	At AV=0 dB		30		MHz
I_{SOURCE}	Output source current	At 0.5V		20		µA
I_{SINK}	Output sink current	At 0.5V		800		µA
Output Block Channel 0 (Boost)						
V_{OUT}	Programmable voltage set point range	Voltage set point range PWM mode. Pre-diode, VBATT=4.2V, I_{LOAD} required $V_{OUT} = V_{BATT} / (1\text{-duty cycle})$	5.75		32	V
		Voltage set point range, PFM mode. Pre-diode VBATT=4.2V, I_{LOAD}=0, $V_{OUT} = V_{BATT} / (1\text{-duty cycle})$	4.2		17	V
ΔV_{OUT}	Output accuracy	Excluding external resistor divider accuracy. Commercial temperature range.	-0.5		+0.5	%
		Excluding external resistor divider accuracy. Industrial temperature range.	-2.0		+2.0	%
R_{DRVH}	HSDRV ON resistance	Output high		11		Ω
		Output low		3		
D.C.	PWM	High	87	91	95	%
		Low		22	26	
	PFM	High	76	80	84	%
		Low		0		
V_{COMP1}	Feedback voltage reference	COMP1 pin Programmable in 4mV steps		1.0		V
ΔV_{COMP1}	Feedback voltage reference accuracy	COMP1 pin	-0.5		+0.5	%
ML	Minimum load[2]	PFM, L=33uF, V_O=12V, V_{IN}=4.2V, V_D=0.3V		29		kΩ
I_{PCHSEQ}	PCHSEQ sink current		50			µA
EN_{TH}	Enable threshold	Voltage on PCHSEQ pin when LSDRV output is enabled		200		mV

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output Block Channel 1 to Channel 3 (Buck)						
V_{OUT}	Voltage nominal set point range	VBATT= 4.2V, I_{LOAD}=0, V_{OUT} = V_{BATT} x (duty cycle)	1.0		4.2	V
ΔV_{OUT}	Output accuracy (including internal resistor divider)	Commercial temperature range	-0.5		+0.5	%
		Industrial temperature range	-2.0		+2.0	%
R_{DRVH}	HSDRV ON resistance	Output high		8		Ω
		Output low		8		Ω
R_{DRVL}	LSDRV ON resistance	Output high		17		Ω
		Output low		3		Ω
V_{COMP1}	Feedback voltage reference	COMP1 pin, programmable in 4mV steps		1.0		V
ΔV_{COMP1}	Feedback voltage reference accuracy	COMP1 pin	-0.5		+0.5	%
D.C.	100% Max Duty Cycle	High Duty Cycle		100		%
		Low Duty Cycle	15	20	24	
Logic levels						
V_{IH}	Input high voltage		0.7x VDD_CAP		6.0	V
V_{IL}	Input low voltage		0		0.3x VDD_CAP	V
V_{OL}	Open drain outputs	I_{SINK} = 1mA	0		0.4	V
I_{OL}	Output low current		0		1.0	mA

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Programmable Monitoring Thresholds						
V_{PUV1}	nBATT_FAULT threshold	Programmable in 150 mV increments	2.55		3.60	V
ΔV_{PUV1}	nBATT_FAULT accuracy		-20		+20	mV
V_{PUV2}	POWER_FAIL threshold	Programmable in 150 mV increments	2.55		3.60	V
ΔV_{PUV2}	POWER_FAIL accuracy		-20		+20	mV
P_{UVTH}	Programmable under voltage threshold	For channels 0-3. Relative to nominal set point voltage		-5		**%**
				-10		
				-15		
				-20		
P_{OVTH}	Programmable over voltage threshold	For channels 0-3. Relative to nominal set point voltage		5		**%**
				10		
				15		
				20		
t_{PPTO}	Programmable power-On sequence timeout period.	Programmable power-On sequence position to sequence position delay.	1.3	1.5	1.7	ms
			10.6	12.5	14.4	
			21	25	29	
			42	50	58	
t_{DPOFF}	Programmable power-off sequence timeout period.	Programmable power-off sequence position to sequence position delay.	1.3	1.5	1.7	ms
			10.6	12.5	14.4	
			21	25	29	
			42	50	58	
t_{PDB}	PWREN1 de-bounce period	When PWREN1 is programmed as power on pin.		0		ms
			21	25	29	
			42	50	58	
			85	100	115	
t_{PRTO}	Programmable reset time-out delay	Programmable time following assertion of last supply before nRESET pin is released high.	21	25	29	ms
			42	50	58	
			85	100	115	
			170	200	230	
			42	50	58	

AC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{PST}	Programmable sequence termination period	Time between active enable in which corresponding outputs must exceed there programmed under voltage threshold. If exceeded, a force shutdown will be initiated.		OFF		ms
			42	50	58	
			85	100	115	
			170	200	230	
t_{PFTO}	POWER_FAIL timeout period	Timeout begins after latch is cleared.	3.2	3.75	4.3	ms
t_{BFTO}	nBATT_FAULT timeout period	Timeout begins after fault conditions cleared.	3.2	3.75	4.3	ms
t_{PGF}	Programmable glitch filter	Period for which fault must persist before fault triggered actions are taken. Present on all outputs		0		µs
			6.8	8	9.2	
SR_{REF}	Programmable slew rate reference	Adjustable slew rate factor proportional to output slew rate.	340	400	460	V/s
			170	200	230	
			85	100	115	
			57	67	77	
			42	50	58	
			28	33	38	
			21	25	29	
			17	20	23	
Output Block - Channel 0						
t_{RL}	LS Driver output rise time	C_G=100pF, VBATT=4.2V		10		ns
t_{FL}	LS Driver output fall time	C_G=100pF, VBATT=4.2V		10		ns
Output Block - Channel 1 to Channel 3						
t_{RL}	LS Driver output rise time	C_G=100pF, VBATT=4.2V		10		ns
t_{FL}	LS Driver output fall time	C_G=100pF, VBATT=4.2V		10		ns
t_{RH}	HS Driver output rise time	C_G=100pF, VBATT=4.2V		15		ns
t_{FH}	HS Driver output fall time	C_G=100pF, VBATT=4.2V		5		ns
t_{DT}	Driver non-overlap delay	High to low transition on HSDRV		20		ns
		Low to high transition on buck HSDRV		10		

1. Guaranteed by design
2. The minimum load for Boost channels is defined by the following equation: where VO = Programmed output voltage, VIN =P-Channel MOSFET source voltage, L = inductance, Vd = forward diode drop (0.6V silicon, 0.3V Schottky)

$$Rmax = \frac{2*L*Vout*(Vout - VIN + Vd)}{VIN^{2}*1.25E-8}$$

3. Voltage accuracies are only guaranteed for factory-programmed settings. Changing the output voltage from that reflected in the customer specific CSIR code will result in inaccuracies exceeding those specified above by 1%.

I²C-2 WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS –100 kHz

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	100kHz			
			Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		0		100	kHz
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period		4.0			µs
t_{BUF}	Bus free time	Before new transmission – Note 4	4.7			µs
$t_{SU:STA}$	Start condition setup time		4.7			µs
$t_{HD:STA}$	Start condition hold time		4.0			µs
$t_{SU:STO}$	Stop condition setup time		4.7			µs
t_{AA}	Clock edge to data valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data output hold time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA rise time	Note 4			1000	ns
t_F	SCL and SDA fall time	Note 4			300	ns
$t_{SU:DAT}$	Data in setup time		250			ns
$t_{HD:DAT}$	Data in hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t_{WR_CONFIG}	Write cycle time config	Configuration registers			10	ms
t_{WR_EE}	Write cycle time EE	Memory array			5	ms

Note 4 - Guaranteed by Design.

TIMING DIAGRAMS

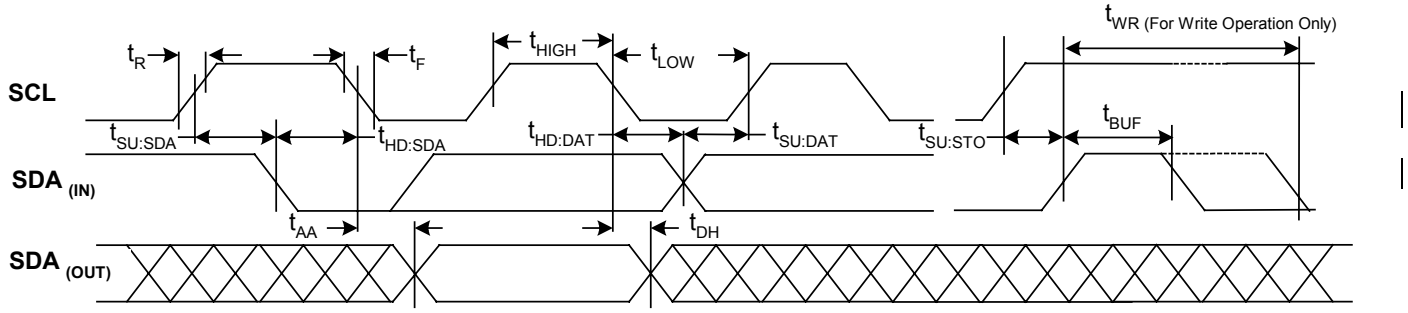
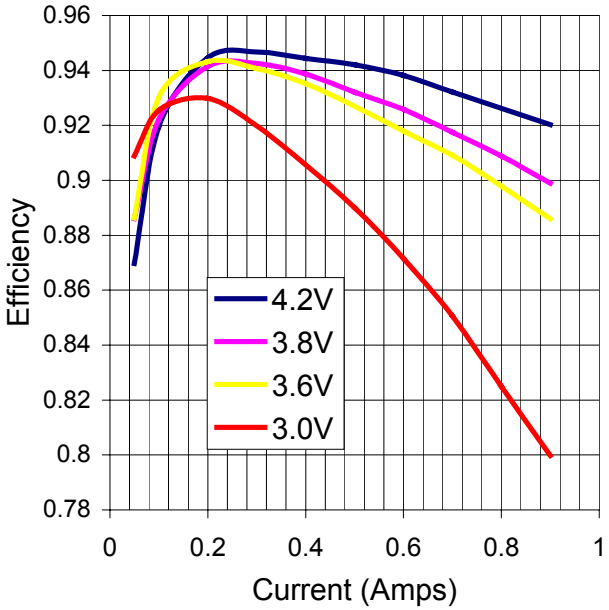


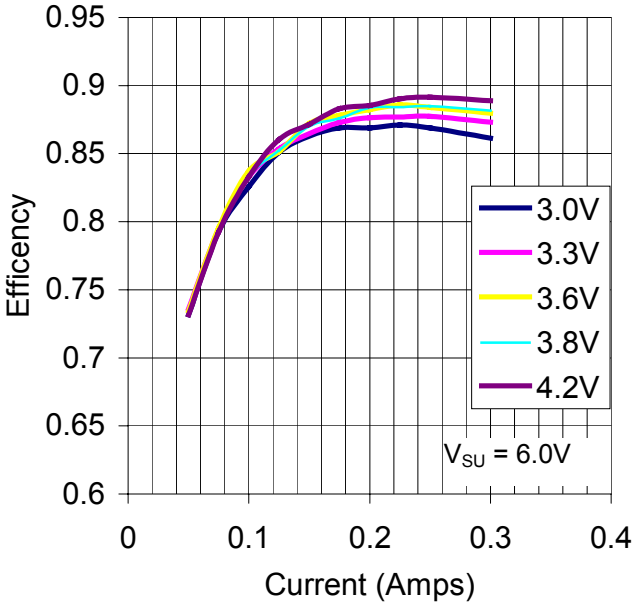
Figure 4 – I²C timing diagram

EFFICIENCY GRAPHS

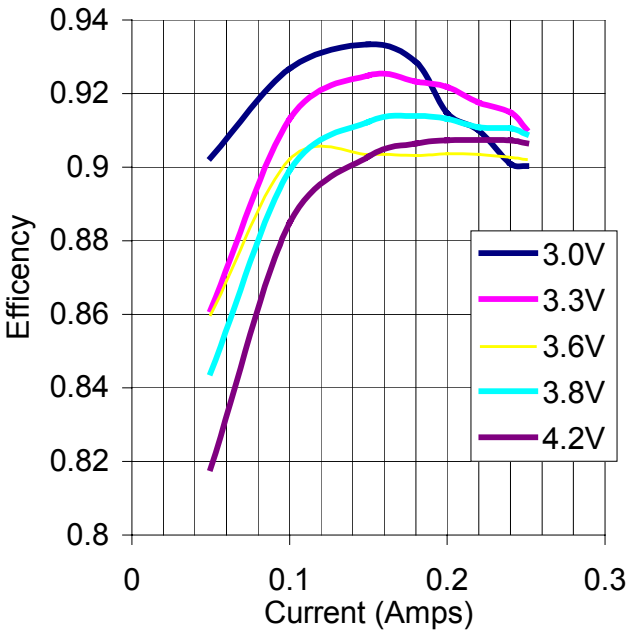
Boost 6.0 Volts



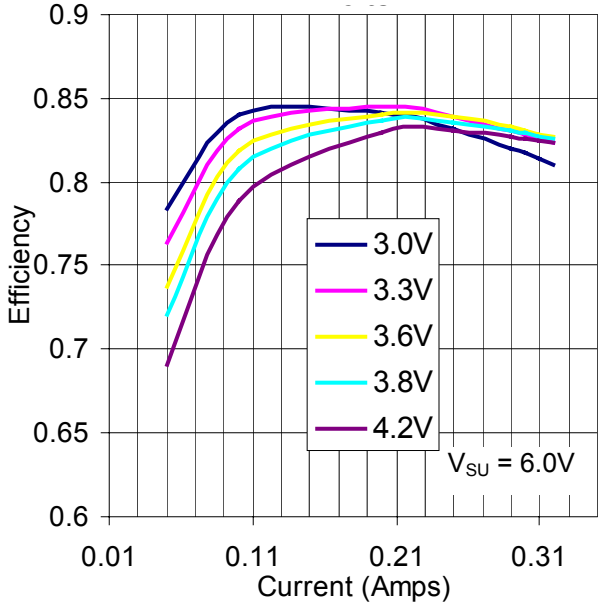
Buck (SU + SD) 5.0 Volts



Buck 2.5 Volts



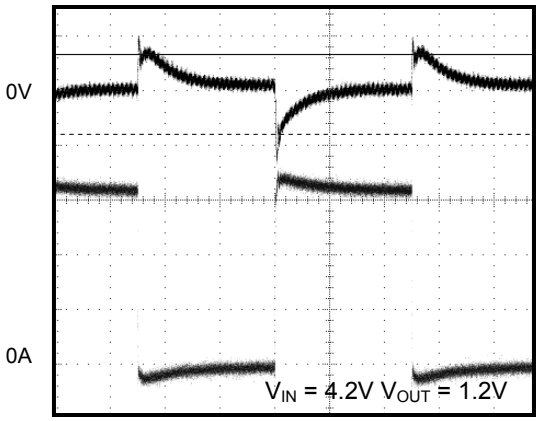
Buck (SU + SD) 3.0 Volts



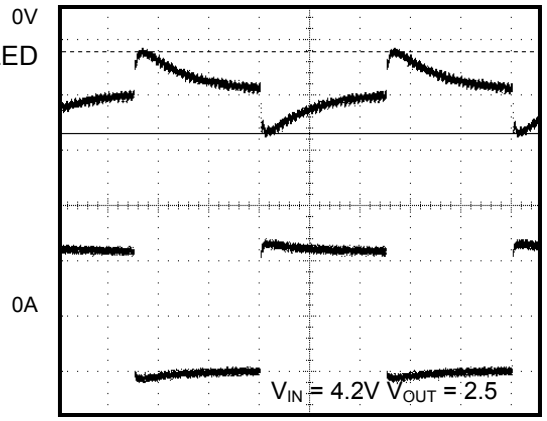
(All measurements are taken at 25°C, and are based on the Applications Schematic.)

TRANSIENT RESPONSE

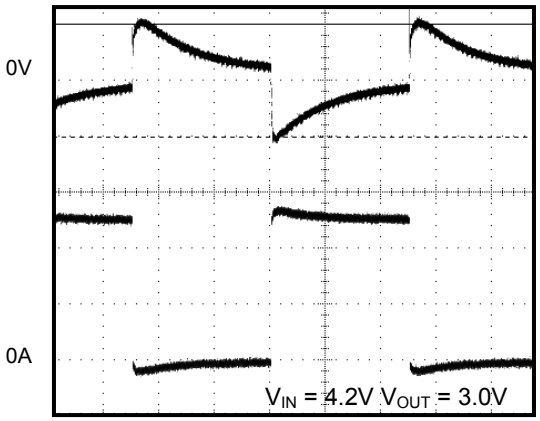
CHANNEL 1 BUCK TRANSIENT RESPONSE



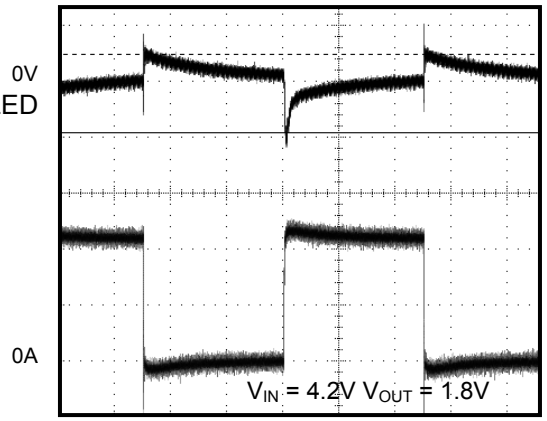
CHANNEL 1 BUCK TRANSIENT RESPONSE



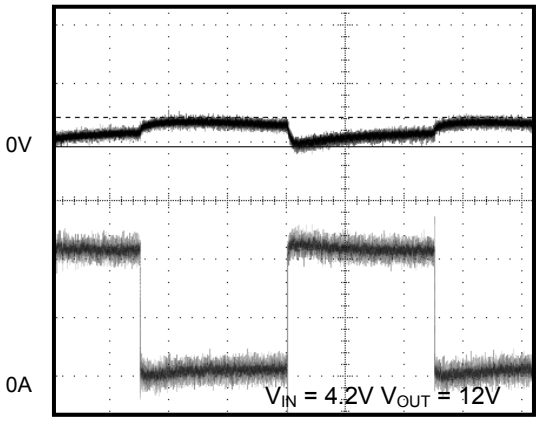
CHANNEL 2 BUCK TRANSIENT RESPONSE



CHANNEL 3 BUCK TRANSIENT RESPONSE



CHANNEL 0 BOOST TRANSIENT RESPONSE



(All measurements are taken at 25°C, and are based on the Applications Schematic.)

TIMING DIAGRAMS: POWER-ON SEQUENCE

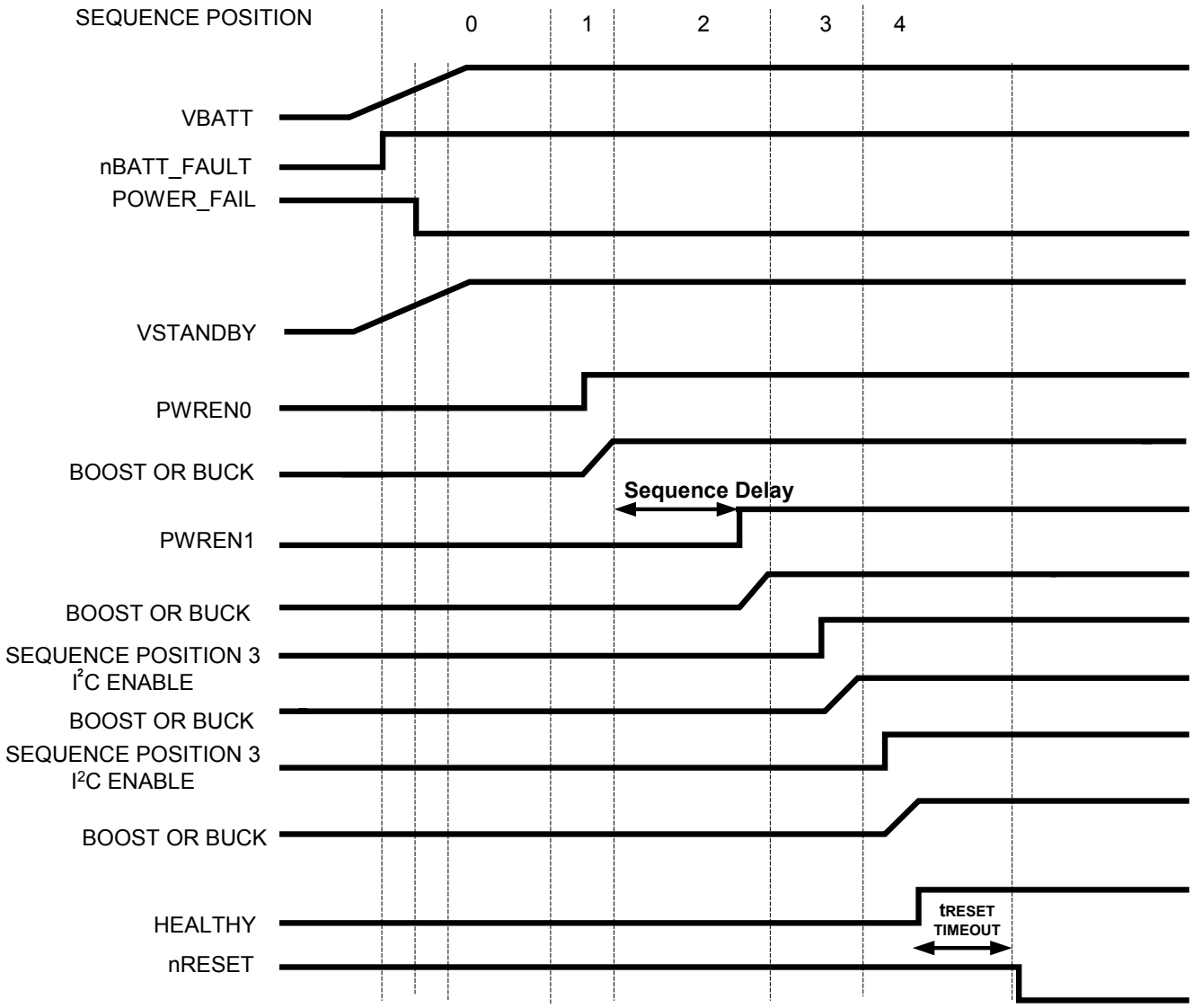


Figure 5 – SMB111 power-On sequence. Any combination of outputs may be enabled in any sequence position by asserting the PWREN[0,1] enable pin. The PWREN1 pin can also be used as a power-on pin sequencing all channels on without an I^2C command. Any PWM channel may be enabled or disabled through an I^2C command or by the PWREN[0,1].

APPLICATIONS INFORMATION

POWER SUPPLY

The SMB111 can be powered from an input voltage between 2.7-6.0 volts applied between the VBATT pin and ground. The SMB111 is optimized for use with a rechargeable single cell Lithium ion battery. The input voltage applied to the VBATT pin is internally regulated and used as an internal VBATT supply. The VBATT pin is monitored by an UnderVoltage Lockout (UVLO) circuit, which prevents the device from turning on when the voltage at this node is less than the UVLO threshold.

POWER-ON/OFF CONTROL

The outputs on the SMB111 can be turned on in one of three ways: first a general purpose enable input pin, PWREN1, can be configured as a power on pin, an I^2C **Power on** command can be issued, and a programmable bit is set to initiate the power on process when the UVLO threshold is exceeded. If a power-off or force-shutdown occurs due to a UV or OV fault on any PWM channel, a sequence termination, or due to an I^2C command, a restart will only occur if the power-on pin is toggled or an I^2C **Power on** command is issued.

ENABLE

Once a power on command has been issued, the power on process can be controlled by means of an enable signal. Each channel can be controlled by one of four enable signals and the assignment type can be mixed and matched for each of the four channels. The enable signal can stall the power-on process until the enable is valid, or disable a controller once all supplies have been enabled. There are two ways to generate the enable signal; the first approach allows the enable signal to be assigned to either the PWREN0 or the PWREN1 pin, and the second approach allows the enable to be controlled by the contents of a volatile register that can be written to at any time. This volatile register will be automatically initialized once the UVLO threshold has been exceeded to a known programmed state.

POWER-ON SEQUENCING

Each channel on the SMB111 may be placed in any one of four unique sequence positions. To provide a programmable sequence order, the SMB111 navigates between each sequence positions using a feedback-based cascade-sequencing circuit. Cascade sequencing is the process in which each channel is continually compared against a programmable reference voltage until the voltage on the monitored channel exceeds the reference voltage, at which point an internal sequence position counter is incremented and the next sequence position is entered.

Once power-on sequencing has been initiated, automated sequencing may commence in one of three ways: normal sequencing, sequencing with enable, and sequencing with channel bypass. In addition, each channel may be powered on in a manual mode, independent of the sequence position. The power-on sequencing mode selection is programmable over the I^2C bus and stored in the non-volatile memory.

NORMAL CASCADE SEQUENCING

During *Normal Sequencing*, the sequence position counter is initialized to the first sequence position (position 1), each channel occupying this position then waits an individual programmable timeout period (t_{PPTO}) of 1.5, 12.5, 25, or 50 ms. Once enabled, all channels occupying the first sequence position will begin a soft-start. As the output voltage of the channel is ramped up, it is monitored by a comparator based, user programmable, under-voltage threshold sensor. After this threshold is exceeded, indicating that the selected channel(s) have reached their nominal operating range the sequence position counter is incremented, and fault monitoring begins for that channel. Once all channels occupying the first sequence position have surpassed their under-voltage thresholds, the power-on delay for the next sequence position will begin. This process continues until all channels have been sequenced on and are above their under-voltage threshold.

SEQUENCING WITH ENABLE

During the *Sequencing With Enable* mode, sequencing commences as with the *Normal Sequencing*, except that prior to a channel beginning to soft-start, the enable corresponding to that channel must be asserted. In the event that the enable is not asserted, sequencing will halt indefinitely until a valid enable is provided. Once a valid enable is provided, a soft-start function will begin for that channel. This process will continue until all channels occupying the first sequence position are above their under-voltage settings, at which point the sequence position counter will be incremented.

SEQUENCING WITH CHANNEL BYPASS

When the *Sequencing With Channel Bypass* mode is selected, sequencing will commence as with the *Sequencing With Enable*, except that if the enable signal is not asserted by the end of the power-on delay period, that channel will be bypassed. If no other channels occupy the current sequence position, the sequence position counter will be incremented beginning the power-on delay for all channels in the next sequence position. Once a channel has been bypassed, it may still be enabled any time prior to a power off operation.

APPLICATIONS INFORMATION (CONTINUED)

MANUAL MODE

The SMB111 also provides a manual power-on mode in which each channel may be enabled individually irrespective of the state of other channels. In this mode, the enable has complete control over the channel, and all sequencing is ignored. In Manual mode channels will not be disabled in the event of a fault, and will not be disabled when the battery voltage falls below the UVLO threshold.

FORCE-SHUTDOWN

When a battery fault occurs, a UV/OV is detected on any output, or an I^2C force-shutdown command is issued, all channels will be immediately disabled, without regard to sequence positions of power off delay times.

SEQUENCE TERMINATION TIMER

At the beginning of each sequence position, an optional internal programmable timer will begin to time out. When the sequence termination timer has expired, the SMB111 will automatically perform a force-shutdown operation. This timer is user programmable with a programmable sequence termination period (t_{PST}) of 50, 100, and 200 ms.

POWER OFF SEQUENCING

The SMB111 has a power-off sequencing operation. During a power off operation the supplies will be powered off in the reverse order they where powered on in. During the power off sequencing, all enables are ignored.

A power-off sequence command can be issued in one of two ways, either by an I^2C command or by the assertion of the PWREN1 pin. Once initiated, the sequence position counter will be set to the last sequence position and disable that channel without soft-start control; once off, the power off delay for the channel(s) in the next to last sequence position will begin to timeout, after which that channel(s) will be disabled. This process will continue until all channels have been disabled and are off. The programmable power-off sequence timeout period (t_{DPOFF}) can be set to 1.5, 12.5, 25, or 50 ms.

MONITORING

The SMB111 monitors all 4 PWM outputs for under-voltage (UV) and over-voltage (OV) faults. The monitored levels are user programmable, and may be set at 5, 10, 15, and 20 percent of the nominal output voltage.

Each output possesses a glitch filter to ensure that short violations in the UV or OV settings will not result in a fault-triggered action. All glitch filters on the SMB111 are user programmable and may be set to either 0 or 8 µs.

In the event that one or more channels violate their respective UV/OV setting for a period exceeding that specified by the glitch filter, all channels (not set to Manual mode) can optionally be powered off and-or, the healthy pin can be triggered. The programmable power off conditions that may result from a threshold violation include the immediate power off all supplies (force-shutdown) or the sequence of all supplies off.

Monitoring is accomplished by a comparator-based approach, in which a programmable voltage reference is compared against the monitored signal. Each channel possesses a dedicated reference voltage generated by a programmable level shifting digital to analog controller. Each of which can be set from 0-1.0 volts in 4mV increments.

BATTERY MONITORING

The battery voltage is monitored for two user programmable UV settings via the VBATT pin

The SMB111 contains two user programmable voltage-monitoring levels, UV1 (nBATT_FAULT) and UV2 (POWER_FAIL). Battery voltage, like all monitored voltages, is compared against a user programmable voltage set internally by a digital to analog controller.

Once the voltage on the VBATT pin has fallen below either of the programmable under voltage set points the SMB111 can be programmed to respond in one of three ways, it can perform: a power-off operation, a force-shutdown operation, or take no action. When programmed to perform a power-off or force-shutdown operation the SMB111 can optionally be programmed to latch the outputs off until an I^2C power-on command is issued or immediately restart once the UV condition has been removed.

SOFT START

The SMB111 provides a programmable soft-start function for all outputs. The soft-start control limits the slew rate that each output is allowed to ramp up without the need for an external capacitor. The soft start slew rate is proportional to the product of the output voltage and a slew rate reference; see Figure 5. This global reference is programmable and may be set to 400, 200, 100, 67, 50, 33, 25, and 20 volts per second. The slew rate control can also be disabled on any channel not requiring the feature.

POWER-ON SEQUENCING FLOW CHART

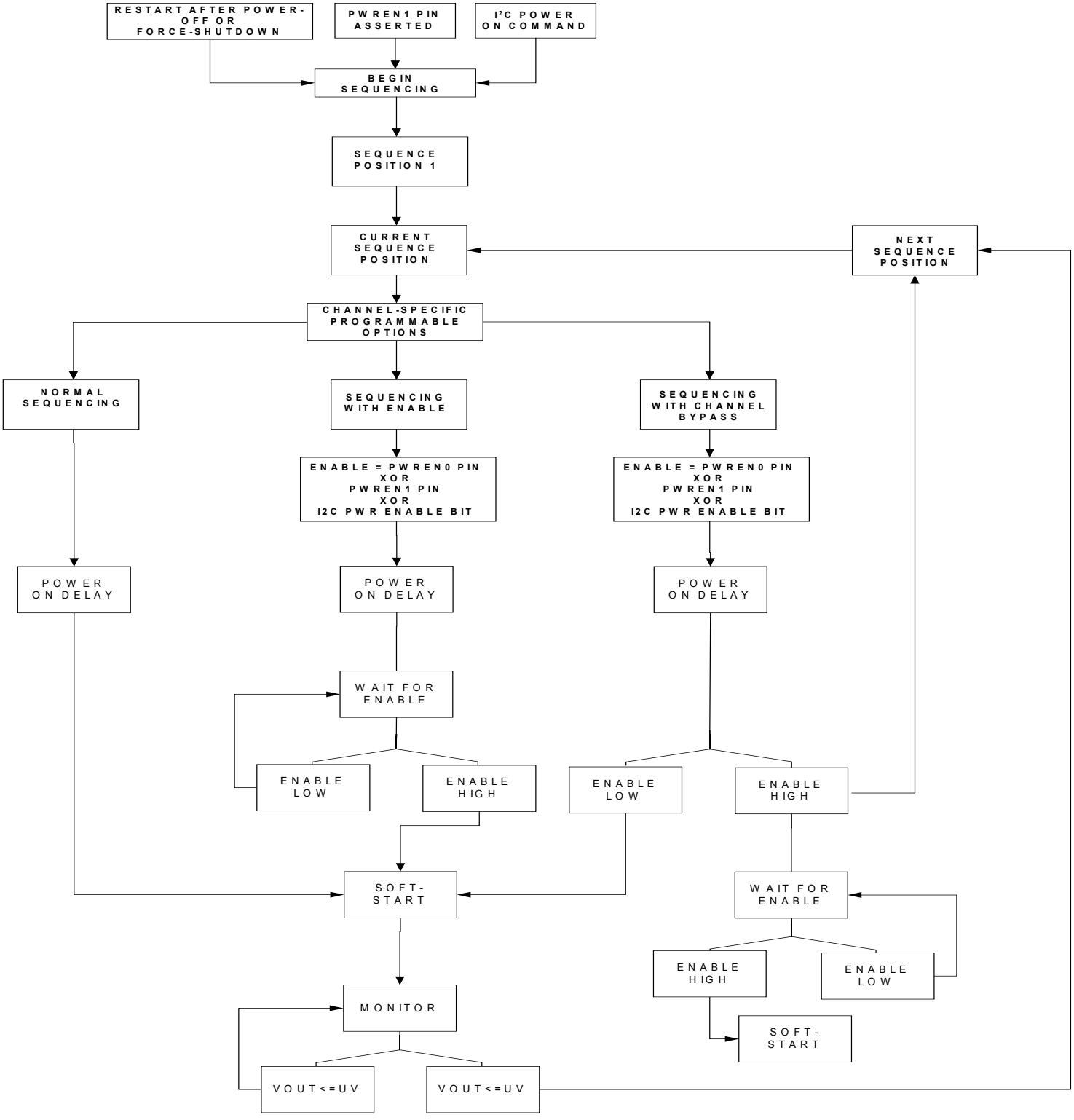


Figure 6 – Power-on sequencing flow chart: There are three automated power-on sequencing modes, and a manual mode.

APPLICATIONS INFORMATION (CONTINUED)

MINIMUM LOAD

The duty cycle is limited to a 10-90% range. Consequently, the boost channels require a minimum load to prevent over voltage conditions from occurring.

This may be overcome by attaching a resistor preload to the output that matches the minimum load requirements. This approach will result in a constant current consumption while the outputs are enabled. Alternatively, a zener diode (with a higher breakdown voltage than the output) can be connected across the output clamping the output voltage. This approach will not draw current when the minimum load is enabled on the output.

MARGINING

The SMB111 has two additional voltage settings for channels 0-3, margin high and margin low. The margin high and margin low voltage settings have the same voltage range as the controllers' nominal output voltage. These settings are stored in the configuration registers and are loaded into the voltage setting by margin commands issued via the I^2C bus.

The margin command registers contain two bits for each channel that decode the commands to margin high, margin low, or control to the nominal setting. Therefore, any combination of margin high, margin low, and nominal control is allowed in the margining mode.

Once the SMB111 receives the command to margin the supply voltages, it begins adjusting the supply voltages to move toward the desired setting. When all channels are at their voltage setting, a bit is set in the margin status registers.

A seven level margining option is available for channel 2. When enabled, seven level margining allows channel 2 to be dynamically modified to one of seven pre-determined voltage levels. This transition is made by means of a volatile I^2C write command.

Channel 1 looses the margin high and margin low settings when channel 2 is configured for seven level margining.

Note: Configuration writes or reads of registers should not be performed while dynamic voltage management.

A typical application utilizing the margining functionality is depicted in Figure 7. When used with a boost controller setup as a constant current white LED driver, margining can be used to adjust the current through the LED chain as an adjustable brightness control.

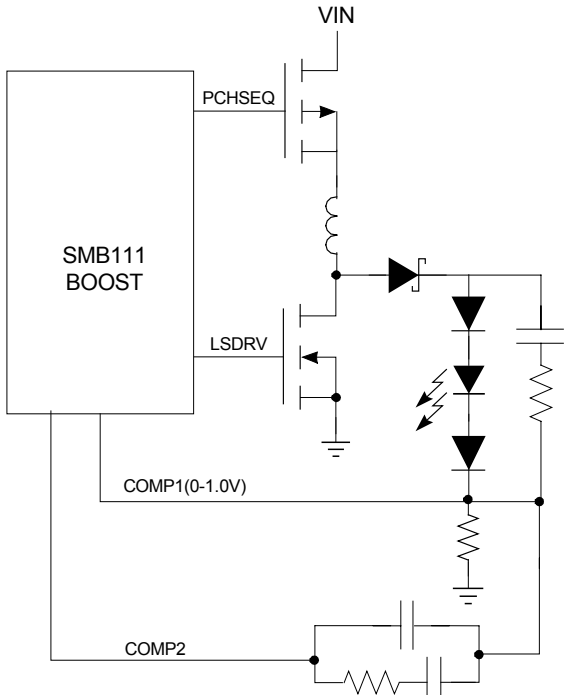


Figure 7 – Boost configured as a constant current LED driver with adjustable current capabilities.

APPLICATIONS INFORMATION (CONTINUED)

MULTIPLE PHASE OPERATION

The SMB111 can be programmed for channel interleaving, where each channel is phase delayed from the next by a programmable phase delay. The phase delay also has an associated.

There are three available phase options: single phase where all channels switch simultaneously, dual phase where channels are separated into two groups, and each group switches 180° out of phase, and a four phase mode where all channels switch at least 45° out of phase.

The PLL option is limited to the dual-phase and four-phase mode, and can be optionally disabled for the dual phase mode.

By default, all channels operate in the four-phase mode. The phase interleaving option cannot be changed with the GUI; however, the current phase option can be read. For ordering purposes, the GUI can be used to select the required phase option.

APPLICATIONS INFORMATION (CONTINUED)

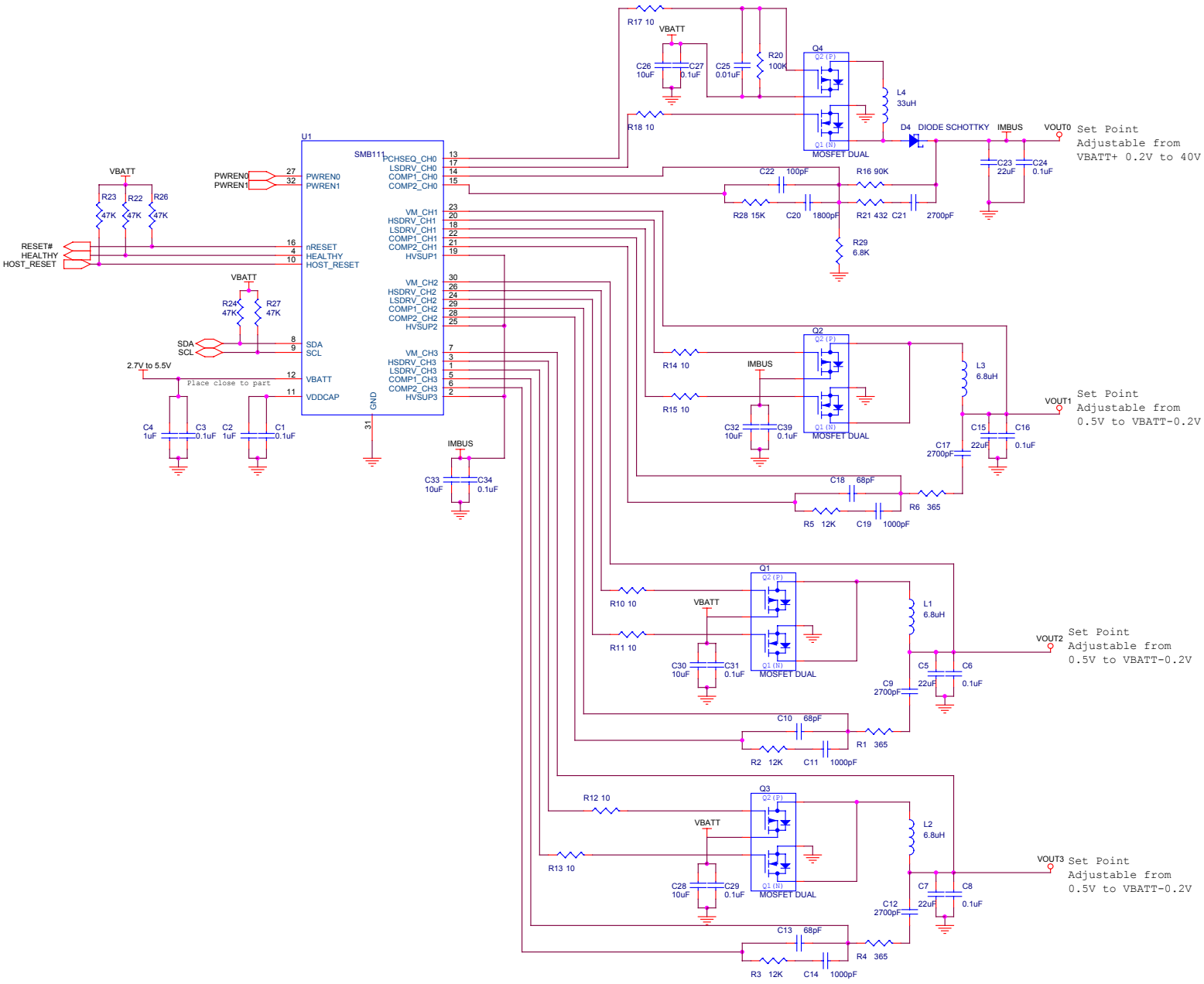


Figure 8 – Applications schematic.

APPLICATIONS INFORMATION (CONTINUED)

Item	Description-	Vendor / Part Number	Qty	Ref. Des.
Resistors				
1	365Ω, 1/16W, 1%, 0402, SMD	Any	3	R1, R4, R6
2	12kΩ 1/16W, 1%, 0402, SMD	Any	3	R2, R3, R5
3	10Ω, 1/16W, 1%, 0402, SMD	Any	8	R10, R11, R12, R13, R14, R15, R17, R18
4	90KΩ, 1/16W, 5%, 0402, SMD	Any	1	R16
5	100KΩ, 1/16W, 5%, 0402, SMD	Any	1	R20
6	432Ω, 1/16W, 5%, 0402, SMD	Any	1	R21
7	47KΩ, 1/16W, 5%, 0402, SMD	Any	5	R22, R23, R24, R26, R27
8	15KΩ, 1/16W, 5%, 0402, SMD	Any	1	R28
9	6.8KΩ, 1/16W, 5%, 0402, SMD	Any	1	R29
Capacitors				
10	0.1uF, 16V, ceramic, X7R, 0402, SMD	Any	11	C1, C3, C6, C8, C16, C24, C27, C29, C31, C34, C39
11	1uF, 6.3V, ceramic, Y5V, 0805, SMD	Any	2	C2, C4
12	22uF, 6.3V, ceramic, Y5V, 1210, SMD	Any	4	C5, C7, C15, C23
13	2700pF, 50V, ceramic, X7R, 0402, SMD	Any	4	C9, C12, C17, C21
14	68pF , 50V, ceramic, X7R, 0402, SMD	Any	3	C10, C13, C18
15	1000pF, 50V, ceramic, X7R, 0402, SMD	Any	3	C11, C14, C19
16	1800pF, 50V ceramic, X7R, 0402, SMD	Any	1	C20
17	100pF, 50V, ceramic, C0G, 0402, SMD	Any	1	C22
18	0.01uF, 50V, ceramic, X7R, 0402, SMD	Any	1	C25
19	10uF, 6.3V, ceramic, X5R, 0805, SMD	Any	5	C26, C28, C30, C32, C33
Semiconductors				
20	MOSFET, Complementary	Fairchild, FDC6420C or Fairchild, FDC6020C	3	Q1, Q2, Q3, Q4
21	Diode, Schottky, 20V, 200mA SS-MI	Panasonic, MA2SD24	1	D4
22	SMB111N	Summit Microelectronics	1	U1
Magnetics				
23	Inductor, 33uH, SMD	Coilcraft DO1608C-333 or Asatech 33uH	1	L4
24	Inductor, 6.8uH, SMD	Sumida Corp CR436R8 or Coilcraft DO1608C-682 or Asatech 6.8uH	3	L1, L2, L3

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 parallel port programming system or the I²C2USB (SMX3201) USB programming system for device prototype development. The SMX3200(1) systems consist of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 and SMX3201 are available from the website (**http://www.summitmicro.com**).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application; while the SMX3201 interfaces directly to the PC's USB port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMB111 via the programming Dongle and cable. An example of the connection interface is shown in Figure 9.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

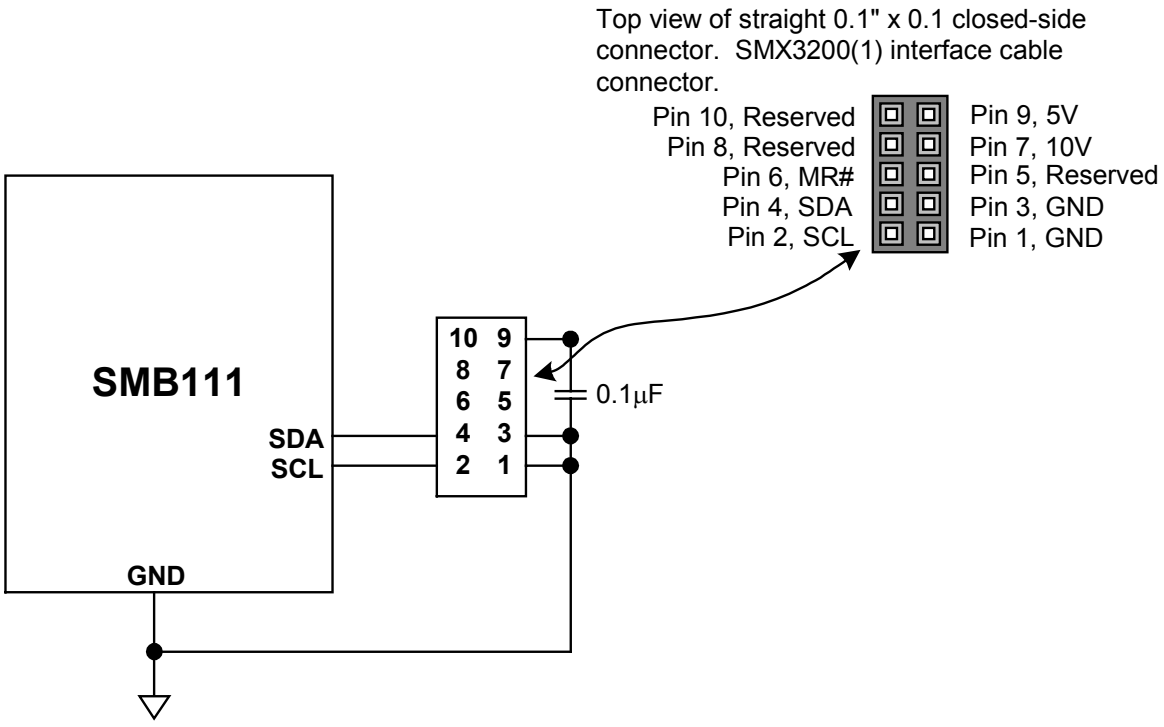


Figure 9 – SMX3200(1) Programmer I²C serial bus connections to program the SMB111.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMB111.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. The slave address can be can be programmed to any seven bit number 0000000_{BIN} through 1111111_{BIN}.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 10 and 11. A Start condition followed by the slave address byte is provided by the host; the SMB111 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB111 responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page.

After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the non-volatile configuration registers and memory registers as well as the volatile command and status registers must be set before data can be read from the SMB111. This is accomplished by issuing a dummy write command, which is a write command that is not followed by a Stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figure 12 for an illustration of the read sequence.

CONFIGURATION REGISTERS

The configuration registers are grouped with the general-purpose memory.

GENERAL-PURPOSE MEMORY

The 96-byte general-purpose memory block is segmented into two continuous independently lockable blocks. The first 48-byte memory block begins at register address pointer $A0_{HEX}$ and the second memory block begins at the register address pointer $C0_{HEX}$; see Table 1. Each memory block can be locked individually by writing to a dedicated register in the configuration memory space.

I²C PROGRAMMING INFORMATION (CONTINUED)

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMB111 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (http://www.summitmicro.com). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMB111. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol. See figure 7 and the SMX3200 Data Sheet.

Slave Address	Register Type
0000000_{BIN} to 1111111_{BIN}	Configuration Registers are located in 00_{HEX} thru $9F_{HEX}$
	General-Purpose Memory Block 0 is located in $A0_{HEX}$ thru BF_{HEX}
	General-Purpose Memory Block 1 is located in $C0_{HEX}$ thru FF_{HEX}

Table 1 - Address bytes used by the SMB111.

I²C PROGRAMMING INFORMATION (CONTINUED)

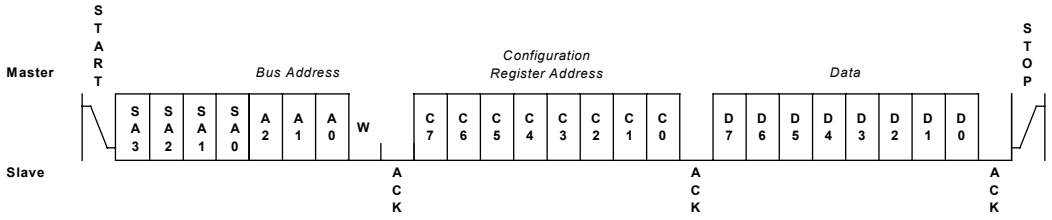


Figure 10 – Register Byte Write

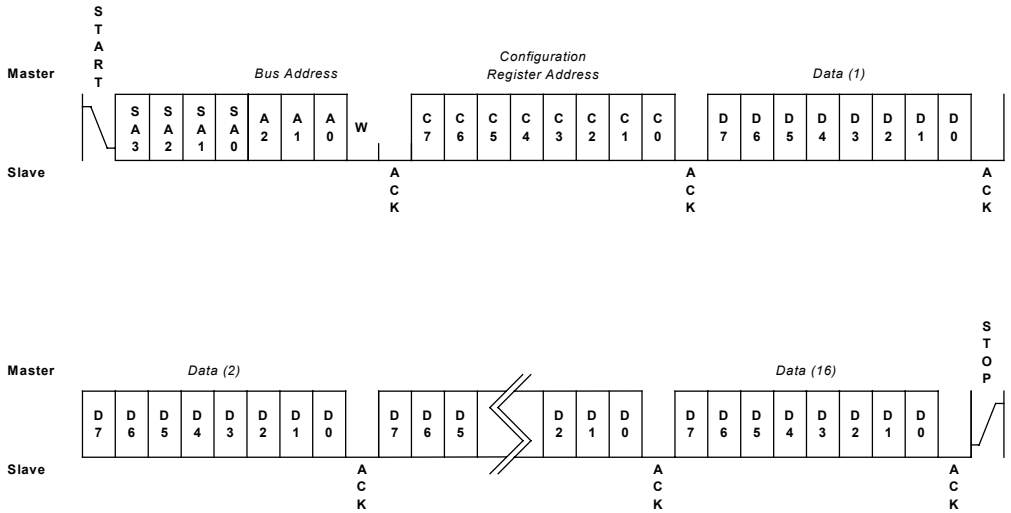


Figure 11 –Register Page Write

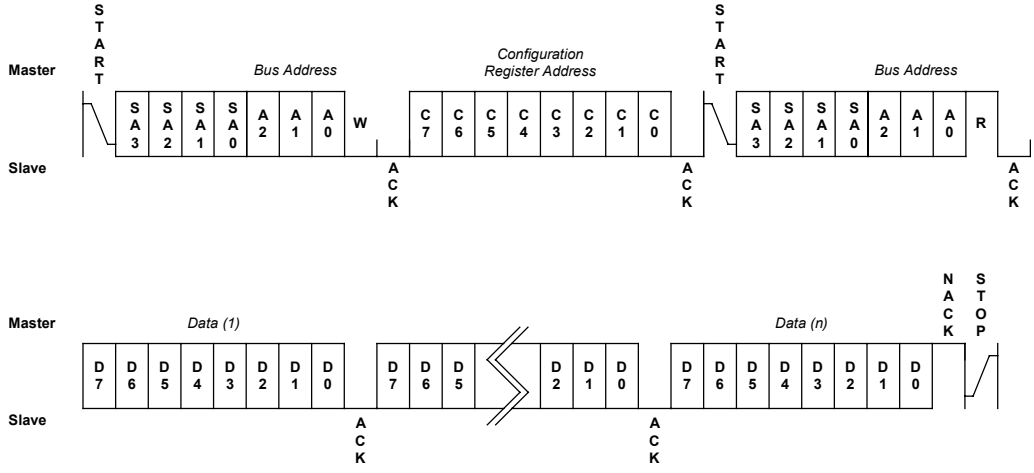


Figure 12 -Register Read

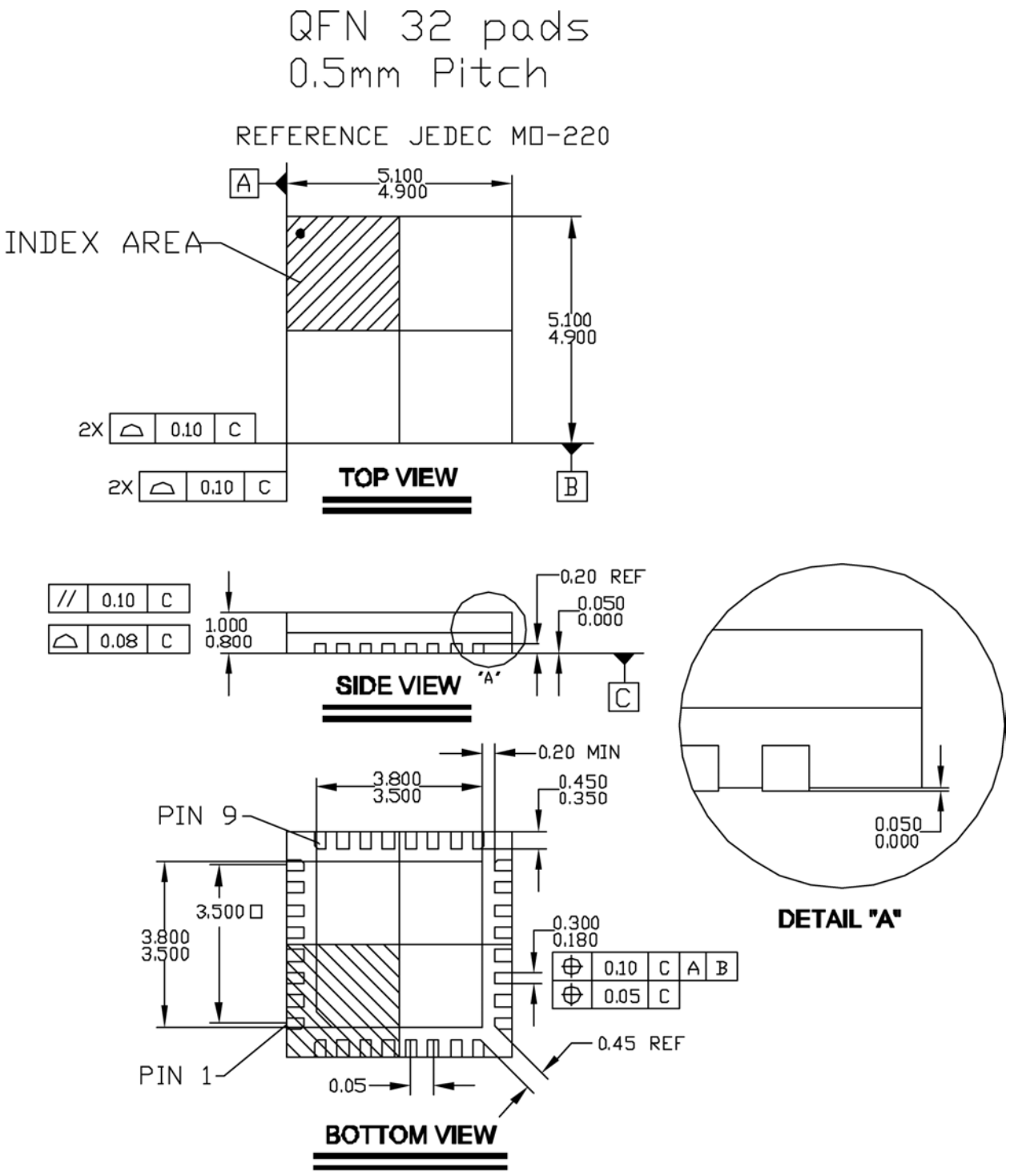
DEFAULT CONFIGURATION REGISTER SETTINGS – SMB111NC-324L

Register	Contents	Register	Contents	Register	Contents
R3	60	R15	00	R2B	00
R4	7D	R16	20	R2C	02
R5	A5	R17	00	R2D	04
R7	B4	R1B	02	R2E	32
RB	60	R1C	02	R2F	06
RC	40	R1D	02	R53	5B
RD	50	R1F	02	R54	77
RF	30	R20	3E	R55	9D
R10	95	R22	30	R57	AB
R11	9A	R23	3E	R5B	65
R12	15	R24	30	R5C	83
R13	10	R28	03	R5D	AD
R14	A0	R2A	00	R5F	BD

Register	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
R30	1	X	X	X	X	X	X	X
R35	1	X	X	X	X	X	X	X
R40	1	1	X	X	X	X	X	X

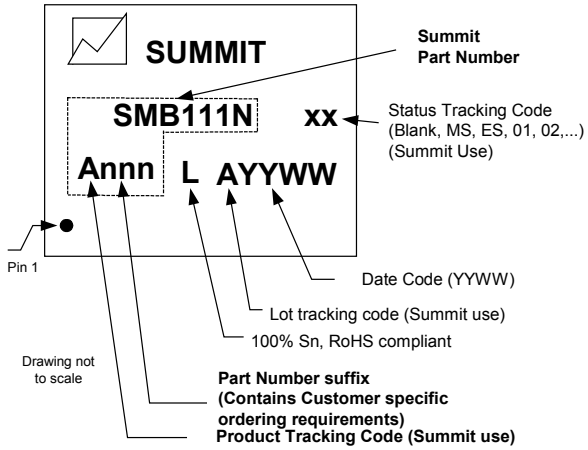
The default device ordering number is SMB111NC-324L. It is programmed with the register contents as shown above and tested over the commercial temperature range. The ordering number is derived from the customer supplied hex file. New device suffix numbers are assigned to non-default requirements.

PACKAGE



1. NOTES: ALL DIMENSIONS ARE mm [MAX] [MIN]

PACKAGE



ORDERING INFORMATION

Summit Part Number SMB111 N C nnn L

Solder Composition
L = 100% Sn, RoHS compliant,

Package
N = 32 Pad QFN

Part Number Suffix
Specific requirements are contained in the suffix

Temperature Range
C = Commercial

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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