Preliminary Information

Five-Channel Digitally Programmable White-LED and TFT/LCD Power Manager

FEATURES & APPLICATIONS

- **Digital programming of all major parameters via I²C interface and non-volatile memory**
  - **Output voltage set-point**
  - **Individual dimming**
  - **Output power-up/down sequencing**
  - **Digital soft-start and output slew rate**
  - **Input/Battery voltage monitoring**
  - **UV/OV monitoring of all outputs**
  - **Enable/Disable outputs independently**
- **Five output channels**
  - **One synchronous step-down (buck) channel**
  - **Two step-up (boost) channels**
  - **One inverting (buck-boost) channel**
  - **One fixed output +3.3V LDO**
- **+2.7V to +6.0V Input Range**
- **Highly accurate reference and output voltage (<0.5%) with Active DC Output Control (ADOC™) technology**
- **Supports multiple strings of up to 12 white LEDs in series**
- **Undervoltage Lockout (UVLO) with hysteresis**
- **800 kHz operating frequency**
- **96 bytes of user configurable nonvolatile memory**

Applications

- **White LED backlighting**
- **High-power LED driving**
- **TFT/LCD Displays/Monitors/TV's**
- **Digital camcorders/still cameras**
- **Portable DVD/MP3/GPS**
- **Camera/smart phones**
- **Mobile Computing/PDA's**

INTRODUCTION

The SMB112 is a highly integrated and flexible five-channel power manager designed for powering TFT/LCD display panels and for driving low- and high-power white-LEDs. The built-in digital programmability allows system designers to custom tailor the device to suit almost any multi-channel power supply application from digital camcorders to mobile phones.

The SMB112 integrates all the essential blocks required to implement a complete five-channel power subsystem for TFT/LCD panels including a synchronous step-down "buck" controller, two step-up "boost" controllers, one inverting "buck-boost" controller and one fixed output +3.3V LDO. Additionally sophisticated power control/monitoring functions required by complex systems are built-in. These include digitally programmable output voltage set point, individual dimming, power-up/down sequencing, enable/disable, margining and UV/OV/input/output monitoring on all channels.

The integration of features and built-in flexibility of the SMB112 allows the system designer to create a "platform solution" that can be easily modified via software without major hardware changes. Combined with the re-programmability of the SMB112 this facilitates rapid design cycles and proliferation from a base design to future generations of product.

The SMB112 is suited to battery-powered applications with an input range of +2.7V to +6.0V. Output voltages are extremely accurate (<0.5%) employing proprietary ADOC™ technology. Communication is via the industry standard I²C bus. All user-programmed settings are stored in non-volatile EEPROM of which 96 bytes may be used for general-purpose memory applications. The operating temperature range is 0C to +70C and the available package is a lead-free, Green, RoHS compliant, 32-pad QFN-32.

SIMPLIFIED APPLICATIONS DRAWING

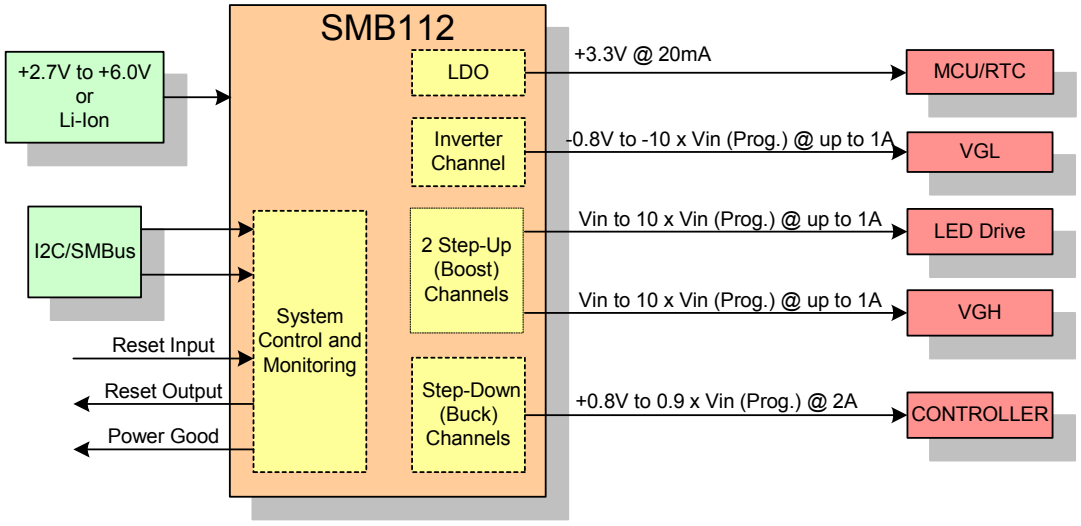

Figure 1: Applications schematic featuring the SMB112 Five-channel, programmable DC-DC controller

Note: This is an applications example only. Some pins, components and values are not shown.

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TABLE OF CONTENTS

GENERAL DESCRIPTION

The SMB112 is a fully programmable DC-DC controller that monitors, margins, and cascade sequences. It has 5 voltage outputs, consisting of: one synchronous “buck” step-down controller, two “boost” step-up controllers, one “boost-buck” negative DC-DC controller, and a 3.3V LDO. A precision 1.0 volt reference is also provided.

The SMB112 is capable of power-on/off cascade sequencing where each channel can be assigned one of four sequence positions. Supplies may also be individually powered on/off through an I^2C command or by assertion of a general purpose enable pin. Cascade sequencing, unlike time based sequencing, uses feedback to ensure that each output is valid before the next channel is enabled.

Each output voltage and the battery are monitored for under-voltage and over-voltage conditions, using a comparator based circuit. In the event of a fault, all supplies may be sequenced down, in the reverse order as power on, or immediately disabled. Multiple output status pins are provided to notify host processors or other supervisory circuits of the systems status.

The SMB112 possesses an Undervoltage Lockout (UVLO) circuit to ensure the IC will not power up until the battery voltage has reached a safe operating voltage. The UVLO function exhibits hysteresis, ensuring that noise on the supply rail does not inadvertently cause faults on the internally regulated supply.

In the event of a system fault, all monitored supplies may trigger fault actions such as power-off, or force-shutdown operations. Each output on the SMB112 may also be turned off individually at any point through an I^2C command or by the enable pin.

When used in portable applications, the SMB112 is powered from the main system battery. This input is continuously monitored for two programmable under-voltage conditions. The first monitored under voltage set point asserts a latched battery status output. Each monitored threshold can be used to assert a status output or to trigger a power off sequence.

The SMB112 is equipped with a synchronous buck outputs that use a fixed 800 kHz oscillator frequency. The feedback circuitry on the step-down channel is simplified by an internal programmable resistor divider.

The SMB112 is equipped with two boost outputs and an inverting buck-boost output. Each boost output uses a fixed 800 kHz oscillator, and an asynchronous topology reducing the necessity for an additional external MOSFET driver. All boost outputs use an external p-channel sequencing MOSFET’s to isolate the switching MOSFET from the battery when not needed.

A Low DropOut linear regulator with fixed 3.3 volt output provides a low current supply for “always on” microcontrollers. The LDO has a special input supply that is internally multiplexed between the LDO supply pin and the battery. This ensures that the LDO will always be active over the recommended operating voltages (2.7V - 6.0V).

The SMB112 provides margining control over all of its output voltages. Through an I^2C command, all outputs can be margined to any voltage setting within the nominal output voltage rage. Margining creates three pre-programmed settings that each channel can be set to via an I^2C command. Margining is ideal when used with a channel configured as an LED driver where margining provides three brightness settings. In addition, each output is slew rate limited by soft-start circuitry that is user programmable and requires no external capacitors.

All programmable settings on the SMB112 are stored in non-volatile registers and are easily accessed and modified over an industry standard I^2C serial bus. For fastest prototype development times Summit offers an evaluation card and a Graphical User Interface (GUI).

TYPICAL APPLICATION

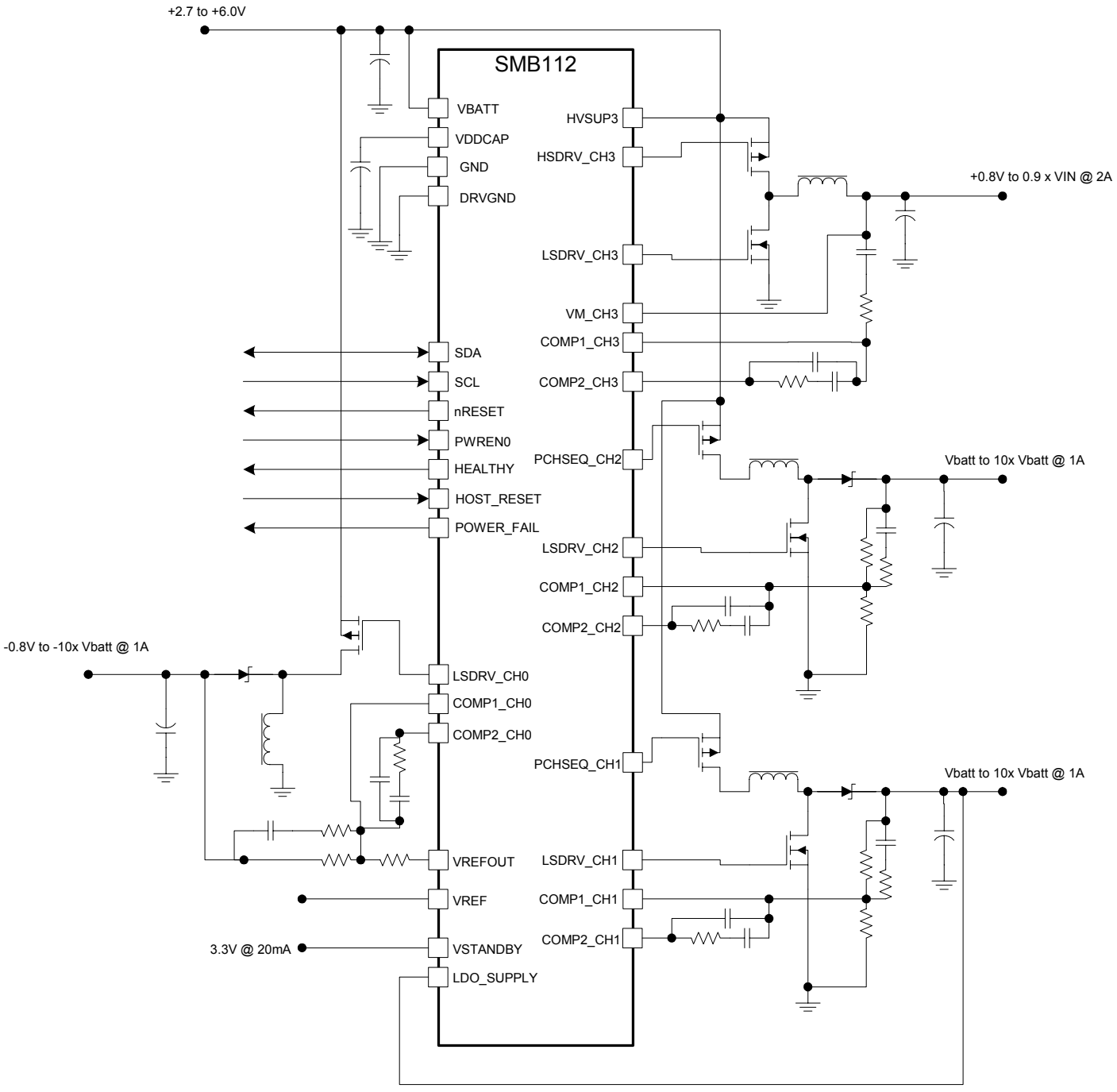


Figure 2 – Typical application schematic showing external circuitry necessary to configure the SMB112 channels as: step-up, step-down, and inverting outputs

TYPICAL APPLICATION

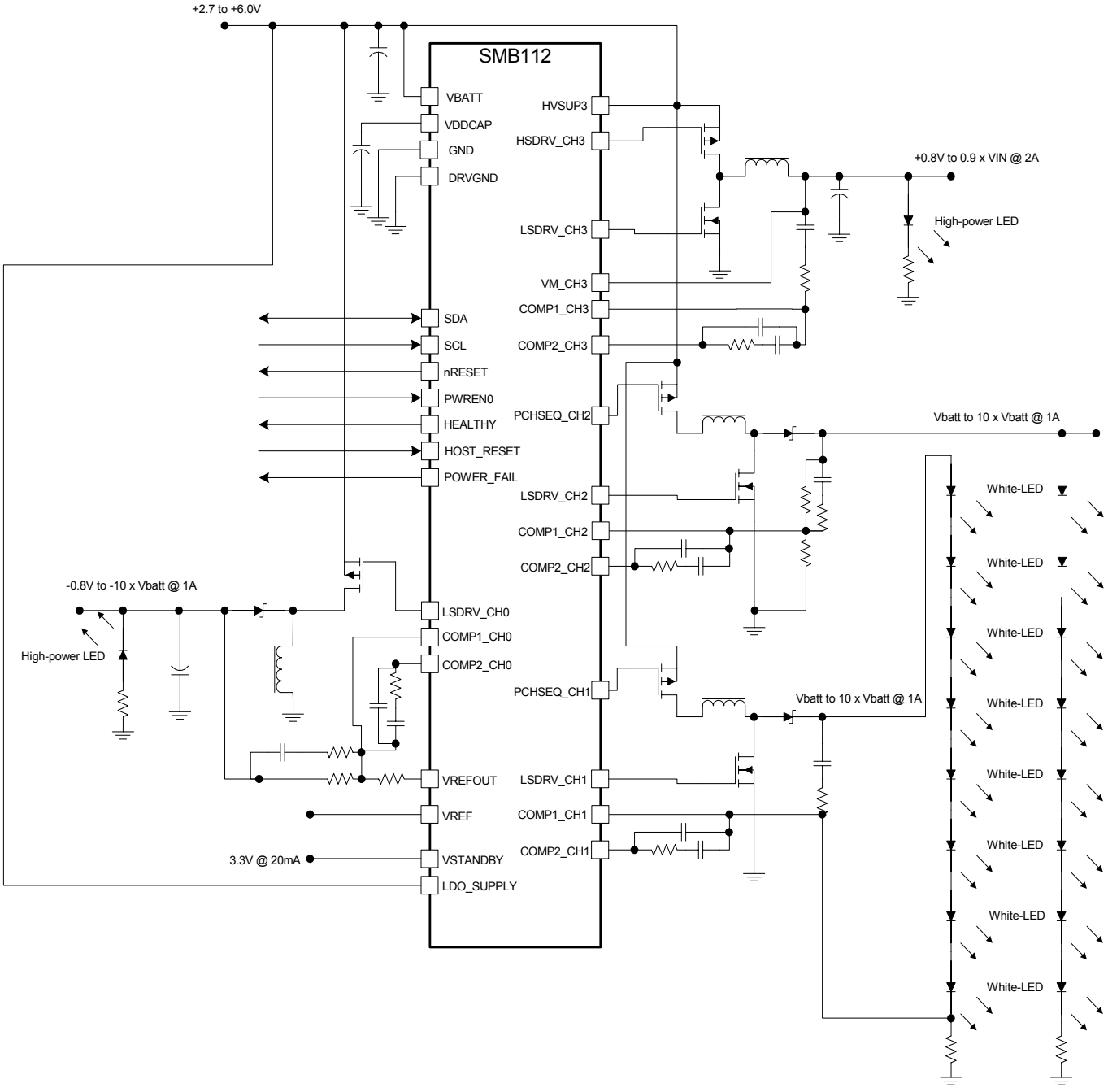


Figure 3 – Typical application schematic showing external circuitry necessary to configure the SMB112 channels as low- and high-power white-LED drivers

INTERNAL BLOCK DIAGRAM

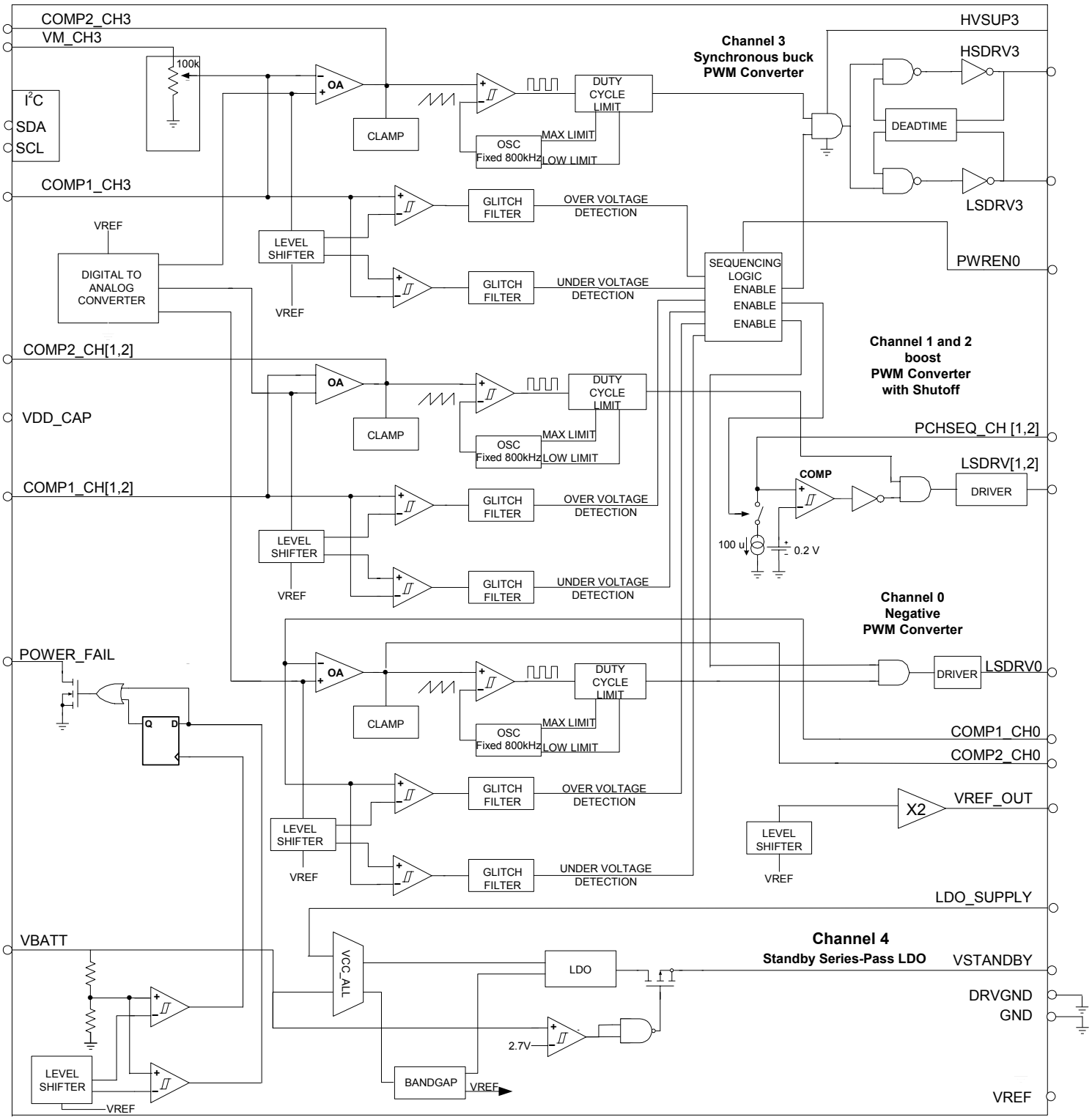


Figure 4 –SMB112 internal Block diagram. Programmable functional blocks include: level shifters, digital to analog converters and the VM_CH3 voltage dividers.

PIN DESCRIPTIONS

Pin Number	Pin Type	Pin Name	Pin Description
1	OUT	HEALTHY	The HEALTHY pin is an open drain output. High when all enabled output supplies are within the programmed levels. HEALTHY will ignore any disabled supply. There is a programmable glitch filter on the under-voltage and over-voltage sensors so that short transients outside of the limits will be ignored by HEALTHY. When used this pin should be pulled high by an external pull-up resistor.
2	I/O	SDA	SDA (Serial Data) is an open drain bi-directional pin used as the I^2C data line. SDA must be tied high through a pull-up resistor.
3	IN	SCL	SCL (Serial Clock) is an open drain input pin used as the I^2C clock line. SCL must be tied high through a pull-up resistor.
4	OUT	VREF_OUT	The VREF_OUT (Voltage Reference) pin is a precision reference output. When an inverting output is used, this pin acts as a level shifting reference for the feedback circuitry. When the inverting output is not used, this pin may be used as a precision 2.0 volt reference.
5	IN	COMP1_CH0	COMP1_CH0 (Channel 0 primary Compensation) pin is the primary feedback input of the inverting controller.
6	IN	COMP2_CH0	COMP2_CH0 (Channel 0 secondary Compensation) pin is the second feedback input of the inverting controller
7	OUT	POWER_FAIL	The POWER_FAIL pin is a latched active high open drain output. Active when voltage at VBATT falls below its programmable threshold level. The output is latched until the threshold level on the VBATT pin is exceeded and either an I^2C clear command is issued or the battery voltage is cycled off and on. After the latch is cleared a timeout period of 3.0-4.5 ms will pass before POWER_FAIL becomes inactive The trip point level is user programmable from 2.55-3.6V in 150 mV increments This pin should be pulled high though a pull-up resistor.
8	OUT	LSDRV_CH0	The LSDRV_CH0 (Channel 0 Low-side Driver) pin is the switching node of the inverting buck-boost controller. The output of this pin should be attached to the gate of an external p-channel MOSFET driver.
9	IN	HOST_RESET	The HOST_RESET pin is an active high reset input. When this pin is asserted high, the nRESET output will immediately go low. When HOST_RESET is brought low, nRESET will go high after a programmed reset delay.
10	CAP	VDD_CAP	The VDD_CAP (VDD Capacitor) pin is an external capacitor input used to filter the internal supply.
11	PWR	VBATT	Power supply to part.
12	OUT	PCHSEQ_CH1	The PCHSEQ_CH1 (Channel 1 Sequence) pin is attached to an external p-channel MOSFET and is used to enable the corresponding channel 1 boost controller. PCHSEQ_CH1 uses an internal 100μA current sink for sequencing. This pin should be pulled high through a parallel RC connection.

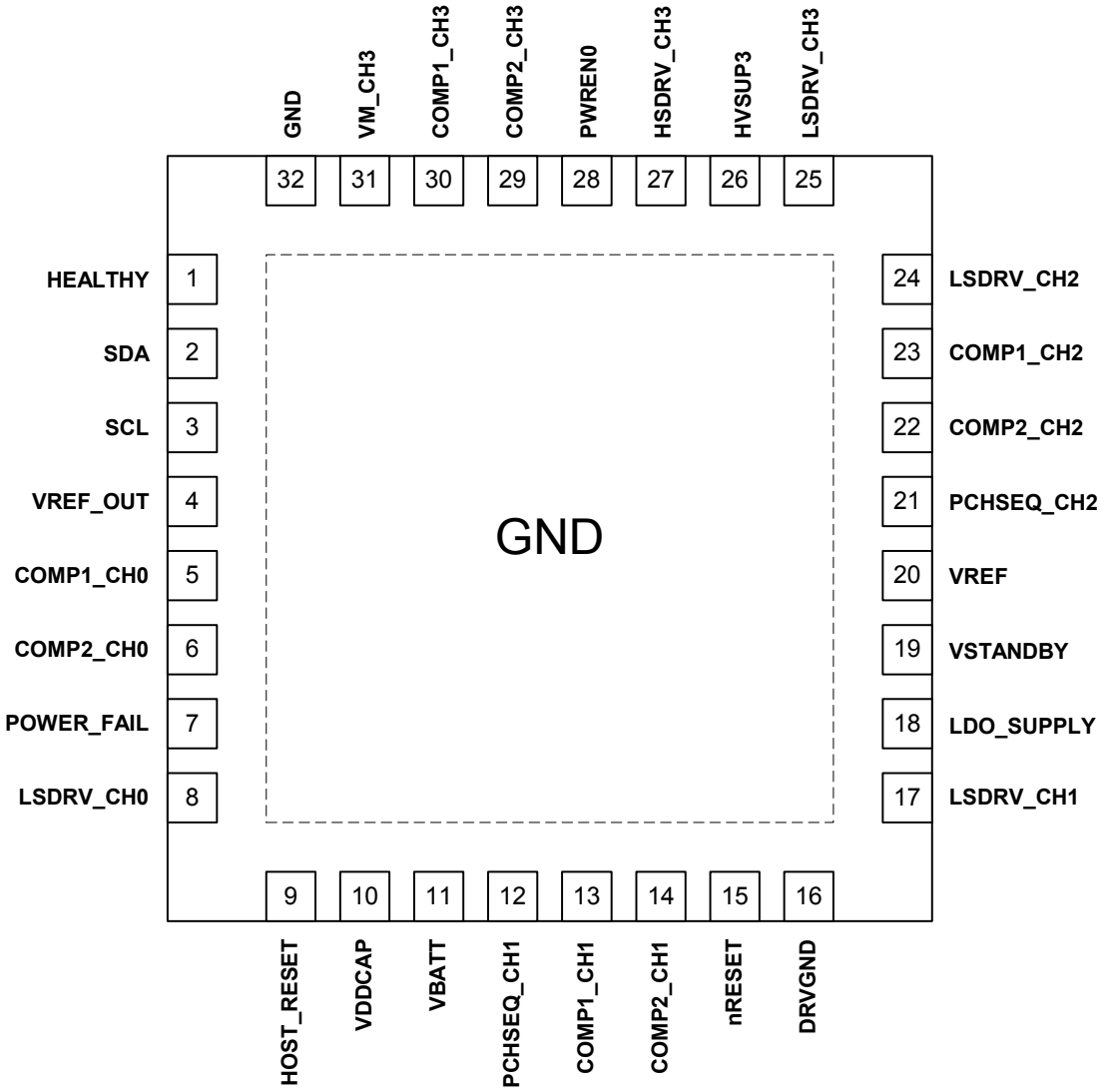
PIN DESCRIPTIONS

Pin Number	Pin Type	Pin Name	Pin Description
13	IN	COMP1_CH1	The COMP1_CH1 (Channel 1 primary Compensation) pin is the primary compensation input of the channel 1 step-up boost controller.
14	IN	COMP2_CH1	The COMP2_CH1 (Channel 1 secondary Compensation) pin is the second compensation input of the channel 1 step-up boost controller.
15	OUT	nRESET	The nRESET (Reset) pin is an active low open drain output. Active when the SMB112 is powered up. Remains low for a user programmable period of 25, 50, 100, or 200 ms after all enabled supplies have exceeded their programmed thresholds. When used, this pin should be pulled high by an external pull up resistor.
16	PWR	DRVGND	DRGND (Driver Ground). The DRGND pin should be attached externally to ground through a short wide wire.
17	OUT	LSDRV_CH1	The LSDRV_CH1 (Channel 1 Low-side Driver) pin is the lower switching node of the synchronous step-down boost controller. This pin attaches to an external n-channel MOSFET
18	PWR	LDO_SUPPLY	The LDO_ SUPPLY pin powers the 3.3V VSTANDBY LDO output. The LDO_ SUPPLY pin should be connected to the output of a boost output (usually the intermediate bus). When the battery voltage drops below the POWER_FAIL threshold, this pin will no longer supply the LDO. Do not apply a voltage in excess of the recommended input voltage to this pin.
19	OUT	VSTANDBY	The VSTANDBY (Voltage Standby) pin is a 3.3V LDO output. VSTANDBY is supplied from the output of the intermediate bus through the LDO_SUPP pin. When PWR_FAIL is asserted an internal analog multiplexer will power VSTANDBY directly from the VBATT pin.
20	OUT	VREF	The VREF (Voltage Reference) pin is a precision 1.0 volt output reference.
21	OUT	PCHSEQ_CH2	The PCHSEQ_CH2 (Channel 2 Sequence) pin is attached to an external p-channel MOSFET and is used to enable the corresponding channel 2 boost controller. PCHSEQ_CH2 uses an internal 100μA current sink for sequencing. This pin should be pulled high through a parallel RC connection.
22	IN	COMP2_CH2	The COMP2_CH2 (Channel 2 secondary Compensation) pin is the second compensation input of the channel 2 step-up boost controller.
23	IN	COMP1_CH2	The COMP1_CH2 (Channel 2 primary Compensation) pin is the primary compensation input of the channel 2 step-up boost controller.
24	OUT	LSDRV_CH2	The LSDRV_CH2 (Channel 2 Low-side Driver) pin is the lower switching node of the synchronous step-down boost controller. This pin attaches to an external n-channel MOSFET
25	OUT	LSDRV_CH3	The LSDRV_CH3 (Channel 3 Low-side Driver) pin is the lower switching node of the channel 3 synchronous step-down buck controller. Attaches to the gate of n-channel MOSFET.
26	PWR	HVSUP3	Channel 3 High Voltage Supply for Channel 3 buck driver.
27	OUT	HSDRV_CH3	The HSDRV_CH3 (Channel 3 High-side Driver) pin is the upper switching node of the channel 3 synchronous step-down buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH3 and assertion of LSDRV_CH3 to prevent excessive current flow during switching.

PIN DESCRIPTIONS			
Pin Number	**Pin Type**	**Pin Name**	**Pin Description**
28	IN	PWREN0	The PWREN0 (Power Enable 0) pin is a programmable input used to enable (disable) selected supplies. When unused this pin should be tied to a solid logic level.
29	IN	COMP2_CH3	The COMP2_CH3 (Channel 3 secondary Compensation) pin is the secondary compensation input of the channel 3 step-down buck controller.
30	IN	COMP1_CH3	The COMP1_CH3 (Channel 3 primary Compensation) pin is the primary compensation input of the channel 3 step-down buck controller. Each pin is internally connected to a programmable resistor divider.
31	IN	VM_CH3	The VM_CH3 (Channel 3 Voltage Monitor) pin connects the channel 3 step-down controller output. Internally the VM_CH3 pin connects to an internal programmable resistor divider.
32	PWR	GND	Ground
PAD	PWR	GND	The bottom slug of the SMB112 should be attached to a ground pad

PACKAGE AND PIN DESCRIPTION

Top view
SMB112
5mm x 5mm QFN-32



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Terminal Voltage with Respect to GND:
VBATT Supply Voltage ..... -0.3V to +6.5V
HVSUP Supply Voltage ..... -0.3V to +6.5V
LDO_SUPPLY ..... -0.3V to +6.5V
All Others ..... -0.3V to VBATT
Output Short Circuit Current 100mA
Reflow Solder Temperature (30 secs)..... 260°C
Junction Temperature..... 150°C
ESD Rating per JEDEC 2000V
Latch-Up testing per JEDEC.....±100mA

RECOMMENDED OPERATING CONDITIONS

Commercial Temperature Range..... 0°C to +70°C
VBATT Supply Voltage .....2.7V to +6.0V
HVSUP Supply Voltage.....2.7V to +6.0V
LDO_SUPPLY.....GND to +6.0V
All Others.....GND to VBATT
Package Thermal Resistance (θ_{JA})
32 Lead QFN. ……..……..……..…TBD
Moisture Classification Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention ..... 100 Years
Endurance.....100,000 Cycle

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Input supply voltage	Input supply voltage (operational)	2.7		6.0	V
V_{LDO_SUPP}	Linear regulator supply voltage	Internally multiplexed with VBATT	2.7		6.0	V
V_{HVSUP}	Regulator supply voltage		2.7		6.0	V
V_{UVLO}	Undervoltage lockout	VBATT rising		2.2		V
		VBATT falling		2.0		
$I_{DD\text{-}MONITOR}$	Monitoring current	All voltage inputs monitored. No supplies switching, VBATT at 4.2V, LDO on with no output enabled			330	µA
I_{SD}	Switching current per Buck output enabled	Current drawn when one output switching		1200		µA
$I_{DD\text{-}ACTIVE}$	Total current all channels switching.	VBATT at 4.2V		2.15		mA
$V_{REF(INT)}$	Internal voltage reference		0.995		1.005	V
Voltage Reference						
$V_{REF(EXT)}$	External voltage reference on VREF output pin	At 1.0 V	0.99	1.0	1.01	V
ΔV_{LOAD}	Load regulation	10uA<Iref<200uA		100		mV
ΔV_{LINE}	Line regulation	2.7V<VBATT <4.2V		0.01		mV
TS	Temperature stability			0.4		%

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
f_{OSC}	Oscillator frequency			800		kHz
Δf_{OSC}	Oscillator frequency accuracy		-10		+10	%
O_{PP}	Oscillator peak to peak[1]			1		V
Δf_{SV}	Frequency stability for voltage			0.1		%/V
Δf_{ST}	Frequency stability for temperature			0.04		%/°C
Error Amplifier						
V_{ACC}	Threshold Voltage accuracy			0.2		%
TS	Temperature stability			0.2		%
A_{VOL}	Open loop voltage Gain	At DC		60		dB
BW	Frequency bandwidth	At AV=0 dB		30		MHz
I_{SOURCE}	Output source current	At 0.5V		20		µA
I_{SINK}	Output sink current	At 0.5V		800		µA
LDO						
V_{OUT}	Nominal output voltage	LDO_SUPPLY = 4.2V, I_{LOAD}=0A		3.3		V
ΔV_{OUT}	Output voltage accuracy	Percent of 3.3V output @ 10mA, LDO_SUPPLY = 4.2V		0.3		%
ΔV_{LOAD}	Load regulation error			0.3		%/V
ΔV_{LINE}	Line regulation error	No load		0.17		%/mA
PSRR	Power supply rejection ratio	20log(Vout/Vin) @10kHz		50		dB
I_Q	Quiescent current	VBATT = 4.2V, I_{LOAD}=0A		50		µA
V_{DO}	Dropout voltage	I_{OUT} = 1 mA		20		mV
		I_{OUT} = 5 mA		100		
		I_{OUT} = 10 mA		200		
		I_{OUT} = 15 mA		300		
		I_{OUT} = 20 mA		400		
I_{LIMIT}	Maximum output current				40	mA
V_N	Output Noise voltage	Peak to peak		1		mV

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output Block (CH0)						
V_{OUT}	Programmable voltage set point range	VBATT=4.2V, I_{LOAD}=0	-35		-0.5	V
ΔV_{OUT}	Output accuracy	Excluding external resistor divider accuracy		0.5		%
V_{COMP1}	Feedback voltage reference	COMP1 pin		1.0		V
ΔV_{COMP1}	Feedback voltage reference accuracy	COMP1 pin	-0.2		+0.2	%
R_{ON}	LSDRV Output ON resistance	R_{OH}		17		Ω
		R_{OL}		3		
D.C.	LSDRV Duty Cycle	High	85		95	%
		Low	5		15	
V_{REF_OUT}	Level shift voltage reference	VREF_OUT pin programmable in 8mV steps	1		2	V
ΔV_{REF_OUT}	Level shift voltage reference accuracy	VREF_OUT pin	-0.3		+0.3	%
I_{REF_OUT}	VREF_OUT source current	VREF_OUT = 1.5V			100	µA
ML	Minimum load[1]	L=33uF, V_O=-7.5V, V_{IN}=4.2V, V_D=0.3V		10.1		kΩ
Output Block Channels 1 and 2						
V_{OUT}	Programmable voltage set point range	VBATT=4.2V, I_{LOAD}=0	4.5		35	V
ΔV_{OUT}	Output accuracy	Excluding external resistor divider accuracy		0.5		%
R_{DRVH}	HSDRV ON resistance	Output high		17		Ω
		Output low		3		
D.C.	Duty Cycle	High	85		95	%
		Low	5		15	
V_{COMP1}	Feedback voltage reference	COMP1 pin Programmable in 4mV steps		1.0		V
ΔV_{COMP1}	Feedback voltage reference accuracy	COMP1 pin	-0.5		+0.5	%
ML	Minimum load[2]	L=33uF, V_O=12V, V_{IN}=4.2V, V_D=0.3V		29		kΩ
I_{PCHSEQ}	PCHSEQ sink current		50		100	µA
EN_{TH}	Enable threshold	Voltage on PCHSEQ pin when LSDRV output is enabled		200		mV

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output Block Channel 3						
V_{OUT}	Voltage nominal set point range	VBATT=4.2V, I_{LOAD}=0	0.5		3.8	V
		VBATT= 6.0V, I_{LOAD}=0	0.6		5.4	
ΔV_{OUT}	Output accuracy	Including internal resistor divider		0.5		%
R_{DRVH}	HSDRV ON resistance	Output high		8		Ω
		Output low		8		
R_{DRVL}	LSDRV ON resistance	Output high		17		
		Output low		3		
V_{COMP1}	Feedback voltage reference	COMP1 pin Programmable in 4mV steps		1.0		V
ΔV_{COMP1}	Feedback voltage reference accuracy	COMP1 pin	-0.5		+0.5	%
D.C.	Duty Cycle	High	85		95	%
		Low	5		15	
Logic levels						
V_{IH}	Input high voltage			0.9xVDD		V
V_{IL}	Input low			0.1xVDD		V
V_{OL}	Open drain outputs	I_{SINK} = 1mA	0		0.4	V
I_{OL}	Output low current		0		1.0	mA
Programmable Monitoring Thresholds						
V_{PUV1}	Programmable UV1 threshold	Programmable UV1 threshold voltage measured on VBATT pin in 150 mV increments	2.55		3.60	V
ΔV_{PUV1}	UV1 accuracy		-20		+20	mV
V_{PPFTH}	Programmable POWER_FAIL threshold	Programmable in 150 mV increments	2.55		3.60	V
ΔV_{PPFTH}	POWER_FAIL accuracy		-20		+20	mV
P_{UVTH}	Programmable under voltage threshold	For channels 0-3. Relative to nominal set point voltage		-5		%
				-10		
				-15		
				-20		
P_{OVTH}	Programmable over voltage threshold	For channels 0-3. Relative to nominal set point voltage		+5		%
				+10		
				+15		
				+20		

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{UVTH}	Programmable under voltage threshold[4]	For channel 0. V_O=-7.5V, R1=392K, R2=33.2K		-6.2		%
				-12.4		
				-18.6		
				-24.8		
P_{OVTH}	Programmable over voltage threshold[5]	For channel 0. V_O=-7.5V, R1=392K, R2=33.2K		+6.2		%
				+12.4		
				+18.6		
				+24.8		

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PPTO}	Programmable power-On sequence timeout period.	Programmable power-On sequence position to sequence position delay.	1.3	1.5	1.7	ms
			10.6	12.5	14.4	
			21.3	25	28.8	
			42.5	50	57.5	
t_{DPOFF}	Programmable power-off sequence timeout period.	Programmable power-off sequence position to sequence position delay.	1.3	1.5	1.7	ms
			10.6	12.5	14.4	
			21.3	25	28.8	
			42.5	50	57.5	
t_{PRTO}	Programmable reset time-out delay	Programmable time following assertion of last supply before nRESET pin is released high.	21.3	25	28.8	ms
			42.5	50	57.5	
			85.0	100	115.0	
			170.0	200	230.0	
t_{PST}	Programmable sequence termination period	Time between active enable in which corresponding outputs must exceed there programmed under voltage threshold. If exceeded, a force shutdown will be initiated.		OFF		ms
			42.5	50	57.5	
			85.0	100	115.0	
			170.0	200	230.0	
t_{PFTO}	POWER_FAIL timeout period	Timeout begins after latch is cleared.	3.2	3.75	4.3	ms
t_{PGF}	Programmable glitch filter	Period for which fault must persist before fault triggered actions are taken. Present on all buck, boost, and inverting supplies.		0		µs
			6.8	8	9.2	

1. The minimum load for Boost channels is defined by the following equation: where VO = Programmed output voltage, VIN =P-Channel MOSFET source voltage, L = inductance, Vd = forward diode drop (0.6V silicon, 0.3V Schottky)

$$Rmax = \frac{2*L*Vout*(Vout - VIN + Vd)}{VIN^{2}*1.25E-8}$$

2. The minimum load for the Inverting Boost-Buck channel is defined by the following equation: where V_O = Programmed output voltage, VIN =P-Channel MOSFET source voltage, L = inductance, Vd = forward diode drop (0.6V silicon, 0.3V Schottky). Lesser values may exist

$$Rmax = \frac{2*L*Vout*(Vout - Vd)}{VIN^{2}*1.25E-8}$$

3,4. The Channel 0 programmable over voltage setting is calculated from the following formula: where VREF_OUT is the voltage o the VREF_OUT pin and R1 and R2 are the upper and lower resistors in the external voltage divider, n corresponds to the available user programmable settings

$$\text{Ch 0 } P_{UVTH} = -100n\left[1 - \left[\frac{V_{REF\_OUT} - .95(1+R2/R1)}{V_{REF\_OUT} - (1+R2/R1)}\right]\right]\% \quad n= 1,2,3,4 \text{ , Ch 0 } P_{OVTH} = 100n\left[1 - \left[\frac{V_{REF\_OUT} - .95(1+R2/R1)}{V_{REF\_OUT} - (1+R2/R1)}\right]\right]\% \; n= 1,2,3,4$$

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
SR_{REF}	Programmable slew rate reference	Adjustable slew rate factor proportional to output slew rate.	340.0	400	460.0	V/s
			170.0	200	230.0	
			85.0	100	115.0	
			56.7	66.7	76.7	
			42.5	50	57.5	
			28.3	33.3	38.3	
			21.3	25	28.8	
			17.0	20	23.0	
Output Block Channel 0						
t_{RH}	HS Driver output rise time	C_G=100pF, V_{DD}=4.2V		10		ns
t_{FH}	HS Driver output fall time	C_G=100pF, V_{DD}=4.2V		10		ns
Output Block Channels 1 and 2						
t_{RL}	LS Driver output rise time	C_G=100pF, V_{DD}=4.2V		10		ns
t_{FL}	LS Driver output fall time	C_G=100pF, V_{DD}=4.2V		10		ns
Output Block Channel 3						
t_{RL}	LS Driver output rise time	C_G=100pF, V_{DD}=4.2V		10		ns
t_{FL}	LS Driver output fall time	C_G=100pF, V_{DD}=4.2V		10		ns
t_{RH}	HS Driver output rise time	C_G=100pF, V_{DD}=4.2V		15		ns
t_{FH}	HS Driver output fall time	C_G=100pF, V_{DD}=4.2V		5		ns
t_{DT}	Driver non-overlap delay	High to low transition on HSDRV			20	ns
		Low to high transition on buck HSDRV			10	

I²C-2 WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS –100 kHz

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	100kHz			
			Min	Typ	Max	Units
f_{SCL}	SCL clock frequency		0		100	kHz
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period		4.0			µs
t_{BUF}	Bus free time	Before new transmission - Note **1/**	4.7			µs
$t_{SU:STA}$	Start condition setup time		4.7			µs
$t_{HD:STA}$	Start condition hold time		4.0			µs
$t_{SU:STO}$	Stop condition setup time		4.7			µs
t_{AA}	Clock edge to data valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data output hold time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA rise time	Note **1/**			1000	ns
t_F	SCL and SDA fall time	Note **1/**			300	ns
$t_{SU:DAT}$	Data in setup time		250			ns
$t_{HD:DAT}$	Data in hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t_{WR_CONFIG}	Write cycle time config	Configuration registers			10	ms
t_{WR_EE}	Write cycle time EE	Memory array			5	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

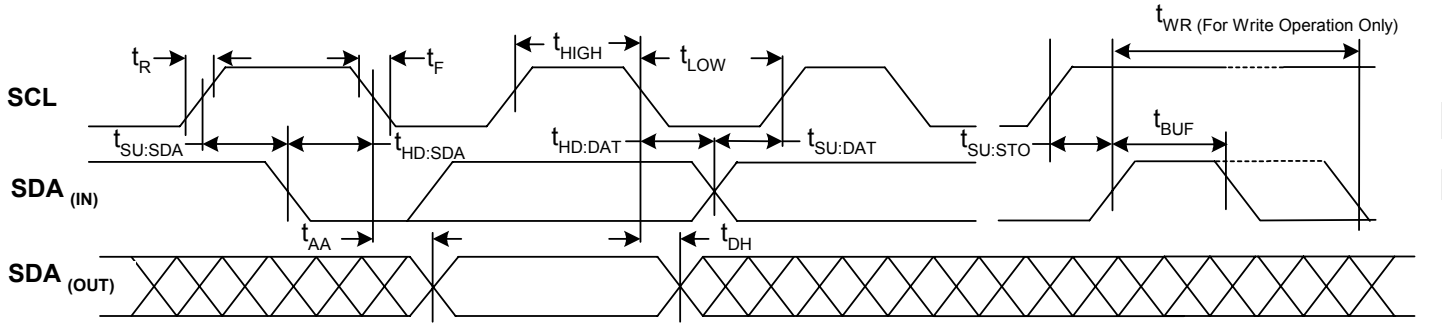
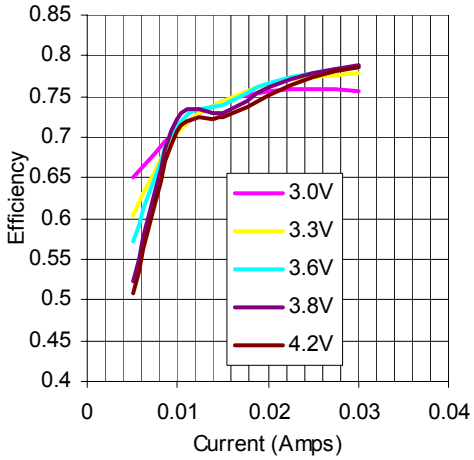


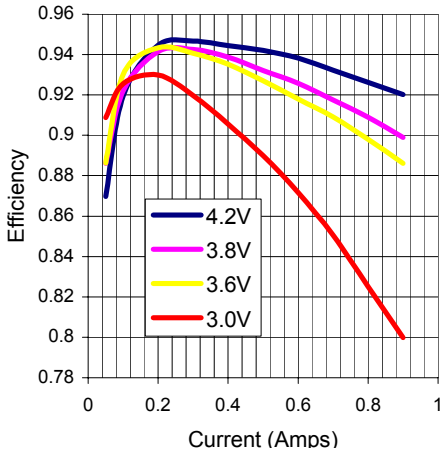
Figure 5 – I²C timing diagram

EFFICIENCY GRAPHS

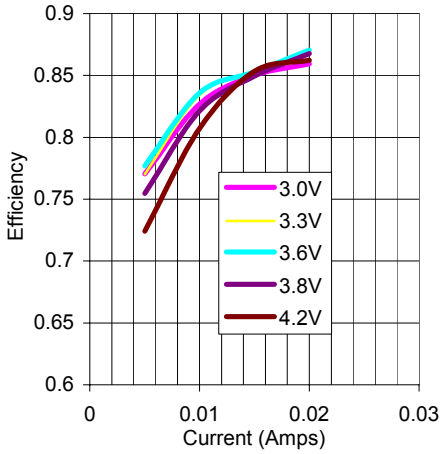
Inverting –7.5 Volts



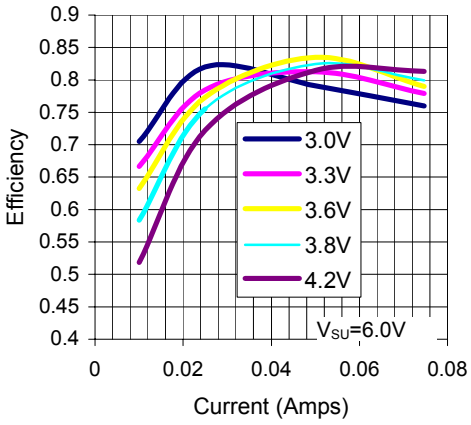
Boost 6.0 Volts



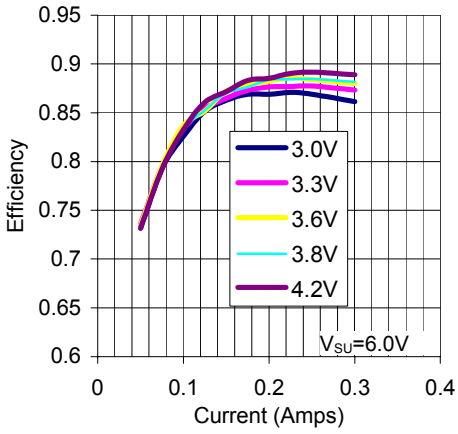
Boost 12.0 Volts



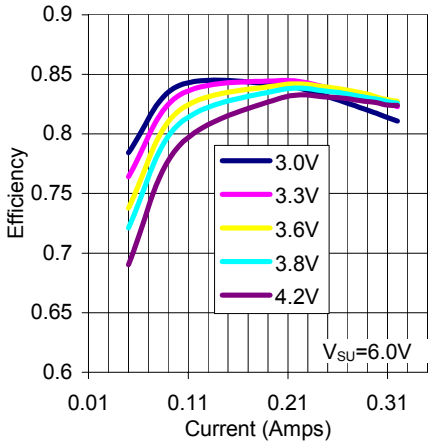
Buck (SU + SD) 3.3 Volts



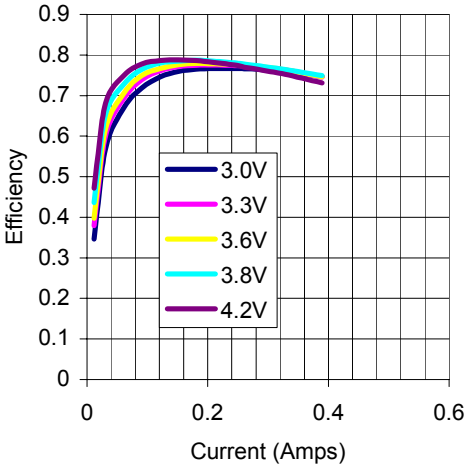
Buck (SU + SD) 5.0 Volts



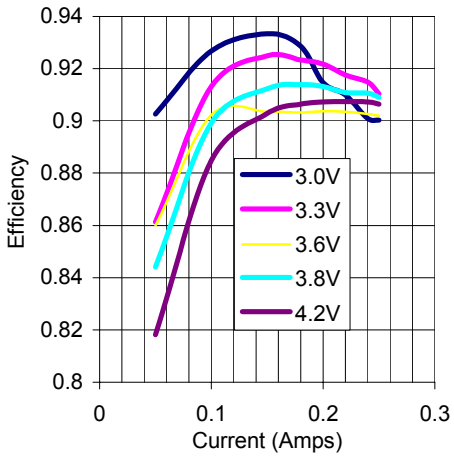
Buck (SU + SD) 3.0 Volts



Buck 1.2 Volts



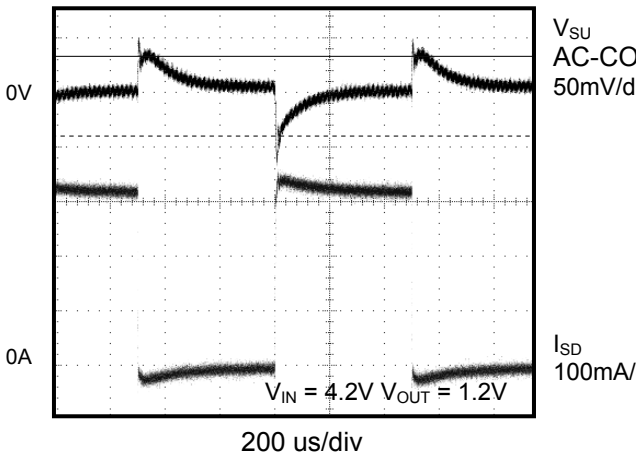
Buck 2.5 Volts



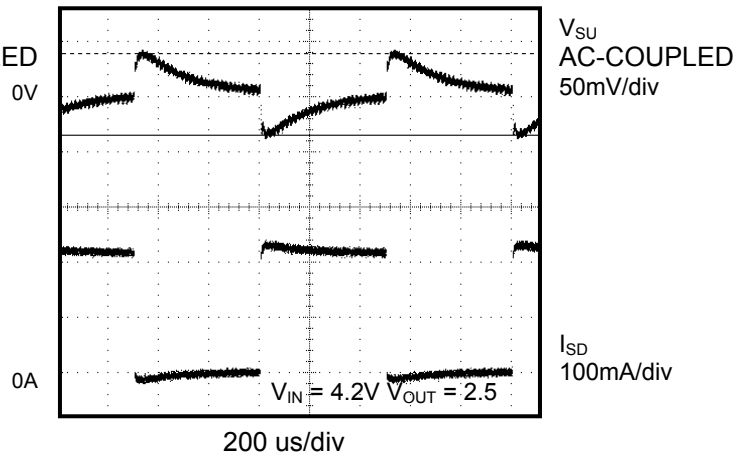
(All measurements are taken at 25°C, and are based on the Applications Schematic.)

TRANSIENT RESPONSE

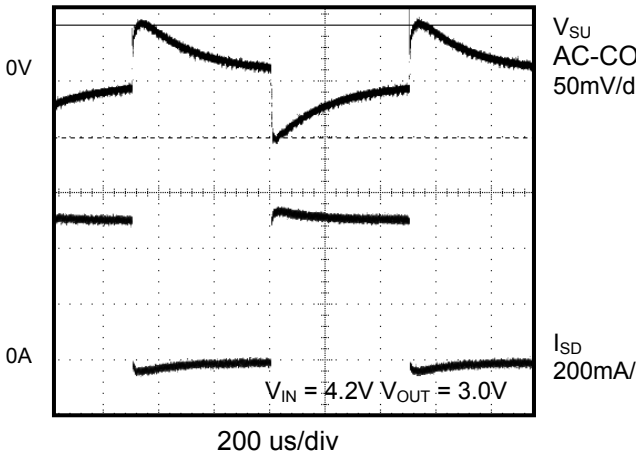
BUCK TRANSIENT RESPONSE



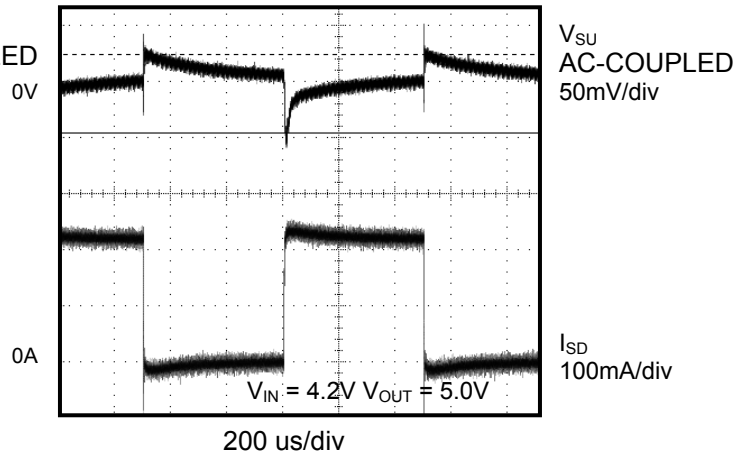
BUCK TRANSIENT RESPONSE



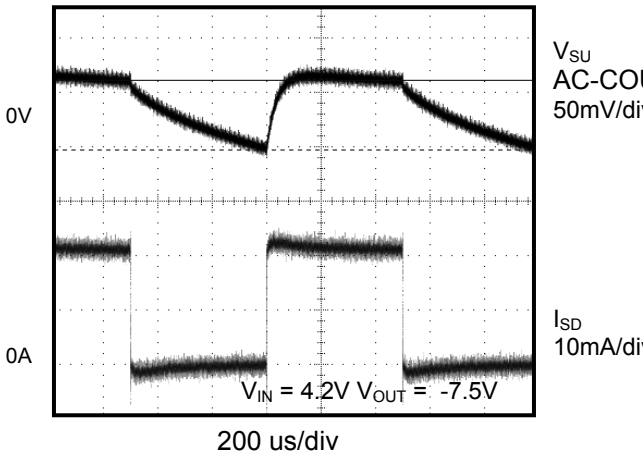
BUCK TRANSIENT RESPONSE



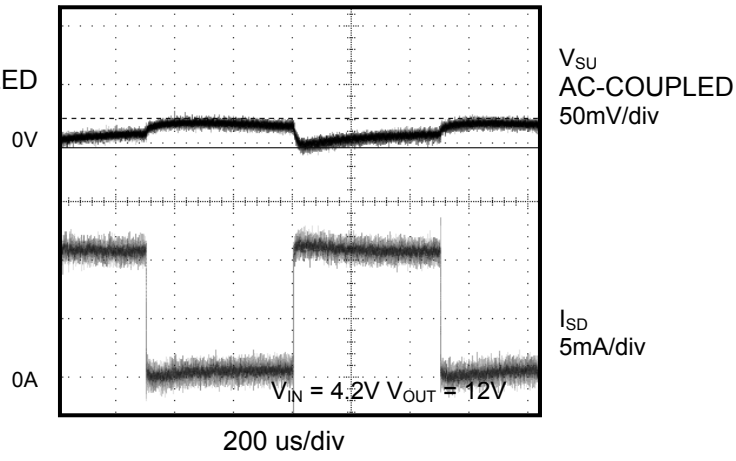
BOOST TRANSIENT RESPONSE



INVERTING TRANSIENT RESPONSE



BOOST TRANSIENT RESPONSE



(All measurements are taken at 25°C, and are based on the Applications Schematic.)

TIMING DIAGRAMS: POWER-ON SEQUENCE

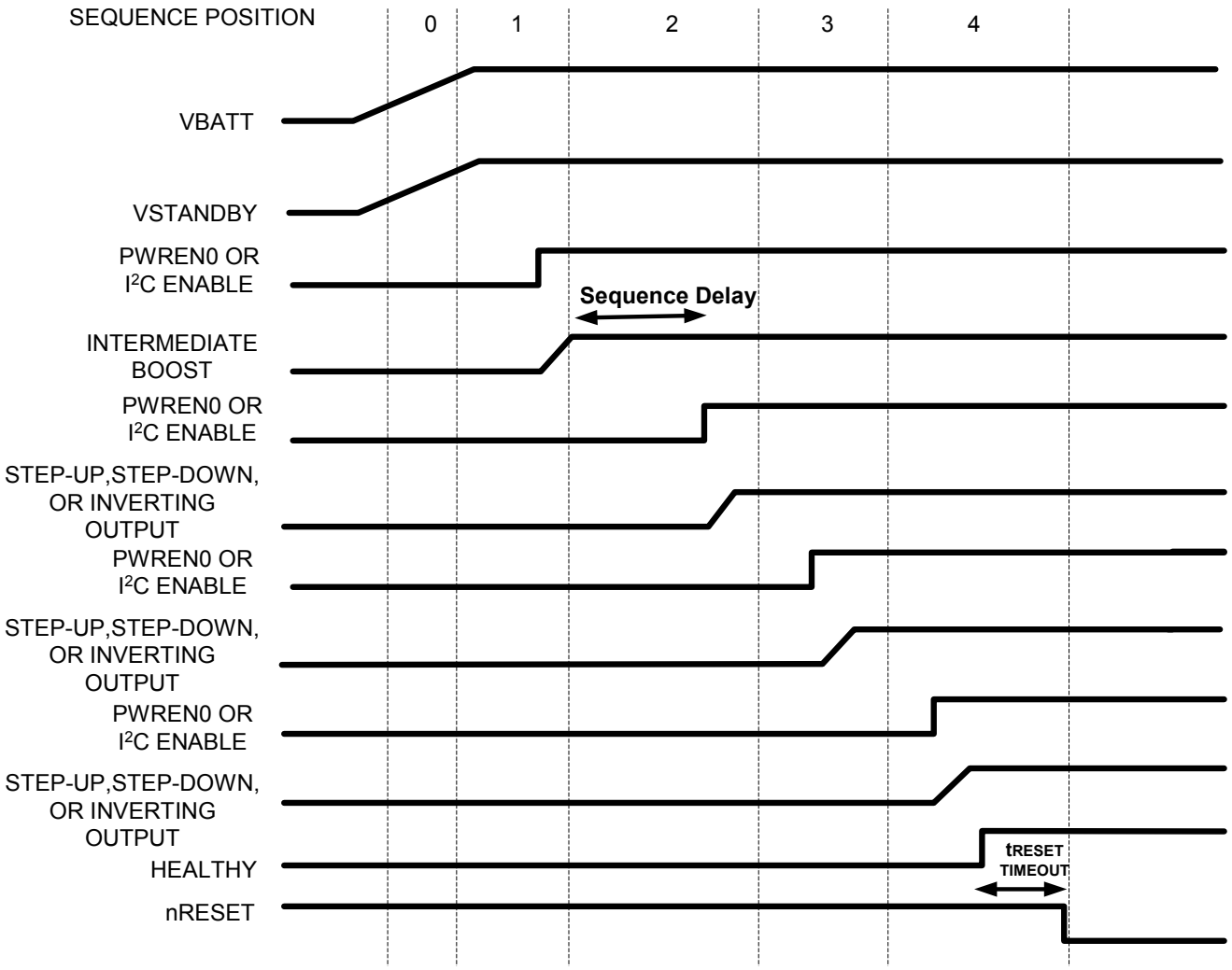


Figure 6 – SMB112 power on sequence. Any PWM channel may be enabled or disabled through an I²C command or by the PWREN0 pin.

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMB112 can be powered from an input voltage between 2.7-6.0 volts applied between the VBATT pin and ground. The SMB112 is optimized for use with a rechargeable single cell Lithium ion battery, The input voltage applied to the VBATT pin is internally regulated and used as an internal VDD supply. The VBATT pin is monitored by an UnderVoltage Lockout (UVLO) circuit, which prevents the device from turning on when the voltage at this node is less than the UVLO threshold.

POWER-ON/OFF CONTROL

The outputs on the SMB112 can be turned on in one of two ways: by an I^2C **Power on** command or via a programmable bit is set to initiate the power on process when the UVLO threshold is exceeded. In addition, after a power-off or force-shutdown condition occur due to a under voltage fault on the battery the SMB112 can optionally restart once the fault condition is cleared. If a power-off or force-shutdown occurs due to a UV or OV fault on any PWM channel, a sequence termination, or due to an I^2C command, a restart will only occur if the power-on pin is toggled or an I^2C **Power on** command is issued.

ENABLE

Once a power on command has been issued, the power on process can be controlled by means of an enable signal. Each channel can be controlled by one of four enable signals and the assignment type can be mixed and matched for each of the four channels. The enable signal can stall the power-on process until the enable is valid, or disable a controller once all supplies have been enabled. There are two ways to generate the enable signal; the first approach allows the enable signal to be assigned the PWREN0 pin, and the second approach allows the enable to be controlled by the contents of a volatile register that can be written to at any time. This volatile register will be automatically initialized once the UVLO threshold has been exceeded to a known programmed state.

POWER-ON SEQUENCING

Each channel on the SMB112 may be placed in any one of four unique sequence positions. To provide programmable order, the SMB112 navigates between these sequence positions using a feedback-based cascade-sequencing circuit. Cascade sequencing is the process in which each channel is continually compared against a programmable reference voltage until the voltage on the monitored channel exceeds the reference voltage, at which point an internal sequence position counter is incremented and the next sequence position is entered.

Once power-on sequencing has been initiated, automated sequencing may commence in one of three ways (Figure 6): normal sequencing, sequencing with enable, and sequencing with channel bypass. In addition, each channel may be powered on in a manual mode, independent of the sequence position. The power-on sequencing mode selection is programmable over the I^2C bus and stored in the non-volatile memory.

NORMAL CASCADE SEQUENCING

During *Normal Sequencing*, the sequence position counter is initialized to the first sequence position (position 1), each channel occupying this position then waits an individual programmable timeout period (t_{PPTO}) of 1.5, 12.5, 25, or 50 ms. Once enabled, all channels occupying the first sequence position will begin a soft-start. As the output voltage of the channel is ramped up, it is monitored by a comparator based, user programmable, under-voltage threshold sensor. After this threshold is exceeded, indicating that the selected channel(s) have reached their nominal operating range the sequence position counter is incremented, and fault monitoring begins for that channel. Once all channels occupying the first sequence position have surpassed their under-voltage thresholds, the power-on delay for the next sequence position will begin. This process continues until all channels have been sequenced on and are above their under-voltage threshold.

SEQUENCING WITH ENABLE

During the *Sequencing With Enable* mode, sequencing commences as with the *Normal Sequencing*, except that prior to a channel beginning to soft-start, the enable corresponding to that channel must be asserted. In the event that the enable is not asserted, sequencing will halt indefinitely until a valid enable is provided. Once a valid enable is provided, a soft-start function will begin for that channel. This process will continue until all channels occupying the first sequence position are above their under-voltage settings, at which point the sequence position counter will be incremented.

SEQUENCING WITH CHANNEL BYPASS

When the *Sequencing With Channel Bypass* mode is selected, sequencing will commence as with the *Sequencing With Enable*, except that if the enable signal is not asserted by the end of the power-on delay period, that channel will be bypassed. If no other channels occupy the current sequence position, the sequence position counter will be incremented beginning the power-on delay for all channels in the

APPLICATIONS INFORMATION (CONTINUED)

next sequence position. Once a channel has been bypassed, it may still be enabled any time prior to a power off operation.

MANUAL MODE

The SMB112 also provides a manual power-on mode in which each channel may be enabled individually irrespective of the state of other channels. In this mode, the enable has complete control over the channel, and all sequencing is ignored. In Manual mode channels will not be disabled in the event of a fault.

POWER OFF OPTIONS

FORCE-SHUTDOWN

When a battery fault occurs, a UV or OV is detected on any PWM channel, or an I^2C force-shutdown command is issued, all channels will be immediately disabled.

SEQUENCE TERMINATION TIMER

At the beginning of each sequence position, an internal programmable timer will begin to time out. When this timer has expired, the SMB112 will automatically perform a force-shutdown operation. This timer is user programmable with a programmable sequence termination period (t_{PST}) of 50,100, 200 ms; this function can also be disabled.

POWER OFF SEQUENCING

The SMB112 has a power-off sequencing operation. During a power off operation the supplies will be powered off in the reverse order they where powered on in. During the power off sequencing, all enables are ignored.

When a power-off command is issued the SMB112 will set the sequence position counter to the last sequence position and disable that channel without soft-start control; once off, the power off delay for the channel(s) in the next to last sequence position will begin to timeout, after which that channel(s) will be disabled. This process will continue until all channels have been disabled and are off. The programmable power-off sequence timeout period (t_{DPOFF}) can be set to 1.5, 12.5, 25, or 50 ms.

If a channel fails to turn off within the sequence termination period, the sequence termination timer will initiate a force shutdown, if enabled.

MONITORING

The SMB112 monitors all 4 PWM outputs for under-voltage (UV) and over-voltage (OV) faults. The monitored levels are user programmable, and may be set at 5,10, 15, and 20 percent of the nominal output voltage.

Each output possesses a glitch filter to ensure that short violations in the UV or OV settings will not result in a fault-triggered action. All glitch filters on the SMB112 are user programmable and may be set to either 0 or 8 µs.

In the event that one or more channels violate their respective UV/OV setting for a period exceeding that specified by the glitch filter, all channels (not set to Manual mode) can optionally be powered off and-or, the healthy pin can be triggered. The programmable power off conditions that may result from a threshold violation include the immediate power off all supplies (force-shutdown) or the sequence of all supplies off.

Monitoring is accomplished by a comparator-based approach, in which a programmable voltage reference is compared against the monitored signal. Each channel possesses a dedicated reference voltage generated by a programmable level shifting digital to analog converter. Each of which can be set from 0-1.0 volts in 4mV increments.

BATTERY MONITORING

The battery voltage is monitored for two user programmable UV settings via the VBATT pin. These two programmable threshold levels are intended to prevent the outputs, once disabled, from turning on due to a reduced load on the battery.

The two user programmable voltage-monitoring levels, UV1 and UV2 should be programmed to two different levels; the first level UV1 being the largest and the second, UV2, being the smaller of the two.

Battery voltage, like all monitored voltages, is compared against a user programmable voltage set internally by a digital to analog converter.

When the voltage on the VBATT pin falls below the UV1 threshold the POWER_FAIL pin will be asserted and latched. The latched condition will persist as long as the voltage on the battery is below the UV1 level. Once the voltage on the battery has risen above the UV1 threshold level, one of two events may clear the latch and allow the POWER_FAIL pin to be released; first, If the voltage on the battery falls below the UV2 threshold, and second if an I^2C *POWER FAIL CLEAR* command is issued. Once one of these conditions has been met, the POWER_FAIL pin will be released after a power-fail timeout period (t_{PFTO}) of 3.0-4.5ms. The POWER_FAIL level is user programmable from 2.55-3.6V at 150 mV increments.

The second battery monitoring threshold voltage UV2 is not latched and is user programmable from 2.55-3.6V, in 150 mV increments.

Once either of the batter monitoring threshold voltages have been violated the SMB112 can be programmed to respond in one of three ways, it may perform: a power-

APPLICATIONS INFORMATION (CONTINUED)

off operation, a force-shutdown operation, or take no action. When programmed to perform a power-off or force-shutdown operation the SMB112 can optionally be programmed to latch the outputs off until the power on pin is toggled or an I^2C power-on command is issued. In addition, the HEALTHY output pin can be asserted.

LDO STANDBY VOLTAGE

The SMB112 has an internal 3.3 volt Low Dropout (LDO) linear regulator. While the battery voltage is above the POWER_FAIL level this supply is powered from the LDO_SUPPLY pin, however, when the battery voltage drops below the POWER_FAIL level the LDO supply voltage will be routed to the battery through an internal analog multiplexer. The LDO will continue to be supplied by the battery until the latched POWER_FAIL pin is released. The LDO will be disabled once the Battery voltage falls below the second battery monitoring threshold UV1.

SOFT START

The SMB112 provides a programmable soft-start function for all PWM outputs. The soft-start control limits the slew rate that each output is allowed to ramp up without the need for an external capacitor. The soft start slew rate is proportional to the product of the output voltage and a slew rate reference; see Figure 6. This global reference is programmable and may be set to 400,200,100,67,50,33,25, and 20 volts per second. The slew rate control can also be disabled on any channel not requiring the feature.

OUTPUT VOLTAGE

The PWM output voltages are set by a resistor voltage divider from the output to the COMP1 node; see Figure 6. For the buck channel (channel 3), the voltage divider is internal to the part and programmable. The resistor divide may be set by adjusting a 100 kΩ resistor string with 8 taps from R1 = 20-90 kΩ. For the boost outputs (channels 1 and 2), the resistor divide is external and any appropriate value of R1 an R2 can be chosen. The reference voltage that sets the output is user programmable, and may be set anywhere from 0-1.0V in 4 mV increments for channels 1 to 3, channel 0 is fixed at 1.0V. The channel 0 inverting output is set by the external resistor divider and the VREF_OUT voltage, which varies from 1.0 – 2.0V in 8 mV increments.

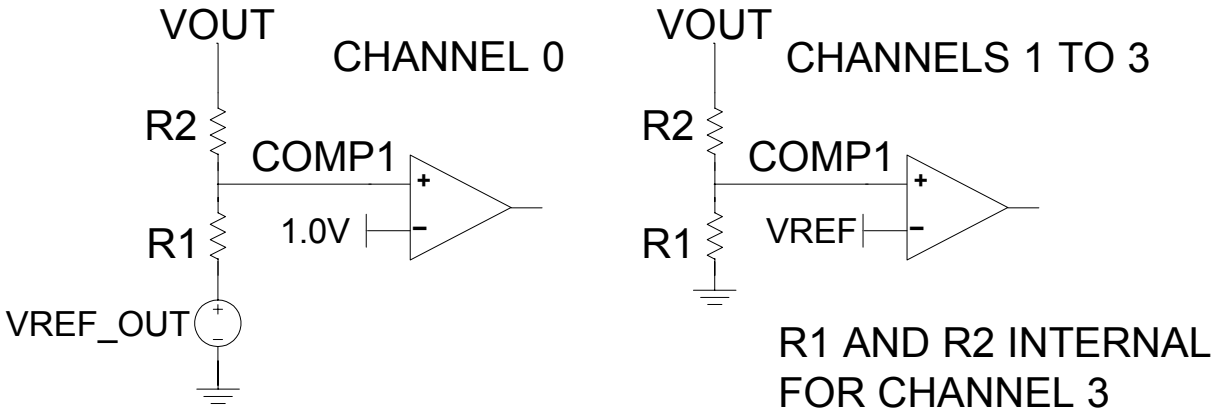


Figure 7: The output voltage is set by the gain of the non-inverting op-amp. The resistor divider is internal for all buck channels. VREF is Programmable from 0 to 1.0 volt in 4 mV increments and VREF_OUT is programmable from 1.0 to 2.0V in 8 mV increments. All voltage references are programmable via the I^2C interface.

APPLICATIONS INFORMATION (CONTINUED)

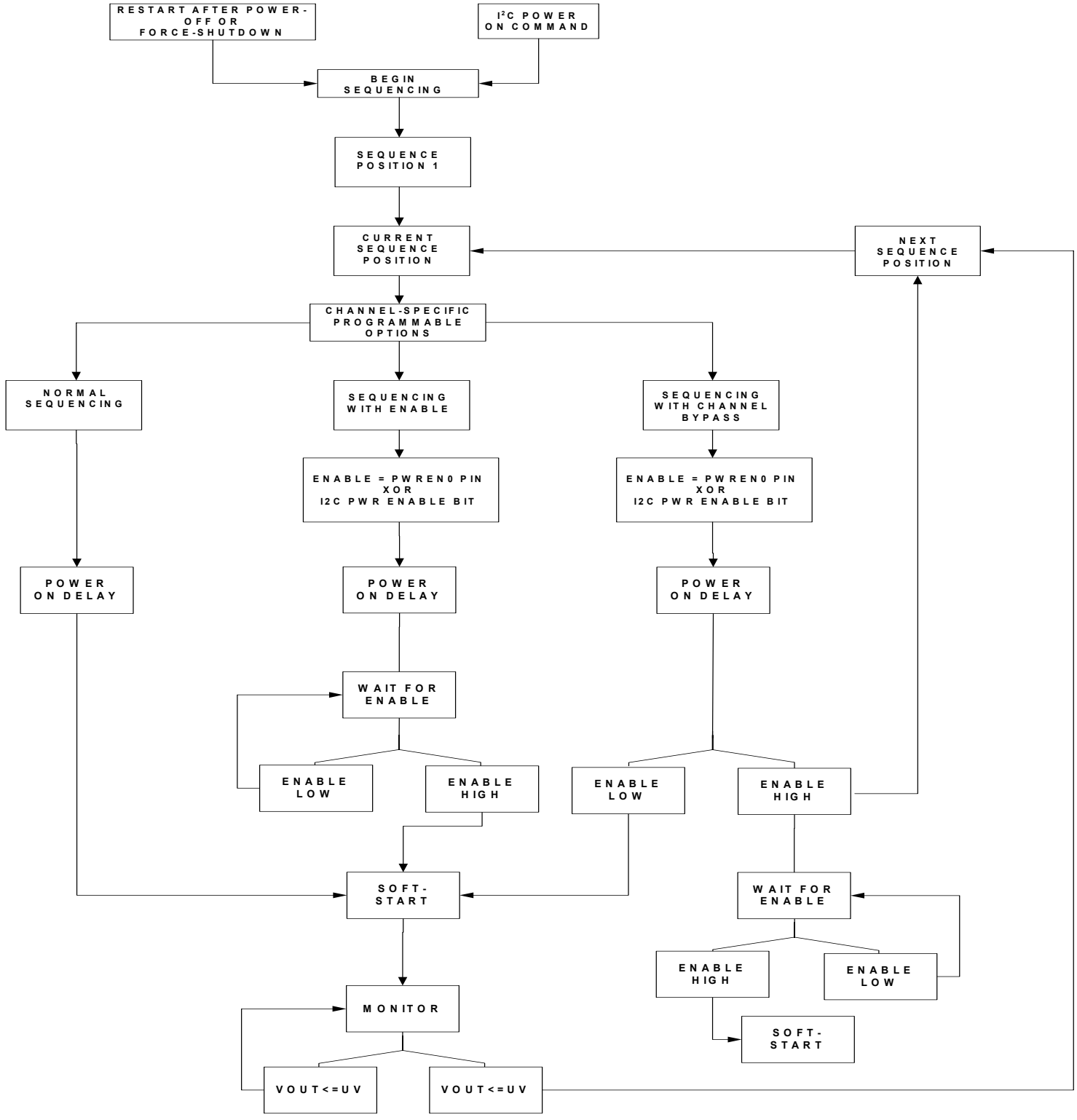


Figure 8 – Power-on sequencing flow chart: There are three automated power-on sequencing modes, and a manual mode.

APPLICATIONS INFORMATION (CONTINUED)

MINIMUM LOAD

The duty cycle is limited to a 10-90% range. Consequently, the boost channels require a minimum load to prevent over voltage conditions from occurring.

This may be overcome by attaching a resistor preload to the output that matches the minimum load requirements. This approach will result in a constant current consumption while the outputs are enabled. Alternatively, a zener diode (with a higher breakdown voltage than the output) can be connected across the output clamping the output voltage. This approach will not draw current when the load is enabled on the output.

MARGINING

The SMB112 has two additional voltage settings, margin high and margin low. The margin high and margin low voltage settings have the same voltage range as the controllers' nominal output voltage. These settings are stored in the configuration registers and are loaded into the voltage setting by margin commands issued via the I^2C bus.

The margin command registers contain two bits for each channel that decode the commands to margin high, margin low, or control to the nominal setting. Therefore, any combination of margin high, margin low, and nominal control is allowed in the margining mode.

Once the SMB112 receives the command to margin the supply voltages, it begins adjusting the supply voltages to move toward the desired setting. When all channels are at their voltage setting, a bit is set in the margin status registers.

Note: Configuration writes or reads of registers should not be performed while margining.

A typical application utilizing the margining functionality is depicted in Figure 9. When used with a boost controller setup as a constant current white LED driver, margining can be used to adjust the current through the LED chain as an adjustable brightness control.

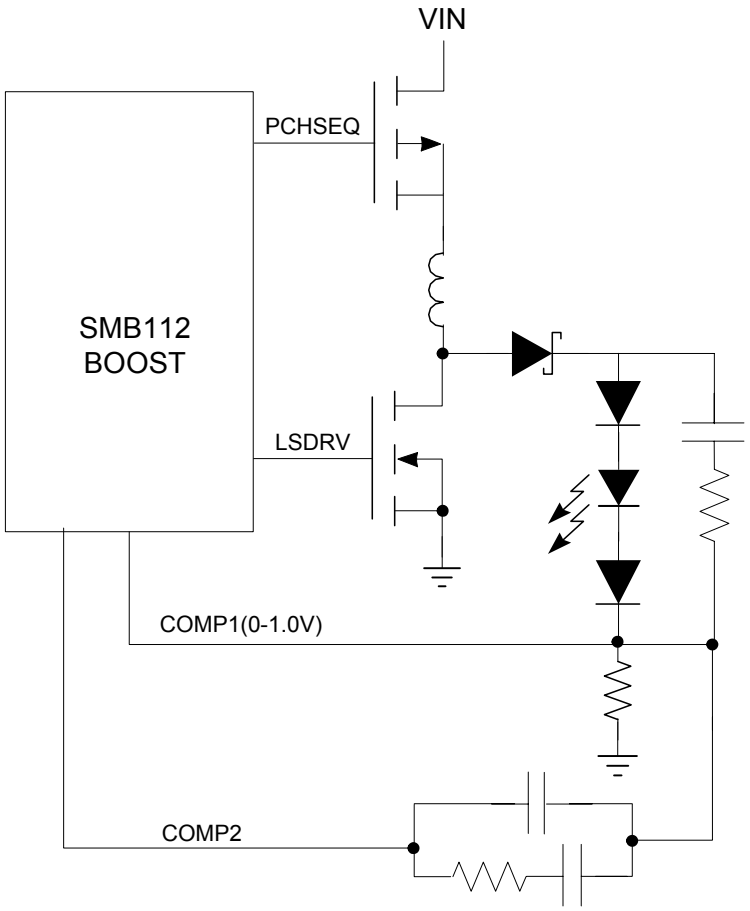


Figure 9 – Boost configured as a constant current LED driver with adjustable current capabilities.

APPLICATIONS INFORMATION (CONTINUED)

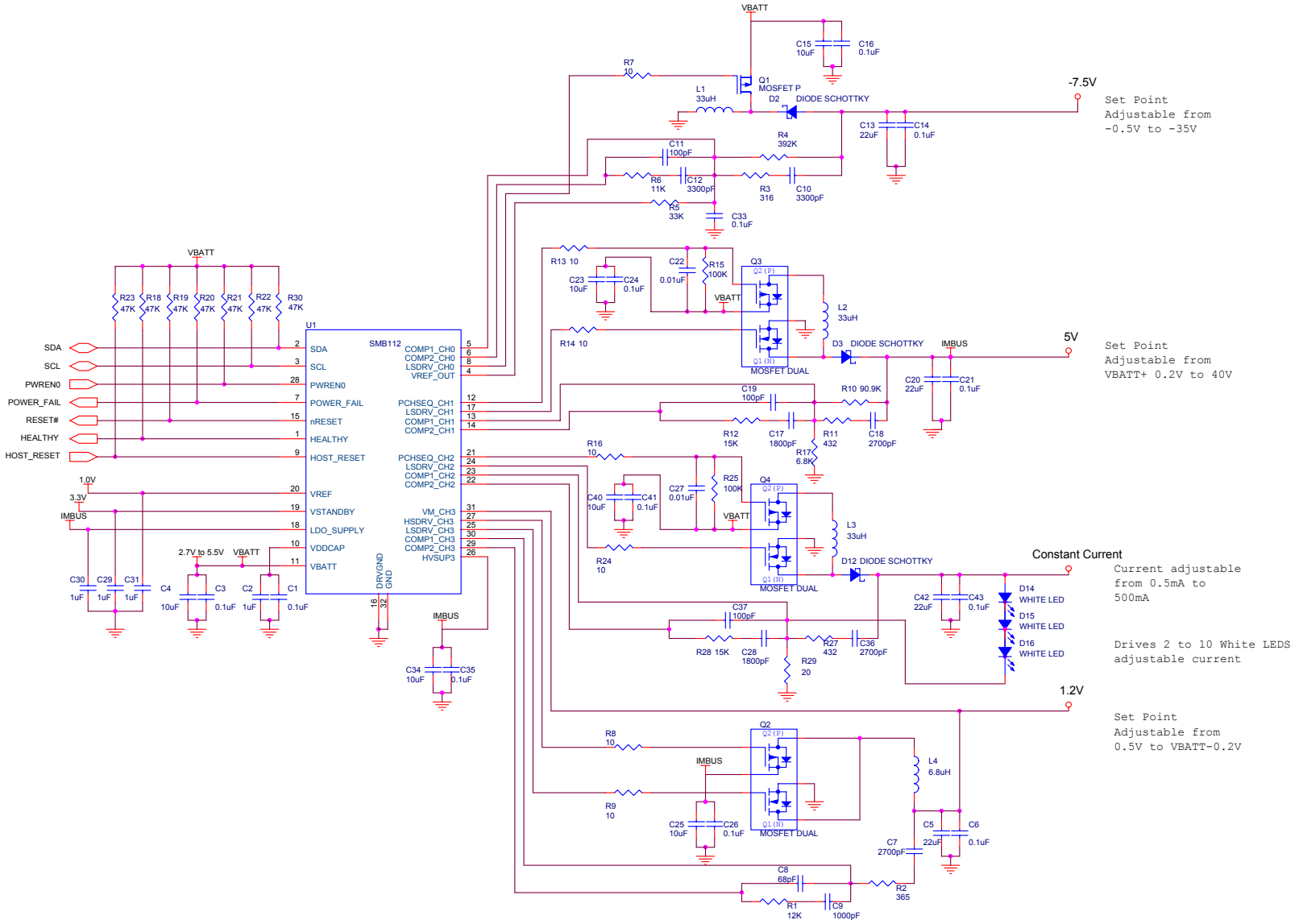


Figure 10 – Applications schematic.

APPLICATIONS INFORMATION (CONTINUED)

Item	Description-	Vendor / Part Number	Qty	Ref. Des.
Resistors				
1	12.1KΩ, 1/16W, 1%, 0402, SMD	Any	1	R1
2	365Ω, 1/16W, 1%, 0402, SMD	Any	1	R2
3	3.6Ω 1/16W, 1%, 0402, SMD	Any	1	R3
4	392KΩ, 1/16W, 1%, 0402, SMD	Any	1	R4
5	33KΩ, 1/16W, 5%, 0402, SMD	Any	1	R5
6	11KΩ, 1/16W, 5%, 0402, SMD	Any	1	R6
7	10Ω, 1/16W, 1%, 0402, SMD	Any	7	R7, R8, R9, R13, R14, R16, R24
8	90.9KΩ, 1/16W, 1%, 0402, SMD	Any	1	R10
9	432Ω, 1/16W, 1%, 0402, SMD	Any	2	R11, R27
10	15KΩ, 1/16W, 5%, 0402, SMD	Any	2	R12, R28
11	100KΩ, 1/16W, 5%, 0402, SMD	Any	2	R15, R25
12	6.81KΩ, 1/16W, 1%, 0402, SMD	Any	1	R17
13	47KΩ, 1/16W, 5%, 0402, SMD	Any	7	R18, R19, R20, R21, R22, R23, R30
14	10Ω, 1/16W, 1%, 0402, SMD	Any	1	R29
Capacitors				
15	0.1uF, 16V, ceramic, X7R, 0402, SMD	Any	6	C1, C3, C6, C14, C16, C21, C24, C26, C33, C35, C41, C43
16	1uF, 50V, ceramic, X7R, 0805, SMD	Any	4	C2, C29, C30, C31
17	10uF, 6.3V, ceramic, X5R, 0805, SMD	Any	3	C4, C15, C23, C25, C34, C40
18	22uF, 6.3V, ceramic, Y5V, 1210, SMD	Any	7	C5, C13, C20, C42
19	2700pF, 50V, ceramic, X7R, 0402, SMD	Any	2	C7, C18, C36
20	68pF , 50V, ceramic, X7R, 0402, SMD	Any	3	C8
21	1000pF, 50V, ceramic, X7R, 0402, SMD	Any	4	C9
22	3300pF, 50V, ceramic, COG, 0402, SMD	Any	4	C10, C12
23	100pF, 50V, ceramic, C0G, 0402, SMD	Any	4	C11, C19, C37
24	1800pF, 50V ceramic, X7R, 0402, SMD	Any	8	C17, C28
25	0.01uF, 50V, ceramic, X7R, 0402, SMD	Any	2	C22, C27
Semiconductors				
30	Diode, Schottky, 20V, 200mA SS-MI	Panasonic, MA2SD24	3	D2, D3, D12
32	MOSFET, Complementary, Fairchild Semiconductor, FDC6420C	Fairchild, FDC6420C or equivalent	6	Q2, Q3, Q4
33	MOSFET, P-channel, -20V, 0.3 Ohm, SOT-23	Fairchild NDS356P	1	Q1
35	SMB112N	Summit Microelectronics	1	U1
Magnetics				
36	Inductor, 33uH, SMD	Coilcraft DO1608C-333 or Asatech 33uH	3	L1, L2, L3
37	Inductor, 6.8uH, SMD	Sumida Corp CR436R8 or Coilcraft DO1608C-682 or Asatech 6.8uH	3	L4

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 parallel port programming system or the I²C2USB (SMX3201) USB programming system for device prototype development. The SMX3200(1) systems consist of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 and SMX3201 are available from the website (**http://www.summitmicro.com**).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application; while the SMX3201 interfaces directly to the PC's USB port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMB112 via the programming Dongle and cable. An example of the connection interface is shown in Figure 11.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

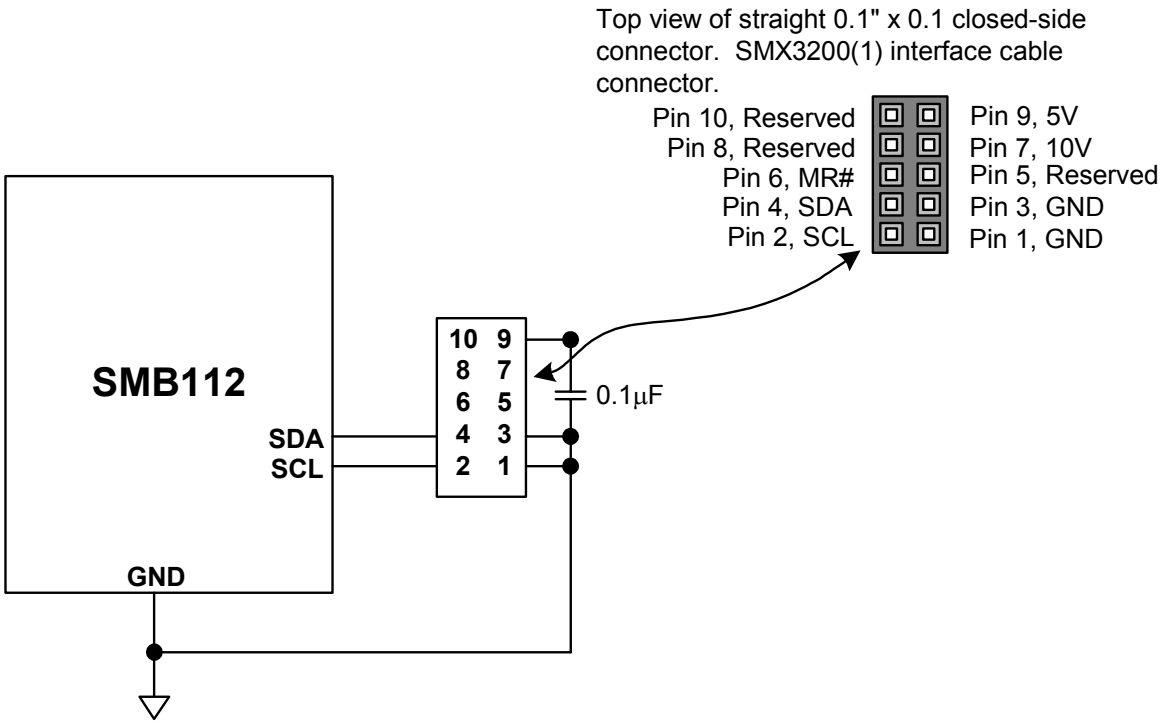


Figure 11 -- SMX3200 Programmer I²C serial bus connections to program the SMB112.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMB112.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. The slave address can be can be programmed to any seven bit number 0000000_{BIN} through 1111111_{BIN}.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 12 and 13. A Start condition followed by the slave address byte is provided by the host; the SMB112 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB112 responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page.

After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the non-volatile configuration registers and memory registers as well as the volatile command and status registers must be set before data can be read from the SMB112. This is accomplished by issuing a dummy write command, which is a write command that is not followed by a Stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figure 14 for an illustration of the read sequence.

CONFIGURATION REGISTERS

The configuration registers are grouped with the general-purpose memory.

GENERAL-PURPOSE MEMORY

The 96-byte general-purpose memory block is segmented into two continuous independently lockable blocks. The first 48-byte memory block begins at register address pointer $A0_{HEX}$ and the second memory block begins at the register address pointer $C0_{HEX}$; see Table 1. Each memory block can be locked individually by writing to a dedicated register in the configuration memory space.

I²C PROGRAMMING INFORMATION (CONTINUED)

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMB112 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (http://www.summitmicro.com). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMB112. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol. See Figure 9 and the SMX3200 Data Sheet.

Slave Address	Register Type
0000000_{BIN} to 1111111_{BIN}	Configuration Registers are located in 00_{HEX} thru $9F_{HEX}$
	General-Purpose Memory Block 0 is located in $A0_{HEX}$ thru BF_{HEX}
	General-Purpose Memory Block 1 is located in $C0_{HEX}$ thru FF_{HEX}

Table 1 - Address bytes used by the SMB112.

I²C PROGRAMMING INFORMATION (CONTINUED)

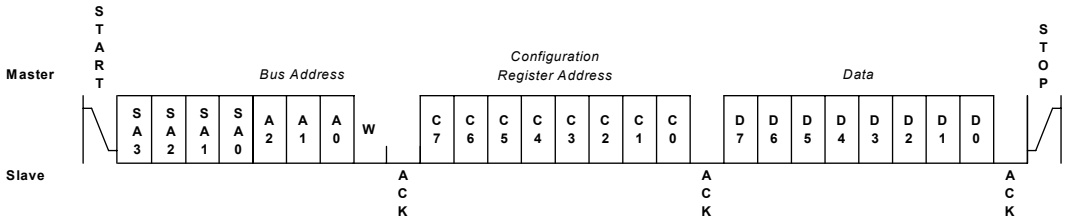


Figure 12 – Register Byte Write

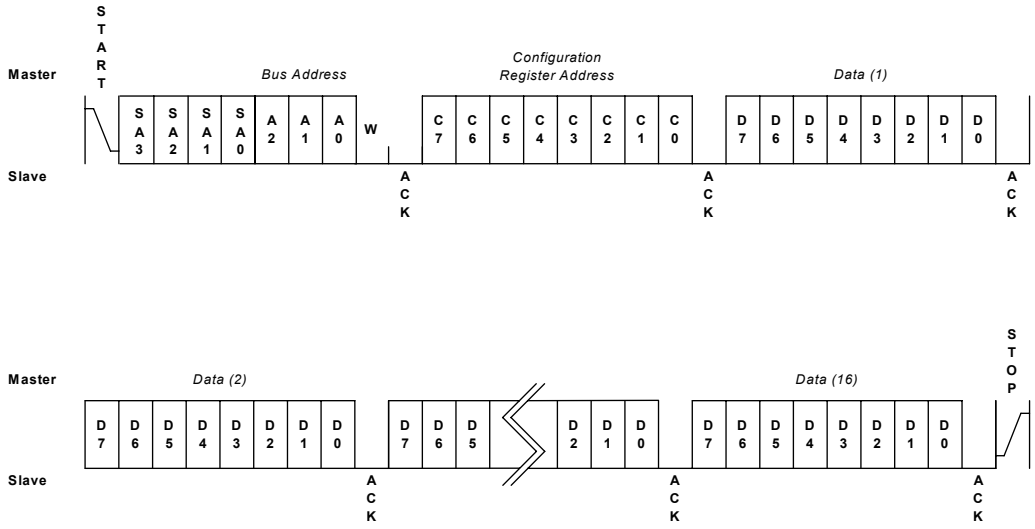


Figure 13 – Register Page Write

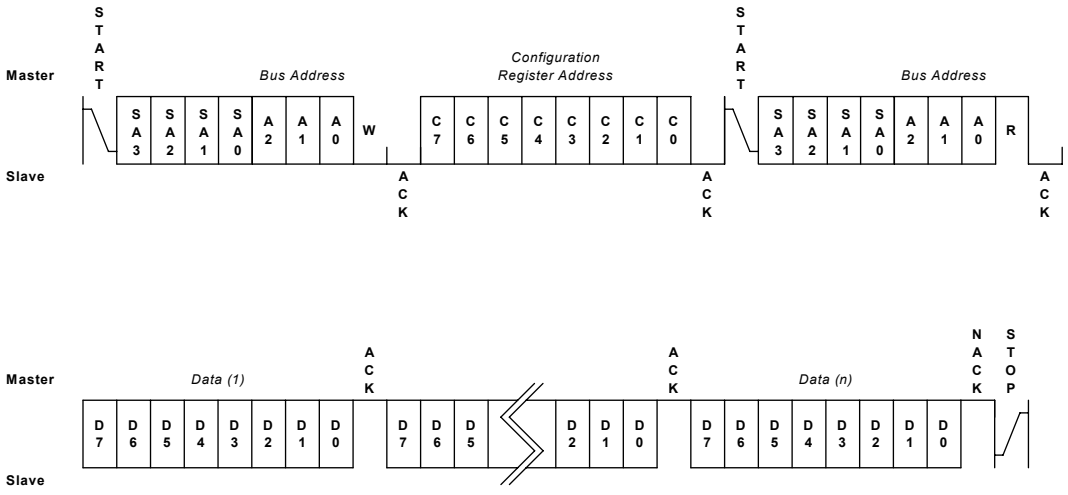
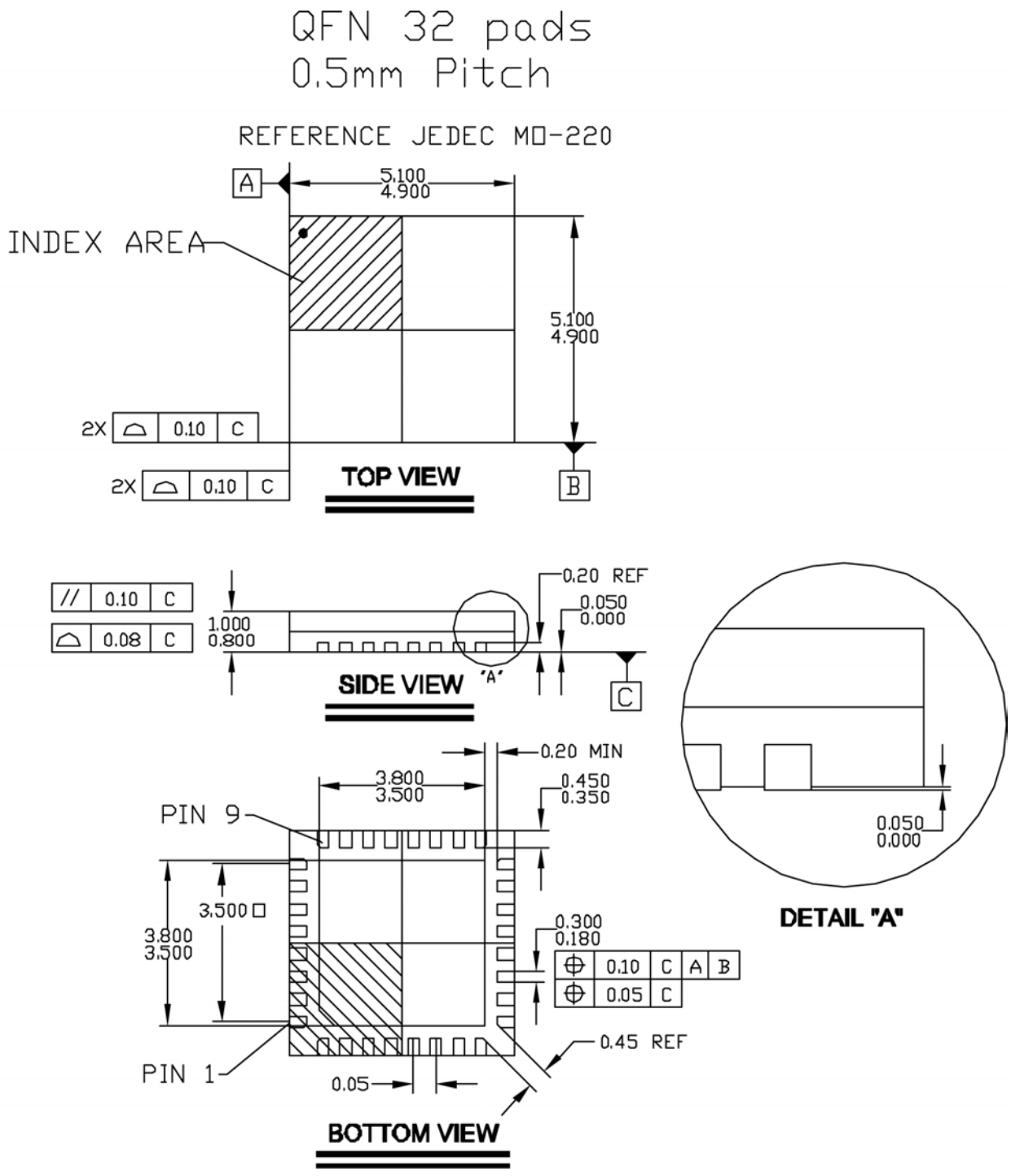


Figure 14 – Register Read

DEFAULT CONFIGURATION REGISTER SETTINGS – SMB112NC-325L					
Register	**Contents**	**Register**	**Contents**	**Register**	**Contents**
R0	D7	R15	00	R2B	00
R2	D2	R16	20	R2C	02
R3	60	R17	00	R2D	04
R4	A5	R18	02	R2E	31
R8	30	R1A	02	R2F	CF
RA	40	R1B	02	R50	C8
RB	60	R1C	02	R52	5B
RC	50	R23	30	R53	9D
R10	A6	R24	30	R54	DF
R11	56	R25	30	R58	DD
R12	04	R27	30	R5A	65
R13	54	R28	03	R5B	AD
R14	A0	R2A	00	R5C	00

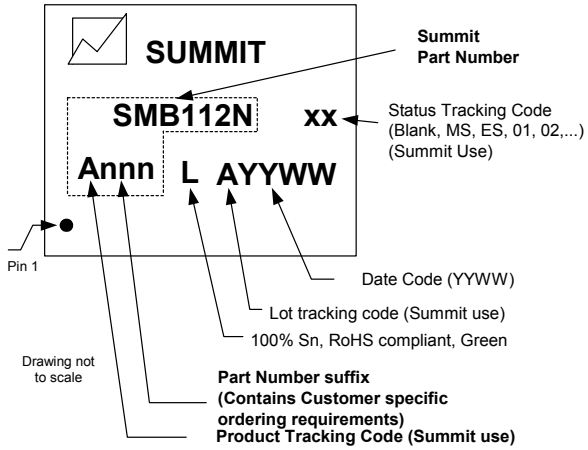
The default device ordering number is SMB112NC-325L. It is programmed with the register contents as shown above and tested over the commercial temperature range. The ordering number is derived from the customer supplied hex file. New device suffix numbers are assigned to non-default requirements.

PACKAGE



1. NOTES: ALL DIMENSIONS ARE mm [MAX] [MIN]

PART MARKING



ORDERING INFORMATION

Summit Part Number SMB112 N C nnn L

Solder Composition
L = 100% Sn, RoHS compliant, Green
Blank = 85% Sn, 15% Pb

Package
N = 32 Pad QFN

Part Number Suffix
Specific requirements are contained in the suffix

Temperature Range
C = Commercial

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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