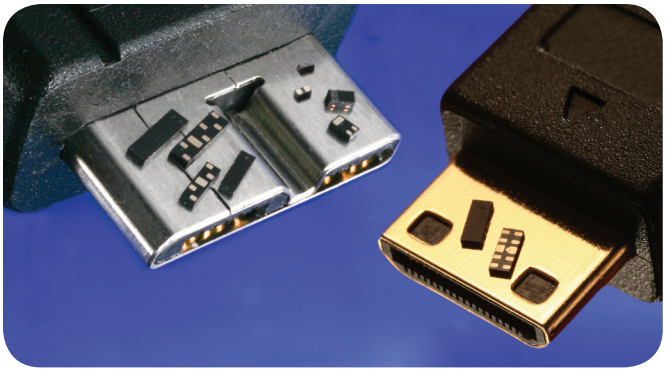
ESD Protection for USB 3.0 (SuperSpeed USB) Ports



Overview

1. Universal Serial Bus (USB) Protection History

In 1999 when it was introduced, the USB 2.0 interface's 480Mbps half-duplex differential channel presented a difficult challenge for designers implementing electrostatic discharge (ESD) protection when the range of low-capacitance, or "low-cap," Transient Voltage Suppressors (TVSs) comprised 1-1.2pF discrete diodes. The subsequent USB 3.0, or SuperSpeed USB, interface maintains the exact physical 2.0 interface, and complicates the protection problem by adding two 5Gbps half-duplex differential pairs (one Tx and one Rx pair), as shown in Figure 1.

Discrete TVS markets in the past lagged behind Moore's Law. While CPU clock speeds and memory sizes scaled internally, the external I/O interfaces of digital devices followed at a slower rate. As internal IC parallel PCI busses were upgraded to internal serial links (PCI Express), external I/O consolidated down into high-speed differential links such as USB, FireWire, and eSATA interfaces.

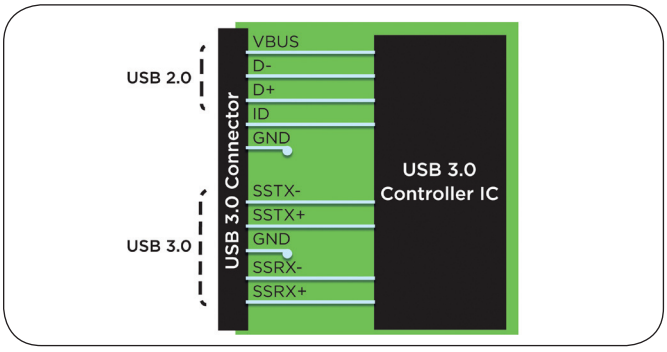


Figure 1. USB 3.0 adds two 5Gbps half differential pairs compared to USB 2.0.

Protection Technology Developments

The rapid increase in the bandwidth to the connectors created another protection challenge; the chipset's interface speeds increased and silicon feature sizes decreased. This combination of faster speed and smaller I/O cells led to increased ESD susceptibility for the chipset's PHY I/O's, while limiting the external impedance loading budget to the point where low-cap ESD was no longer low enough.

As a result, designers have transitioned from copying-and-pasting generic discrete ESD component layouts into new designs, to performing careful board characterization with respect to timing, matched impedances and insertion loss.

ESD Protection for USB 3.0

When adding ESD protection to USB 3.0 systems it is essential to consider the potential impact of additional capacitance and inductance on the timing of the chosen device on the high-speed differential pairs. When operating at 5Gbps on each of the SuperSpeed USB differential pairs, any additional impedance on the line can distort the signal, leading to:

- greater difficulty in meeting the required eye diagrams for rise times and signal levels,
- additional constraints on board design,
- lower system level performance, and
- interoperability issues with different cables (quality and length).

To minimize timing impact on these high-speed lines, and to provide adequate protection to the downstream chipset, there are four, key technical considerations to be made regarding the ESD protection device:

1. Low capacitance / low insertion loss for optimal signal integrity
2. ESD device robustness and interaction with the downstream protected IC
3. A small, flow-through ESD device package
4. An optimized layout

1. Low-Capacitance / Low Insertion Loss

Any physical protection device placed on a circuit node will add parasitic electrical elements to the system. Even the routing of an ideal clamp device can create unavoidable disturbances in the PCB trace geometry, including parasitic capacitance created by the plate capacitor formed on the PCB by the solder pad, inductive discontinuities caused by fan-in/fan-out routing bends, or unavoidable vias.

Capacitance Measurements

When reviewing specifications for TVSs, some common characteristic parameters are listed primarily as a historical legacy of lab measurements, rather than as data which has been collected specifically to make the system designer's choice easier and more comprehensive. For example, input capacitance (C_{IN}) or channel capacitance (C_{CH}) are often specified at 1MHz because earlier discrete and logic devices were measured with 1MHz LCR meters. While it is not likely to find a 1MHz capacitance measurement for a 5GBps PHY I/O pin, it may be surprising to find such a measurement for a device targeted for that application.

So rather than trying to overlay a legacy capacitance value over a cutting-edge application, it is more productive to consider the impedance and insertion loss due to the device in the circuit at the frequencies and harmonics of interest (beyond hundreds of MHz and GHz for USB 3.0).

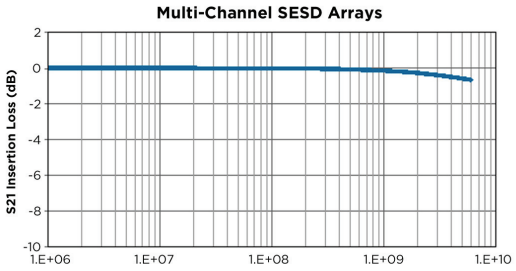
TE Circuit Protections' Silicon ESD (SESD) devices exhibit capacitance that is characterized at 3GHz, providing the designer an immediate indication of its impact in the target application. This information can also be derived from the s-parameter models of the device as part of a more complex parasitic model of diode and package capacitance and bondwire inductance. However, providing an effective capacitance measurement at the frequency of interest conveniently enables a lumped-element "sanity check" in a single, relevant number, and therefore saves design time.

Insertion Loss

For selection of a single passive component within a channel, insertion loss characterization reveals the primary relevant contributions of parasitic effects on the channel for that device.

It can be noted in Figure 2 that the insertion loss measurement is limited to 6GHz, just short of the 7.5GHz and 12.5GHz 3rd and 5th harmonics in USB 3.0. Indeed at some point any TVS device will exhibit a self-resonance where the primary channel capacitance and the bondwire inductance will nullify the insertion loss. After this point the bondwire inductance will tend to isolate the parasitic capacitance from loading the channel. However, while Figure 2 describes performance, other factors such as interconnects and losses in higher dielectric PCB materials, may tend to overwhelm the attenuation contributions of the TVS device. (These effects can be further isolated with TDR analysis and other techniques.)

For a first-pass evaluation of a TVS device, an insertion loss plot showing <-0.5dB at 2.5 GHz is a precise indicator of suitability for use in a USB 3.0 system. TE Circuit Protection's low capacitance SESD Arrays have an low insertion loss of -0.29dB at 2.5GHz which provide more than ample margin for the overall system. The discerning designer will pursue this further with more details on differential insertion loss, crosstalk, and other metrics specific to the particular implementation environment.



Application	Bit Rate (Gbps)	@Frequency (GHz)	Insertion Loss (dB)
HDMI 1.4 (1080p)	2.25	1.13	-0.15
Display Port	2.70	1.35	-0.20
HDMI 1.4 (max spec)*	3.40	1.70	-0.23
USB 3.0	5.00	2.50	-029
eSATA	6.00	3.00	-0.35
Thunderbolt	10.00	5.00	-0.50

* Devices are HDMI 4K / QuadHD resolutions (4096 x 2160) ready

Figure 2. Single-ended insertion loss of a typical SESD device.

ESD Robustness and Interaction with the Downstream IC

System level robustness: TVS interaction with ASIC protection

In general, an overall system is only as robust as its weakest elements. On each node the current sharing of each device will naturally select the least robust component for first failure during an ESD strike. In the most simplified example of modeling destructive behavior (Figure 3), a TVS device and the I/O structure of the protected ASIC (Application-Specific Integrated Circuit) are modeled as simple diode clamps connected with the lumped element or transmission line of a PCB trace.

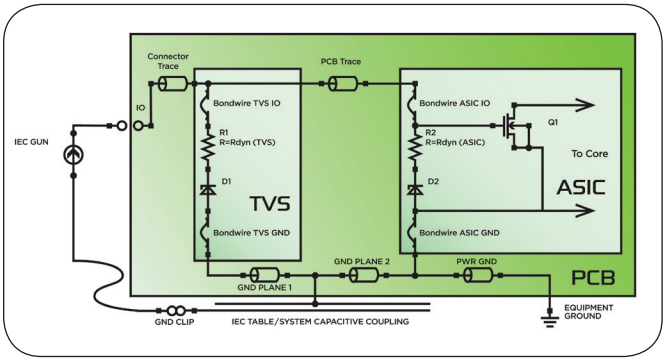


Figure 3. Simplified ESD PCB high-current discharge paths (IEC bleed resistors omitted for clarity).

The protection objective of external TVS clamps, such as SESD devices, is to divert sufficient current from the ESD pulse applied to the system through the TVS clamp (I_{TVS}) such that the residual current (I_{ASIC}) and clamped voltage levels can be tolerated by the ASIC without damage ("hard-failure") and, if possible, without a system upset or "soft-failure."

Protection circuits fabricated in deep submicron ASIC technology are inherently fast and clamp at very low voltages; but the fine geometry also limits the physical clamp dimensions and thus the total clamp power handling capability. A single TVS device die geometry may be larger than complete logical blocks in a protected ASIC, such as the PHY being protected in order to dissipate the peak power of high-voltage IEC strikes.

As always, the design engineer should validate the system interaction between the external TVS and the ASIC.

System Robustness Target

ESD robustness in the real world relies on an assumption about the margin of safety and the probabilistic distribution of strike event energy over time. If a device survives a bare minimum 10 test strikes at 8kV, this information does not offer a clear indication about its robustness. For instance, the device may not survive an 11th strike at 8kV, and it may not even survive an 11th strike at 3kV.

An attempt has been made by the industry to extend the confidence of the characterization with multi-strike capability, or qualifications of 1,000 consecutive strikes at a given robustness level to demonstrate a lifetime of repeatability.

If an ESD device shorts out due to localized filaments or subsequent EOS before the metallization fails, then the device may fail short. If the device fails after a short damages an interconnect in the device, then the result may be open.

If the device fails short, then the ASIC is protected from further strikes, but the system port functionality may be disabled. If the device fails open, the next strike will most certainly damage the ASIC I/O and may permanently damage larger parts of the ASIC. In the case of a core logic chip with integrated USB 3.0 ports, this may mean an entire PC system is rendered inoperable.

So the actual pulse intensities expected with respect to those recreated by a standard IEC61000-4-2 simulator should be considered as a probabilistic distribution rather than a clear cutoff point. Therefore, some extended characterization of the "outliers" that the device can withstand will help establish an idea of the perimeter of this distribution and the likely margin of robustness. A device with demonstrated multi-strike performance at 8kV as well as 50 pulses at 10kV could very well be more robust than a device rated for 10 pulses at 10kV.

TE Circuit Protection's SESD devices are specified to pass 1000 strikes at 8kV, 100 strikes at 10kV, and 1 strike at 20kV. Per IEC6100-4-2 standard

3. A Small, Flow-Through ESD Device Package

Packaging development has also been a key design factor in ESD protection. SOT-23 and MSOP-10 plastic packages, once the mainstay of TVS components, are now considered unacceptable for low-cap applications such as USB 3.0. The traditional packages, previously thought to be compact, require PCB pad sizes that inherently contribute as much or more parasitic capacitance even before the TVS device is populated.

To meet the requirements of today's leading high-speed applications, silicon ESD devices must take into account the applications' pad sizes and PCB routing difficulties. This has driven the need for flow-through layouts.

Also, to meet the applications' timing and insertion loss requirements, today's highest-performance silicon ESD devices have reduced their package sizes in order to mitigate the parasitic effects of long inductive leadframes and bondwires, as well as to save board space. In addition, today's newest silicon ESD devices, such as TE Circuit Protection's SESD devices, offer the industry's smallest and shortest-height, flow-through packages (Figures 4 and 5). They also offer reduced package height to minimize bondwire length and parasitic impedance. Moreover, the reduced-height devices are well-suited for today's ultra-slim mobile/portable applications.

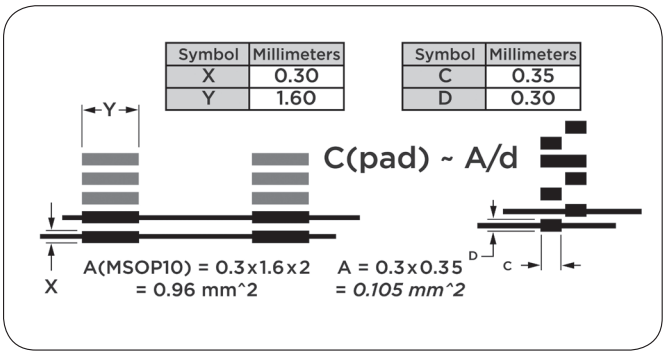


Figure 4. SESD packages provide 2/3 reduction in pad area and capacitance.

4. Optimizing Layout

Designers of USB-enabled devices face a common challenge: reducing time-to-market. When designing for high-frequency applications, reference layouts play a key role in minimizing design risk, engineering cost, and re-engineering time. Adding ESD protection to USB 3.0 is no exception.

TE Circuit Protection's portfolio of industry-leading devices offers designers a variety of options for adding ESD protection to USB 3.0 applications. Figure 6 through Figure 8 illustrate ESD protection layouts for USB 3.0 designs. TE Circuit Protection's polymeric positive thermal coefficient (PPTC) overcurrent devices are shown in the layouts, and are intended for USB 3.0 downstream port applications.

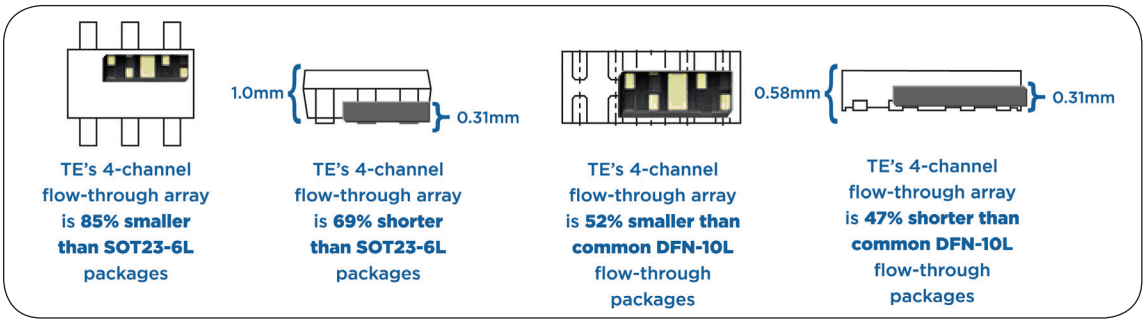


Figure 5. SESD package benefits for single- and multi-channel devices.

Figure 6 shows a 6-channel array (SESD1103Q6UG-0020-090) protecting the six signal lines routed from a Standard-A USB 3.0 connector. Figure 7 shows a 6-channel array (SESD1103Q6UG-0020-090) protecting the six signal lines routed from a USB 3.0 Micro-B connector. And Figure 8 shows two 4-channel miniature arrays (SESD0802Q4UG-0020-090) protecting all eight signal and ID / VBUS lines routed from a USB 3.0 Micro-B connector. (Note the straight-through, flow-through layout for the SuperSpeed USB lines operating at 5Gbps, minimizing reflections and signal distortions.)

As always, the designer should always verify the layout in-system for TDR impedance and crosstalk. Even when channel compliance is validated with other required compliance test methods, confirming that passive discontinuities are minimized with TDR is always beneficial.

Summary

When designing SuperSpeed USB systems, adding ESD protection need not be a complex and confusing task. TE Circuit Protection's new SESD devices offer industry-leading low-capacitance, highest ESD kV rating for low-cap devices as well as the smallest size flow-through arrays. For USB 3.0, a effective solution can be to use a single 6-channel array when protecting only six high-speed lines. If the system requirement is to protect all eight lines (including VBUS and ID), designers can employ two 4-channel miniature arrays. Of course, all individual circuits should be tested by the user.

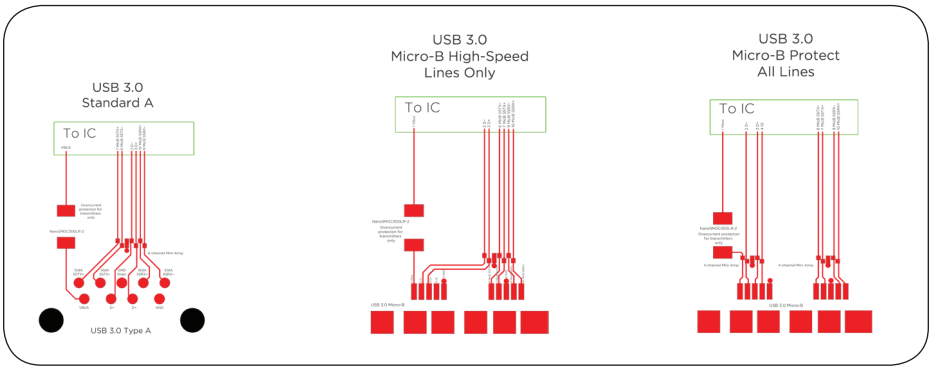


Figure 6. One 6-channel SESD protects USB 3.0.

Figure 7. One 6-channel SESD protects USB 3.0 Micro-B.

Figure 8. Two 4-channel SESD arrays protect Micro-USB3.0.

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