H5MS5122EFR

The SK Hynix H5MS5122EFR Series is 536,870,912-bit CMOS Low Power Double Data Rate Synchronous DRAM (Mobile DDR SDRAM), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 4,194,304 x32.

The SK Hynix H5MS5122EFR series uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins.

The SK Hynix H5MS5122EFR Series offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (Mobile DDR SDRAM operates from a differential clock: the crossing of CK going HIGH and CK going LOW is referred to as the positive edge of CK), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the Low Power DDR SDRAM (Mobile DDR SDRAM) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits

registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Low Power DDR SDRAM (Mobile DDR SDRAM) provides for programmable read or write bursts of 2, 4 or 8 locations.

An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multibank architecture of Low Power DDR SDRAM (Mobile DDR SDRAM) allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

The Low Power DDR SDRAM (Mobile DDR SDRAM) also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half, quarter and 1/8 and 1/16 array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule).

Only Read bursts in progress with auto precharge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Autoprecharge enabled and for Write bursts.

The SK Hynix H5MS5122EFR series has the special Low Power function of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

Deep Power Down Mode is an additional operating mode for Low Power DDR SDRAM (Mobile DDR SDRAM). This mode can achieve maximum power reduction by removing power to the memory array within Low Power DDR SDRAM (Mobile DDR SDRAM). By using this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up mother-board power-line layout flexibility.

All inputs are LVCMOS compatible. Devices will have a VDD and VDDQ supply of 1.8V (nominal).

Features

- Mobile DDR SDRAM
  - Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
  - x32 bus width
  - Multiplexed Address (Row and Column address)
- SUPPLY VOLTAGE
  - 1.8V device: VDD and VDDQ = 1.7V to 1.95V
- MEMORY CELL ARRAY
  - 512Mbit (x32 device) = 4M x 4Bank x 32 I/O
- DATA STROBE
  - x32 device: DQS0 ~ DQS3
  - Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DQS
- LOW POWER FEATURES
  - PASR (Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
  - DPD (Deep Power Down): DPD is an optional feature, so please contact SK Hynix office for the DPD feature
- INPUT CLOCK
  - Differential clock inputs (CK, /CK)
- Data MASK
  - DM0 ~ DM3: Input mask signals for write data
  - DM masks write data-in at the both rising and falling edges of the data strobe
- MODE RERISTER SET, EXTENDED MODE REGISTER SET and STATUS REGISTER READ
- CAS LATENCY
  - Programmable CAS latency 2 or 3 supported
- BURST LENGTH
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- AUTO PRECHARGE
  - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE
- CLOCK STOP MODE
  - Clock stop mode is a feature supported by Mobile DDR SDRAM.
  - Keep to the JEDEC Standard regulation
- INITIALIZING THE MOBILE DDR SDRAM
  - Occurring at device power up or interruption of device power
- PACKAGE
  - 90 Ball, Lead & Halogen Free FBGA
- Operating Temperature
  - Mobile Temp.: -30oC ~ 85oC
- This product is in compliance with the directive pertaining of RoHS.