Panasonic

NN30196A

VIN = 4.5 V to 5.6 V, 9 A
Synchronous DC-DC Step down Regulator
comprising of Controller IC and Power MOSFET

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Two 9 mΩ (Typ.) MOSFETs for High Efficiency at 9 A
- SKIP (discontinuous) Mode for Light Load Efficiency
- Up to 9 A Output Current
- Input VoltageRange : AVIN : 4.5 V to 5.6 V
  PVIN : 3.1 V to 5.6 V
  Output Voltage Range : 0.6 V to 3.5 V
  Selectable Switching Frequency 500 kHz , 1 MHz , 2 MHz
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Open Drain Power Good Indication for Output Over , Under Voltage
- Built-in Under Voltage Lockout (UVLO),
  Thermal Shut Down (TSD),
  Over Voltage Detection (OVD),
  Under Voltage Detection (UVD),
  Over Current Protection (OCP),
  Short Circuit Protection (SCP)
- HQFN040-A3-0606 (Size:6 mmX6 mm,0.5mm pitch)
  40pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)

DESCRIPTION

NN30196A is a synchronous DC-DC Step down Regulator (1-ch) comprising of a Controller IC and two power MOSFETs and employs the hysteretic control system.

By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.

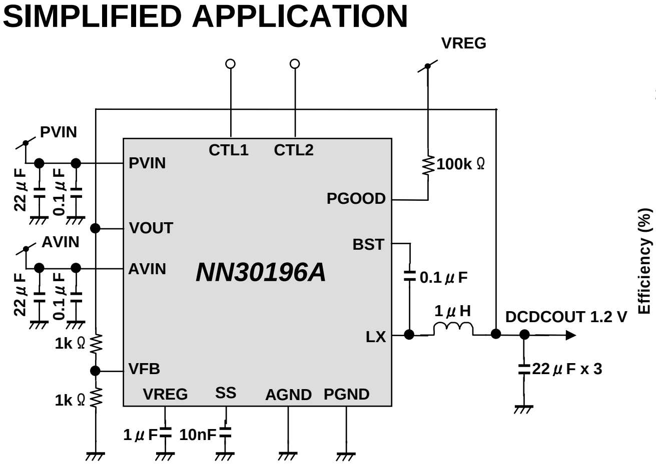
Since it is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts. Output voltage is adjustable by user.

Maximum current is 9 A.

APPLICATIONS

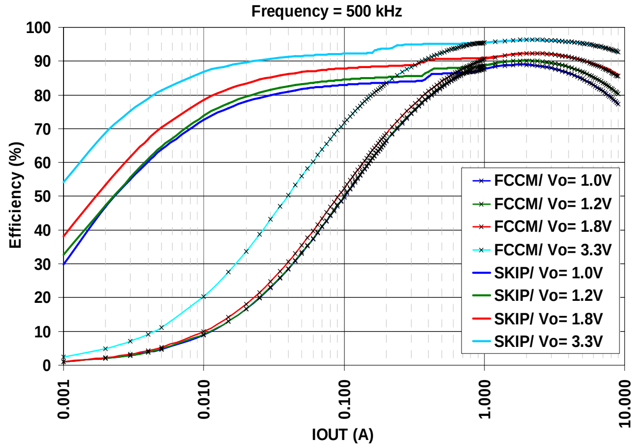
High Current Distributed Power Systems such as
- HDDs (Hard Disk Drives)
- SSDs (Solid State Drives)
- PCs
- Game consoles
- Servers
- Security Cameras
- Network TVs
- Home Appliances
- OA Equipment etc.

SIMPLIFIED APPLICATION



Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

EFFICIENCY CURVE



Condition)

V_{IN} = 5 V, Vout = 1.0 V , 1.2 V , 1.8 V , 3.3 V

Lo = 1 μH, Co = 66 μF (22 μF x 3), Frequency = 500 kHz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	6.0	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	MODE,CTL1,CTL2,VFB, VOUT	-0.3 to (V_{IN} + 0.3)	V	*1, *3
Output Voltage Range	LX,PGOOD	-0.3 to (V_{IN} + 0.3)	V	*1, *3
ESD	HBM (Human Body Model)	2	kV	—

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.
This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating.
This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
V_{IN} is voltage for AVIN, PVIN.
*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.
*3:(V_{IN} + 0.3) V must not exceed 6 V.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
40 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	44.4 °C /W	2.82 W	1.46 W	*1

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1:Glass Epoxy Substrate (4 Layers) [Glass-Epoxy: 50 X 50 X 0.8 t (mm)]
Die Pad Exposed , Soldered.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	AVIN	4.5	5.0	5.6	V	—
	PVIN	2.9	5.0	5.6	V	—
Input Voltage Range	MODE	– 0.3	—	V_{IN} + 0.3	V	*1
	CTL1	– 0.3	—	V_{IN} + 0.3	V	*1
	CTL2	– 0.3	—	V_{IN} + 0.3	V	*1
Output Voltage Range	LX	– 0.3	—	V_{IN} + 0.3	V	*1
	PGOOD	– 0.3	—	V_{IN} + 0.3	V	*1

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND. AGND = PGND
Vin is voltage for AVIN, PVIN. AVIN = PVIN.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*1 : (V_{IN} + 0.3) V must not be exceeded 6 V. (VDD + 0.3) V must not be exceeded 3.6 V.

ELECRTRICAL CHARACTERISTICS

Co = 22 µF X 3, Lo= 1 µH, VOUT Setting = 1.2 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = High (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Consumption current at active	IVDDACT	CTL1 = 5 V, I_{OUT} = 0 A RFB1 = 1 kΩ RFB2 = 1 kΩ Skip mode	—	500	1000	µA	—
Consumption current at standby	IVDDSTB	CTL1 = CTL2 = 0 V	—	—	2	µA	—
Logic Pin							
CTL1 pin Low-level input voltage	VCTL1L	—	—	—	0.3	V	—
CTL1 pin High-level input voltage	VCTL1H	—	1.5	—	—	V	—
CTL1 pin leak current	ILEAKCTL1	CTL1 = 5 V	—	3.5	10.0	µA	—
CTL2 pin Low-level input voltage	VCTL2L	—	—	—	0.3	V	—
CTL2 pin High-level input voltage	VCTL2H	—	1.5	—	—	V	—
CTL2 pin leak current	ILEAKCTL2	CTL2 = 5 V	—	3.5	10.0	µA	—
MODE pin Low-level input voltage	VMODEL	—	—	—	0.3	V	—
MODE pin High-level input voltage	VMODEH	—	2.0	—	—	V	—
MODE pin leak current	ILEAKMD	MODE = 5 V	—	3.5	10.0	µA	—
VREG							
VREG output voltage	VREGOUT	IVREG = – 6 mA	2.4	2.6	2.8	V	—
VREG drop out voltage	VREGDO	IVREG = 0 A to – 6 mA	—	15	50	mV	—

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 3, Lo= 1 µH, VOUT Setting = 1.2 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = High (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

	Parameter	Symbol	Condition	Limits			Unit	Note
				Min	Typ	Max		
VFB								
	VFB comparator threshold	V_{FBTS}	—	0.594	0.600	0.606	V	—
Under Voltage Lock Out								
	AVIN UVLO start voltage 2	$V_{UVLODET2}$	AV_{IN} = 5 V to 0 V	3.25	3.40	3.55	V	—
	AVIN UVLO recover voltage 2	$V_{UVLORMV2}$	AV_{IN} = 0 V to 5 V	3.65	3.90	4.15	V	—
	PVIN UVLO start voltage 1	$V_{UVLODET1}$	PV_{IN} = 5 V to 0 V	2.45	2.60	2.75	V	—
	PVIN UVLO recover voltage 1	$V_{UVLORMV1}$	PV_{IN} = 0 V to 5 V	2.55	2.80	3.05	V	—
PGOOD								
	PGOOD Threshold 1 (VFB ratio for UVD detect)	V_{THPG1}	PGOOD : High to Low	78	85	92	%	—
	PGOOD Hysteresis 1 (VFB ratio for UVD release)	V_{HYSPG1}	PGOOD : Low to High	2	5	8	%	—
	PGOOD Threshold 2 (VFB ratio for OVD detect)	V_{THPG2}	PGOOD : High to Low	108	115	122	%	—
	PGOOD Hysteresis 2 (VFB ratio for OVD release)	V_{HYSPG2}	PGOOD : Low to High	2	5	8	%	—
	PGOOD ON resistance	RPG	CTL1 and CTL2 = 0 V	—	10	15	Ω	—

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 3, Lo= 1 µH, VOUT Setting = 1.2 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = High (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC							
DC-DC line regulation	DD_{REGIN}	PVIN = 4.5 V to 5.6 V I_{OUT} = – 100 mA	—	0.5	1.5	%/V	—
DC-DC load regulation	DD_{REGLD}	I_{OUT} = 0 A to – 9 A	—	1.5	3.5	%	*1
DC-DC efficiency 1	DD_{EFF1}	I_{OUT} = – 10 mA Skip mode	—	66	—	%	*1
DC-DC efficiency 2	DD_{EFF2}	I_{OUT} = – 9 A	—	78	—	%	*1
DC-DC output ripple voltage 1	DD_{VRPL1}	I_{OUT} = – 10 mA	—	10	—	mV [p-p]	*1
DC-DC output ripple voltage 2	DD_{VRPL2}	I_{OUT} = - 9 A	—	5	—	mV [p-p]	*1
DC-DC load transient response	DD_{DVAC}	I_{OUT} = – 100 mA ↔ – 4 A Δt = 0.5 A / µs	—	50	—	mV	*1
DC-DC High Side MOS ON resistance	DD_{RONH}	VGS = 5 V	—	9	20	mΩ	—
DC-DC Low Side MOS ON resistance	DD_{RONL}	VGS = 5 V	—	9	20	mΩ	—
MIN Input and output voltage difference	DV	DV = PVIN – VOUT	—	2.0	—	V	*1
VFB							
VFB comparator threshold 2	V_{FBTS2}	Topr = 0 °C to 60 °C	0.588	—	0.612	V	—
VFB pin leak current 1	$I_{LEAKFB1}$	VFB = 0 V	– 1	—	1	µA	—
VFB pin leak current 2	$I_{LEAKFB2}$	VFB = 3.6 V	– 1	—	1	µA	—

*1 : Typical Value checked by design.

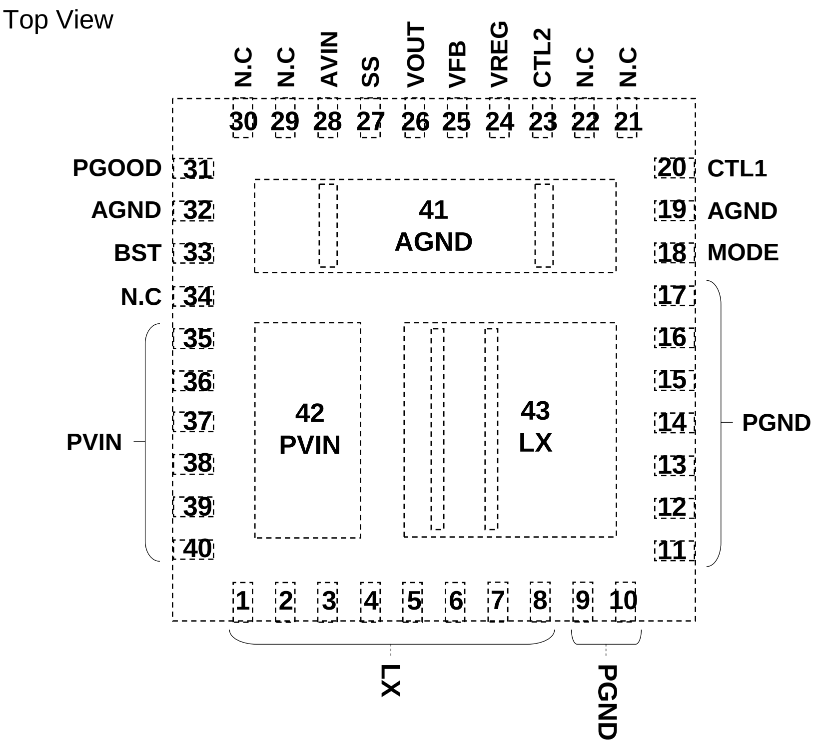
ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 3, Lo= 1 µH, VOUT Setting = 1.2 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = High (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PROTECTION							
DC-DC output current limit	DD_{ILMT}	—	—	14	—	A	*1
DC-DC Output GND Short Protection Threshold	DD_{SHPTH}	FB = 0.6 V to 0.0 V	55	70	85	%	—
Soft-Start Timing							
SS Charge Current	I_{SSCHG}	V_{SS} = 0.3 V	– 4	– 2	—	µA	—
SS Discharge Resistance (Shut-down)	R_{SSDIS}	CTL1 = CTL2 = 0 V	—	2	4	kΩ	—
Switching Frequency Adjustment							
DC-DC Switching Frequency 1	DD_{FSW1}	I_{OUT} = – 9 A CTL1 = 0 V CTL2 = 5 V	—	500	—	kHz	*1
DC-DC Switching Frequency 2	DD_{FSW2}	I_{OUT} = – 9 A CTL1 = 5 V CTL2 = 0 V	—	1000	—	kHz	*1
DC-DC Switching Frequency 3	DD_{FSW3}	I_{OUT} = – 9 A CTL1 = 5 V CTL2 = 5 V	—	2000	—	kHz	*1

*1 : Typical Value checked by design.

PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	LX	Output	Power MOSFET output pin
2			
3			
4			
5			
6			
7			
8			
9	PGND	Ground	Ground pin for Power MOSFET
10			
11			
12			
13			
14			
15			
16			
17			

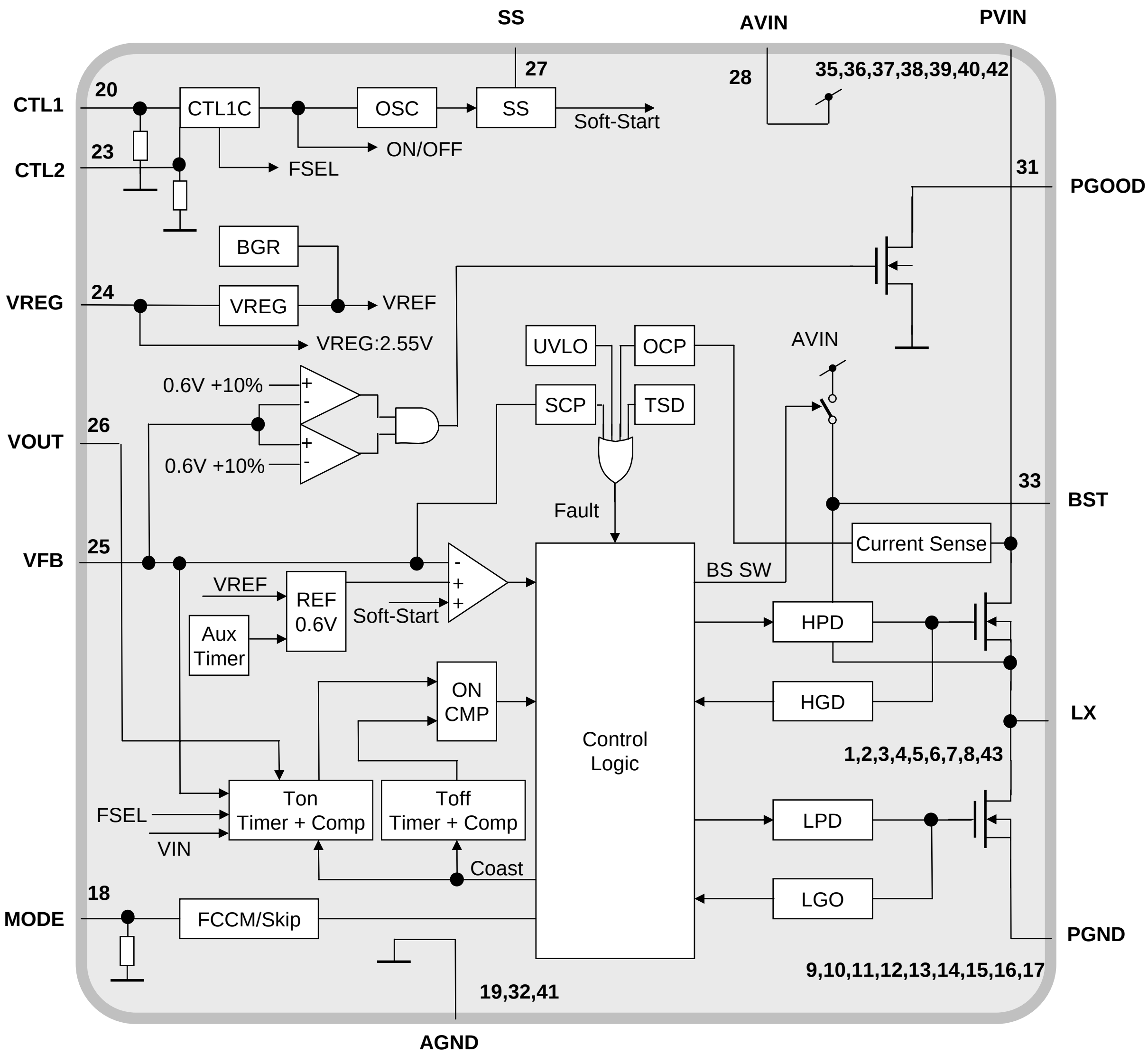
Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

PIN FUNCTIONS(Continued)

Pin No.	Pin name	Type	Description
18	MODE	Input	Skip / FCCM mode select pin
19	AGND	Ground	Ground pin
20	CTL1	Input	ON/OFF control pin 1 / Frequency selection pin
21	N.C	—	No Connection
22	N.C	—	No Connection
23	CTL2	Input	ON/OFF control pin 2 / Frequency selection pin
24	VREG	Output	LDO output pin (Power supply for internal control circuit)
25	VFB	Input	Comparator negative input pin
26	VOUT	Input	Output voltage sense pin
27	SS	Output	Soft start capacitor connect pin
28	AVIN	Power supply	Power supply pin
29	N.C	—	No Connection
30	N.C	—	No Connection
31	PGOOD	Output	Power good open drain pin
32	AGND	Ground	Ground pin
33	BST	Output	Supply input pin for high side FET gate driver
34	N.C	—	No Connection
35	PVIN	Power supply	Power supply pin for Power MOSFET
36			
37			
38			
39			
40			
41	AGND	Ground	Ground pin for radiation of heat
42	PVIN	Power supply	Power supply pin for radiation of heat
43	LX	Output	Power MOSFET output pin for radiation of heat

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

1. Protection

(1).Output Over-Current Protection (OCP) function And Short-Circuit Protection (SCP) function

1) The Over Current Protection is activated at about 14 A (Typ.) During the OCP, the output voltage continues to drop at the specified current.

2) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 70 % of the set voltage of 0.6 V.

3) The SCP operates intermittently at 2 ms-ON, 16 ms OFF intervals.

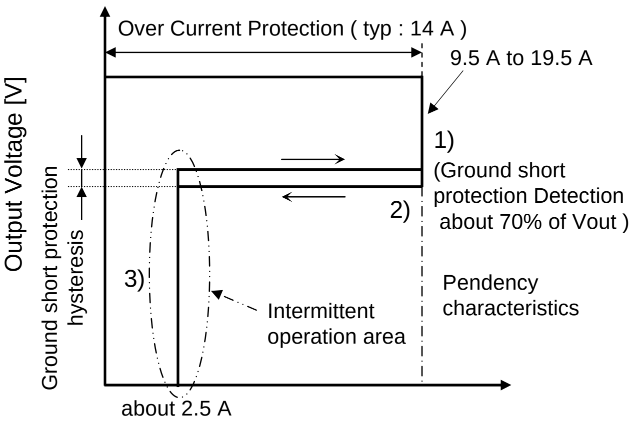


Figure : OCP and SCP Operation

(2).Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

1).The NMOS connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115 % of its set voltage (0.6 V).

2).After (1) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110 % of its set voltage (0.6 V).

3).The NMOS connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85 % of its set voltage (0.6 V).

4).After (3) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 90 % of its set voltage (0.6 V).

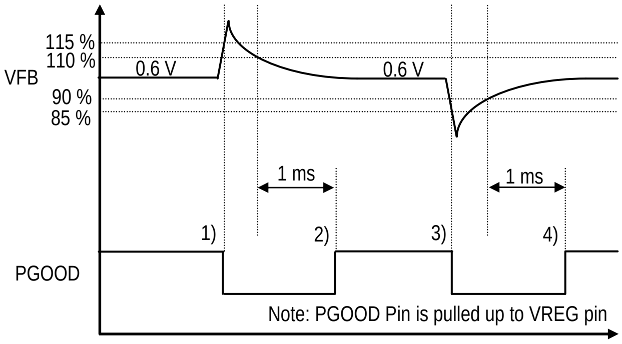


Figure : OVD and UVD Operation

(3).Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 140 °C, TSD operates and DCDC turns off.

2. Pin Setting

(1).Operating Mode Setting

The IC can operate at two different modes : Skip mode and Forced Continuous Conduction mode (FCCM).

In Skip mode, the IC is working under pulse skipping mechanism to improve efficiency at light load condition.

In FCCM mode, the IC is working at fixed frequency to avoid EMI issues.

The Operating Mode can be set by MODE pin as follows.

MODE pin	Mode
Low	Skip
High	FCCM

(2).Switching Frequency Setting

The IC can operate at three different frequency : 1000 kHz, 500 kHz and 2000 kHz.

The Switching Frequency can be set by CTL1 & CTL2 pin as follows.

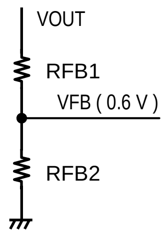
CTL1 pin	CTL2 pin	Frequency [kHz]
Low	Low	0 (DCDC OFF)
Low	High	500
High	Low	1000
High	High	2000

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

3. Output Voltage Setting

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows.
(VIN = 5V, IOUT = 0 A, FCCM, Fsw = 1 MHz)



$$VOUT = -0.0142\left(\frac{RFB1}{RFB2}\right)^2 + 0.623\left(\frac{RFB1}{RFB2}\right) + 0.593$$

Below resistors are recommended for following popular output voltage.

VOUT [V]	RFB1 [Ω]	RFB2 [Ω]
1.8	3.0 k	1.5 k
1..2	1.0 k	1.0 k
1.0	1.0 k	1.5 k

Note: RFB2 can be set to a maximum value of 10 kΩ.
A larger FBR2 value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1 %, but the actual output voltage accuracy becomes more than ± 1 % due to the influence from the circuits other than VFB comparator.
In the case of VOUT setting = 1.2 V, the actual output voltage accuracy becomes ± 1.5 %.
(VIN = 5.0 V, IOUT = 0 A, FCCM, Fsw = 1 MHz).

4. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the CTL1 or CTL2 (or both) pin becomes High, the current (2 μA) begin to charge toward the external capacitor (Css) of SS pin, and the voltage of SS pin increases straightly.

Because the voltage of FB pin is controlled by the voltage of SS pin during start up, the voltage of FB increase straightly to the regulation voltage (0.6 V) together with the voltage of SS pin and keep the regulation voltage after that. On the other hand, the voltage of SS pin increase to about 2.8 V and keep the voltage. The calculation of Soft Start Time is as follows.

$$Soft\ Start\ Time(\mathrm{sec}) = \frac{0.6}{2\mu} \times Css$$

When Css is set at 10 nF, soft-start time is approximately 3 ms.

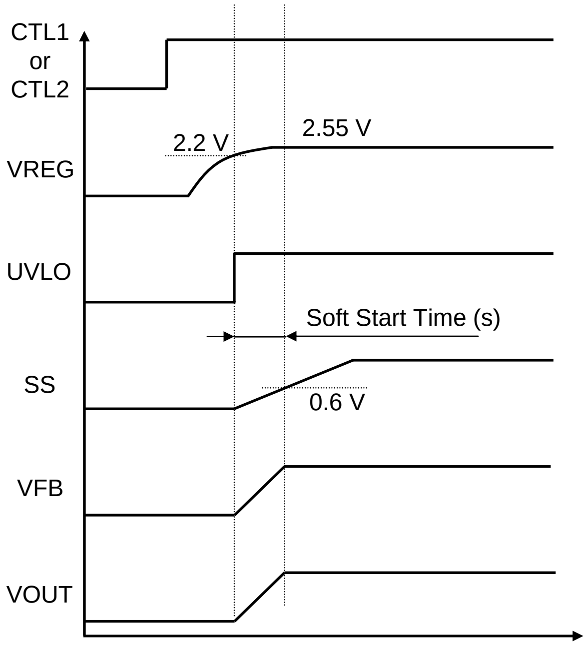


Figure : Soft Start Operation

5. Power ON / OFF sequence

(1) When the CTL1/2 pin is set to “High” after the VIN settles, UVLO is released if VIN exceeds its threshold, then the VREG starts up.
(2) When VREG voltage exceeds its threshold, the SOFT START sequence is enabled. The capacitor connected to the SS pin begins to charge and the SS pin voltage increases linearly.
(3) The VOUT pin (DCDC Output) voltage increases at the same rate as the SS pin. Normal operation begins after the VOUT pin reaches the set voltage.
(4) When the CTL1/2 pin is set to “Low”, VREG and UVLO stop operation. The VOUT pin / SS pin voltage starts to drop and the VOUT pin discharge by internal MOSFET (R = 50 Ω).

Note: The SS pin capacitor should be discharged completely before restarting the startup sequence. An incomplete discharge process might result in an overshoot of the output voltage.

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

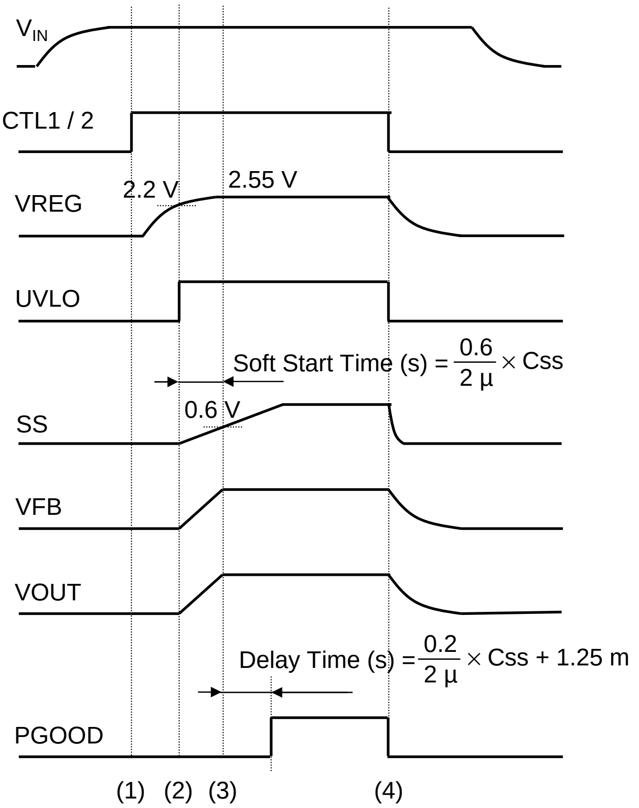
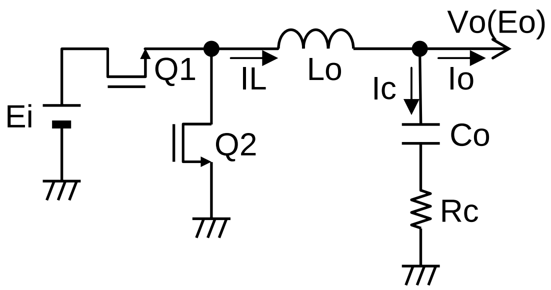


Figure : Power ON/OFF sequence



Given the desired input and output voltages, the inductor value and operating frequency determine the ripple Current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40 % of IOUT(MAX). The largest ripple current occurs at the highest VIN. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\ \mathrm{Ei} = \mathrm{Ei\_max}$$

And its maximum current rating is

$$IL\_max = \mathrm{Io\_max} + \frac{\Delta IL}{2} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

The selection of COUT is primarily determined by the ESR (Rc) required to minimize voltage ripple and load transients. The output ripple Vrpl is approximately bounded by:

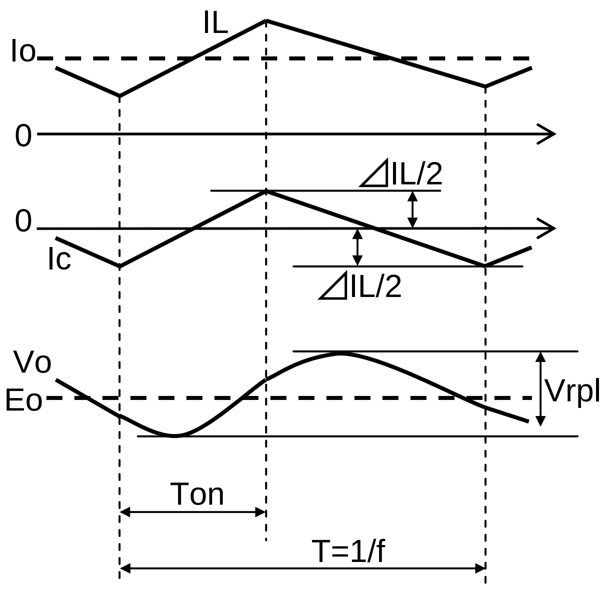
$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\mathrm{rms})\_max = \frac{\Delta IL}{2\sqrt{3}} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

6. Inductor and Output Capacitor Setting

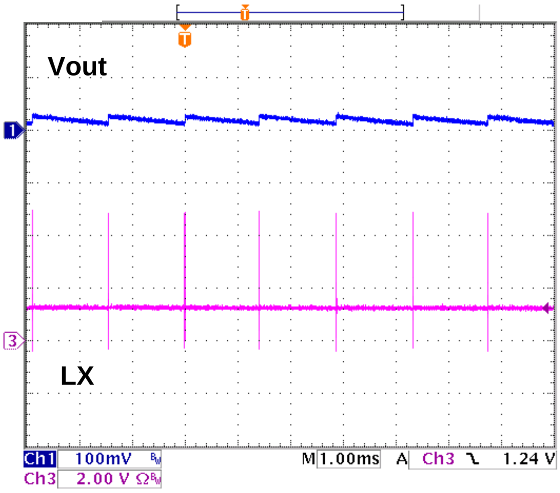


TYPICAL CHARACTERISTICS CURVES

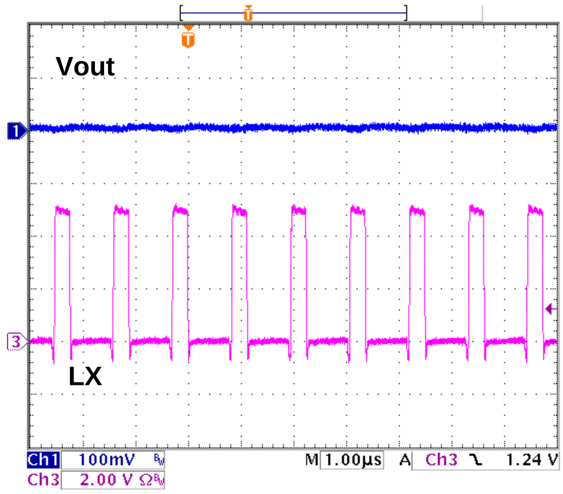
(1) Output Ripple Voltage

Condition : VIN=5V,Vout = 1.2V,Frequency = 1000kHz,Skip Mode

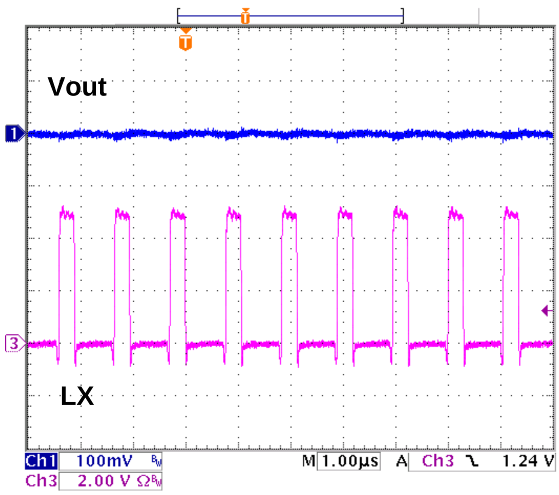
I Load = 0A



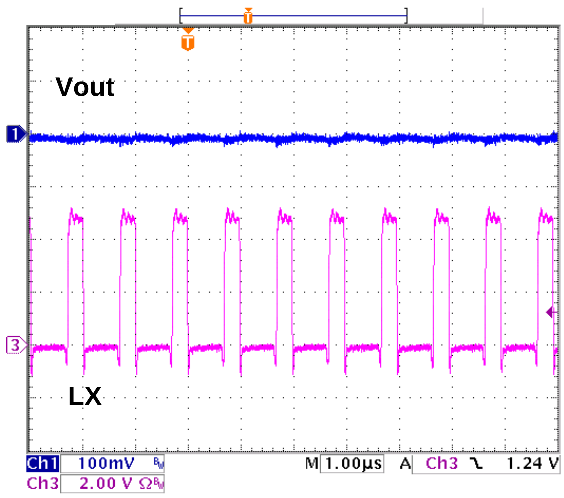
I Load = 3A



I Load = 6A



I Load = 9A

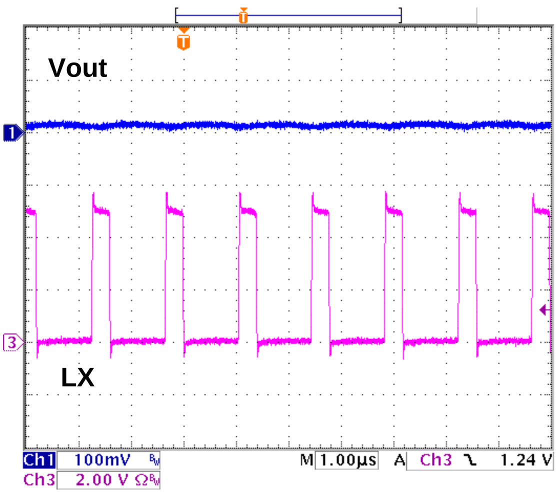


TYPICAL CHARACTERISTICS CURVES (Continued)

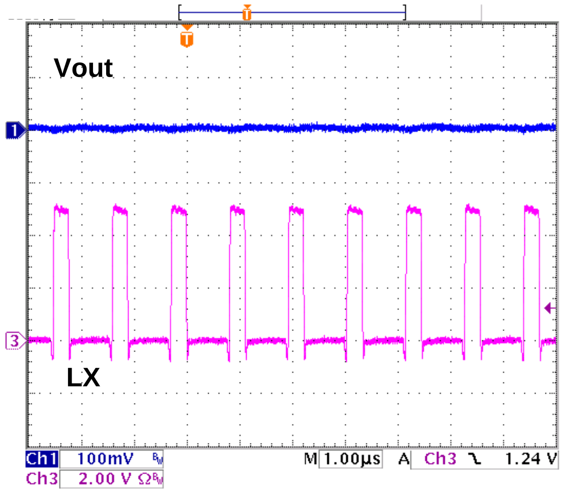
(1) Output Ripple Voltage

Condition : VIN=5V,Vout = 1.2V,Frequency = 1000kHz,FCCM Mode

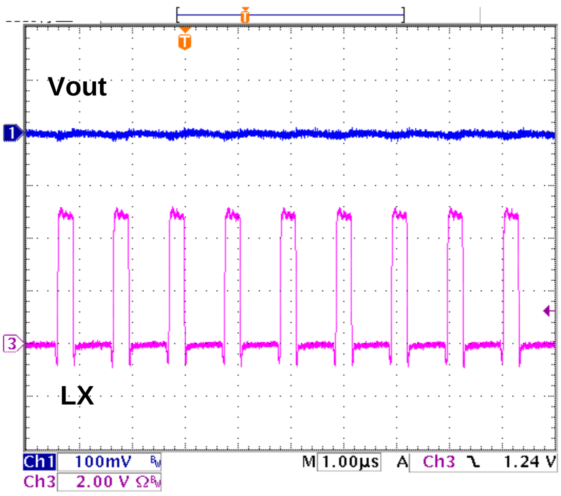
I Load = 0A



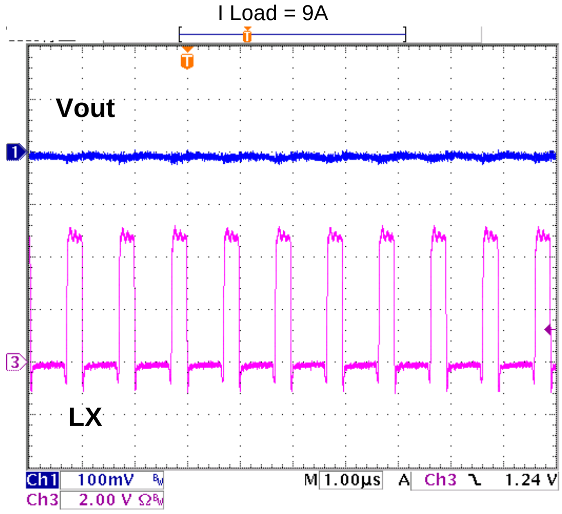
I Load = 3A



I Load = 6A



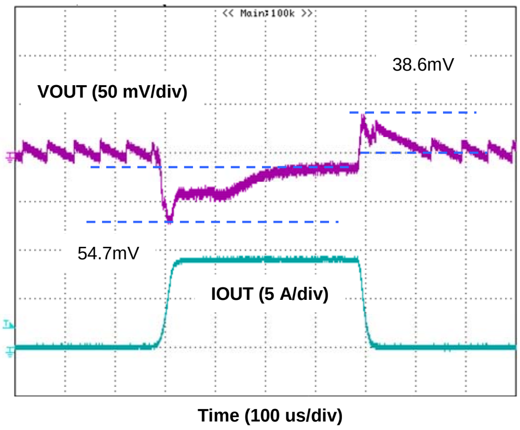
I Load = 9A

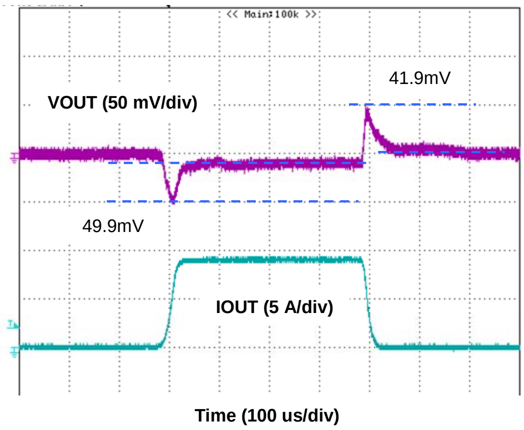


TYPICAL CHARACTERISTICS CURVES (Continued)

(2) Load transient

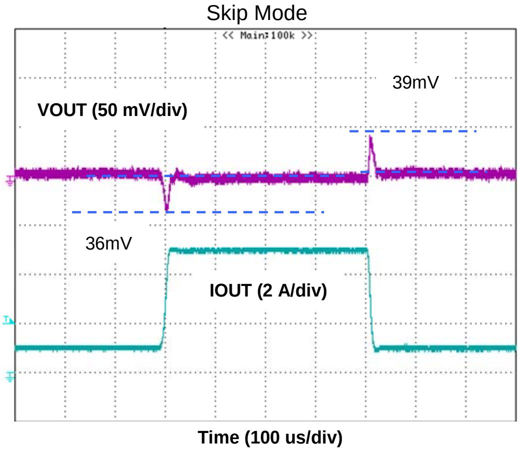
Condition : VIN = 5.0 V, Vout = 1.2 V, Frequency = 1 MHz, Iout = 10 mA ←→ 9 A (0.5 A / µs)



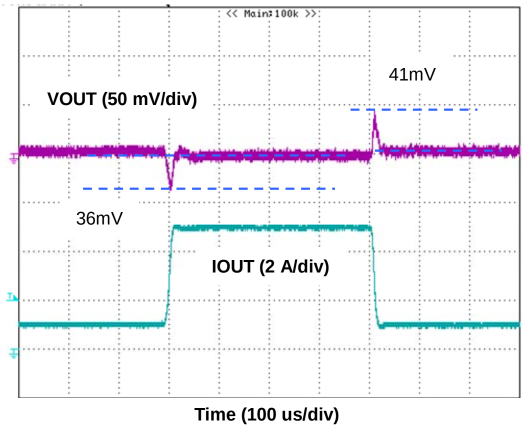


Condition : VIN = 5.0 V, Vout = 1.2 V, Frequency = 1 MHz, Iout = 1 A ←→ 5 A (0.4 A / µs)

Skip Mode

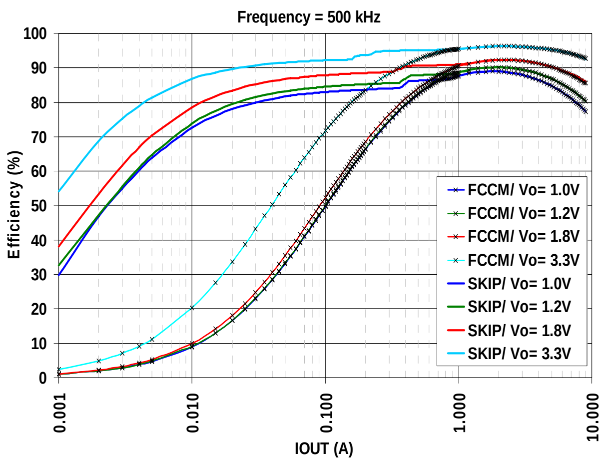


FCCM Mode

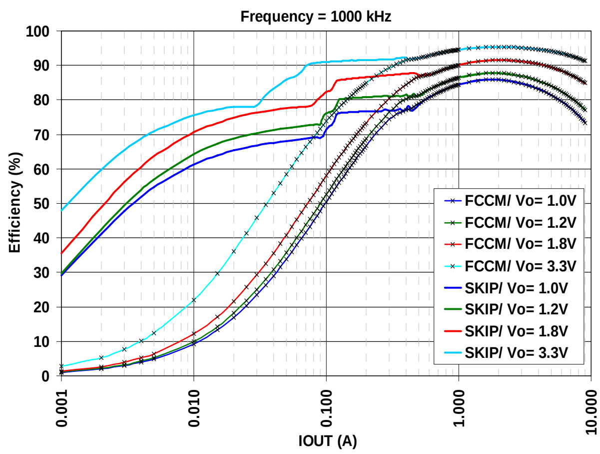


(3) Efficiency

Condition : Vin = 5.0 V, Vout = 1.0 V / 1.2 V / 1.8 V / 3.3 V,
L = 1 µH, Cout = 66 µF (22 µF x 3), Frequency = 500 kHz



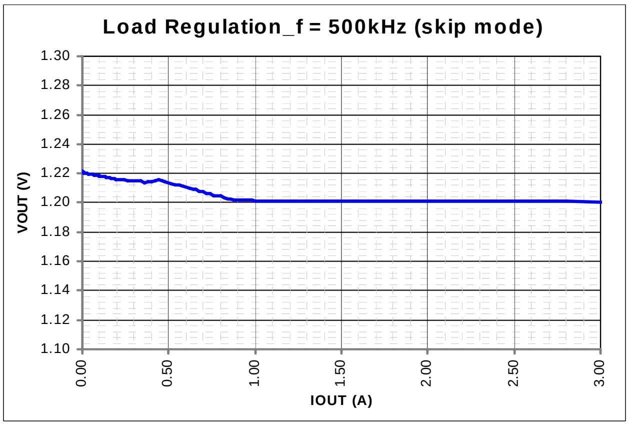
Condition : Vin = 5.0 V, Vout = 1.0 V / 1.2 V / 1.8 V / 3.3 V,
L = 1 µH, Cout = 66 µF (22 µF x 3), Frequency = 1 MHz

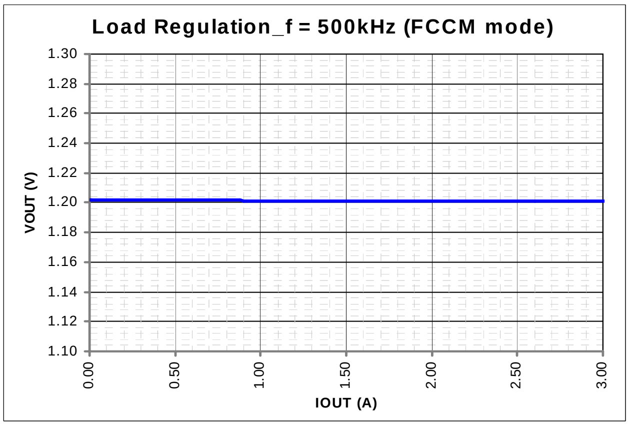


TYPICAL CHARACTERISTICS CURVES (Continued)

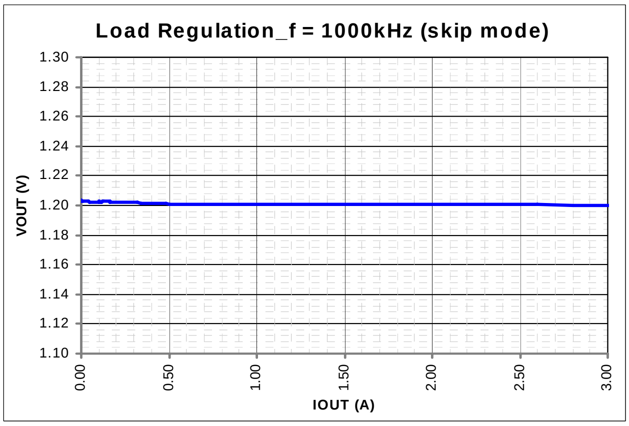
(4) Load regulation

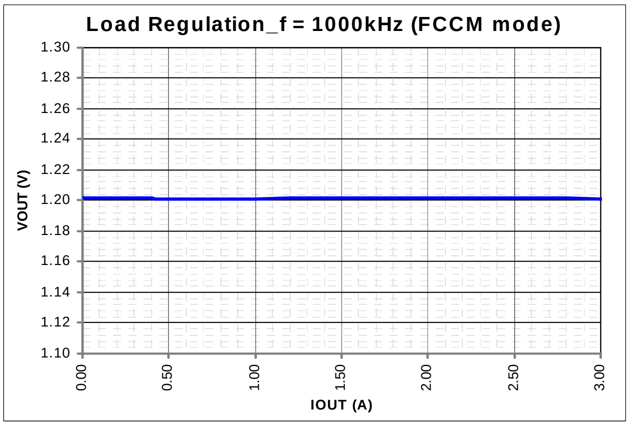
Condition : VIN = 5.0 V, Vout = 1.2 V, Frequency = 500 kHz





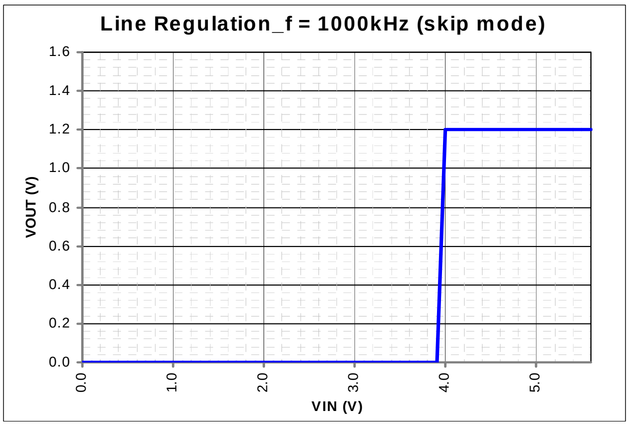
Condition : VIN = 5.0 V, Vout = 1.2 V, Frequency = 1 MHz

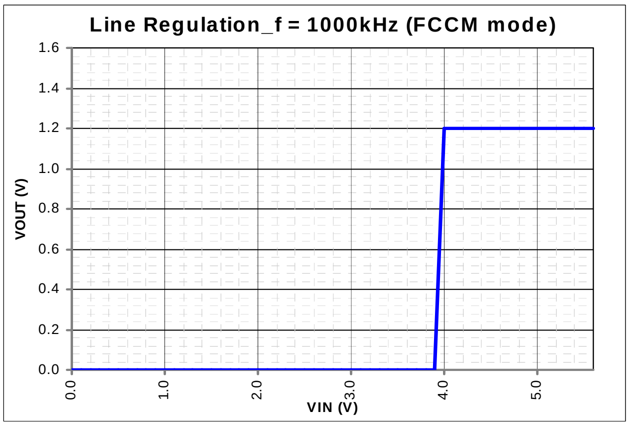




(5) Line regulation

Condition : VIN = 5.0 V, Vout = 1.2 V, Frequency = 1 MHz, Iout = 1.5 A

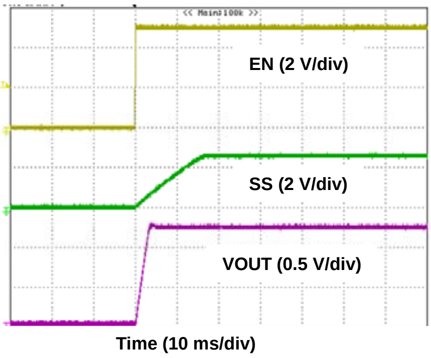


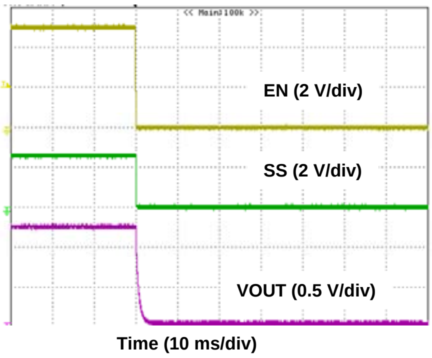


TYPICAL CHARACTERISTICS CURVES (Continued)

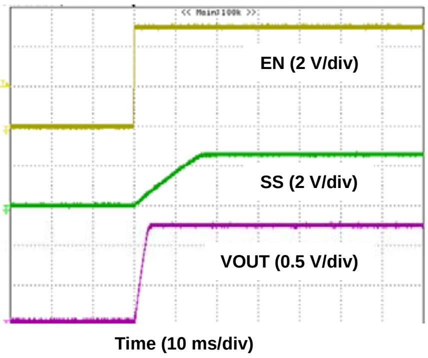
(6) start/shut down

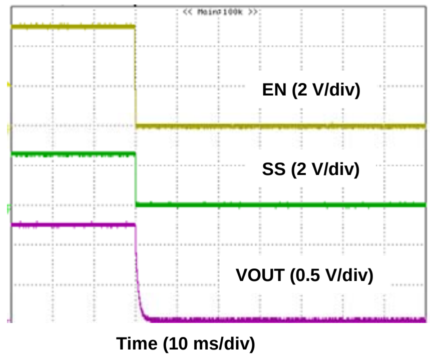
Condition : VIN = 5 V, Vout = 1.2 V, Frequency = 1 MHz, SKIP mode, Iout = 0 A



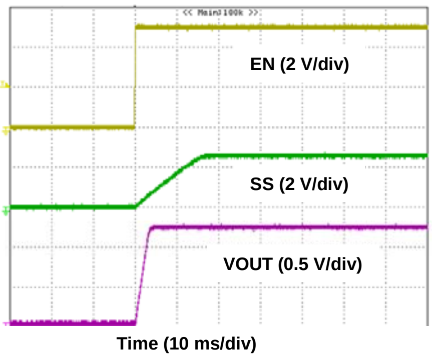


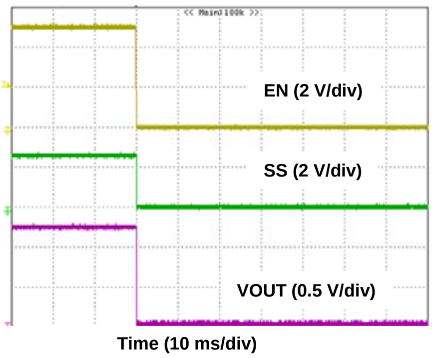
Condition : VIN = 5 V, Vout = 1.2 V, Frequency = 1 MHz, FCCM mode, Iout = 0 A



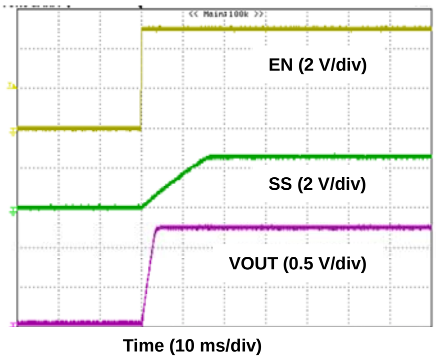


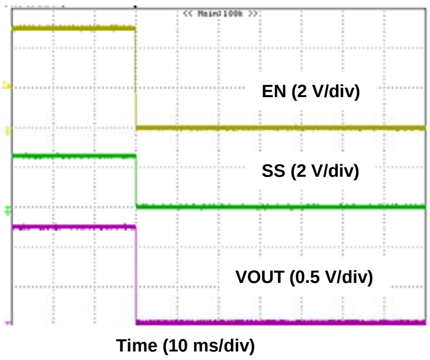
Condition : VIN = 5 V, Vout = 1.2 V, Frequency = 1 MHz, SKIP mode, Rload = 0.5 Ω





Condition : VIN = 5 V, Vout = 1.2 V, Frequency = 1 MHz, FCCM mode, Rload = 0.5 Ω



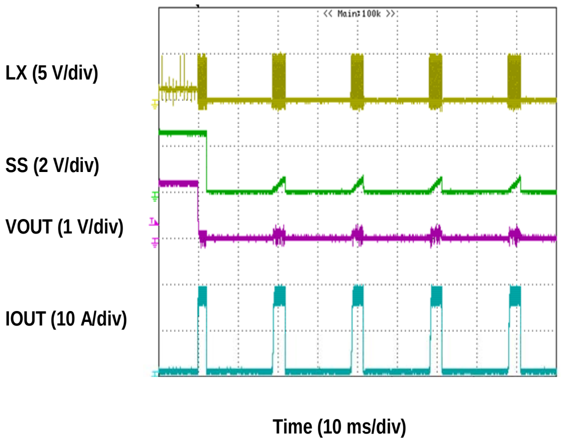


TYPICAL CHARACTERISTICS CURVES (Continued)

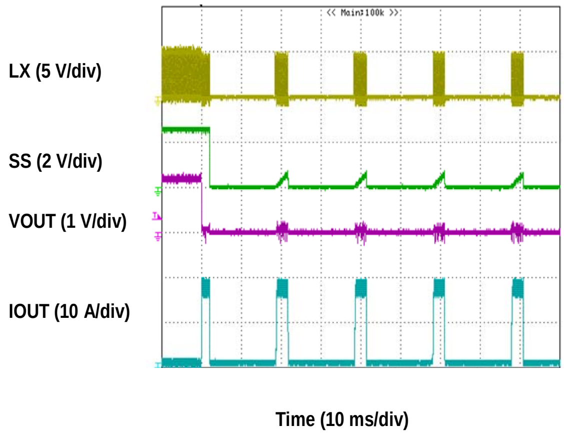
(7) Short Current Protection

Condition : VIN = 5 V, Vout = 1.2 V, Frequency = 1 MHz

Skip Mode

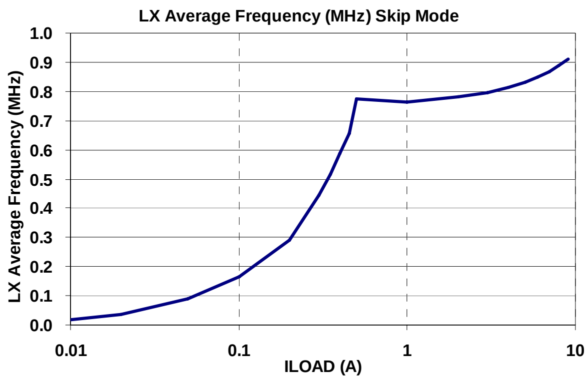


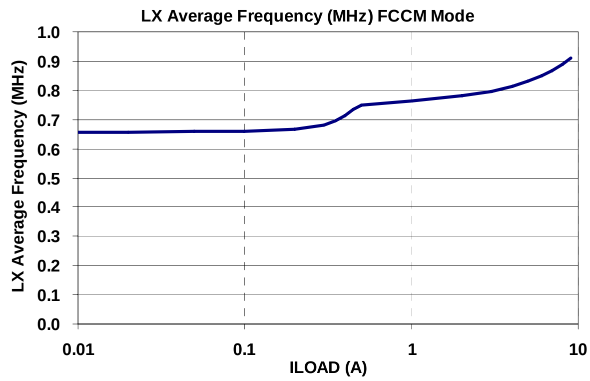
FCCM Mode



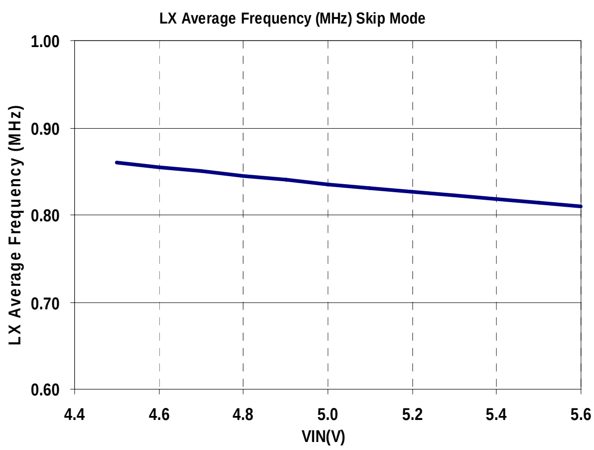
(8) Switching Frequency

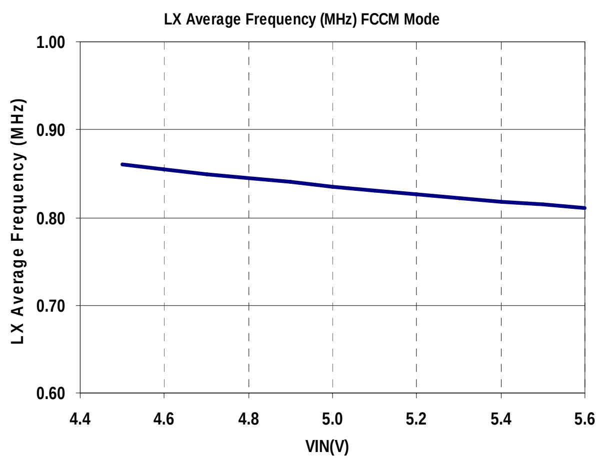
Condition : Vin = 5 V, Vout = 1.2 V, Frequency = 1 MHz, Iout = 10 mA to 9 A





Condition : Vin = 4.5 V to 5.6 V, Vout = 1.2 V, Frequency = 1 MHz, Iout = 5 A

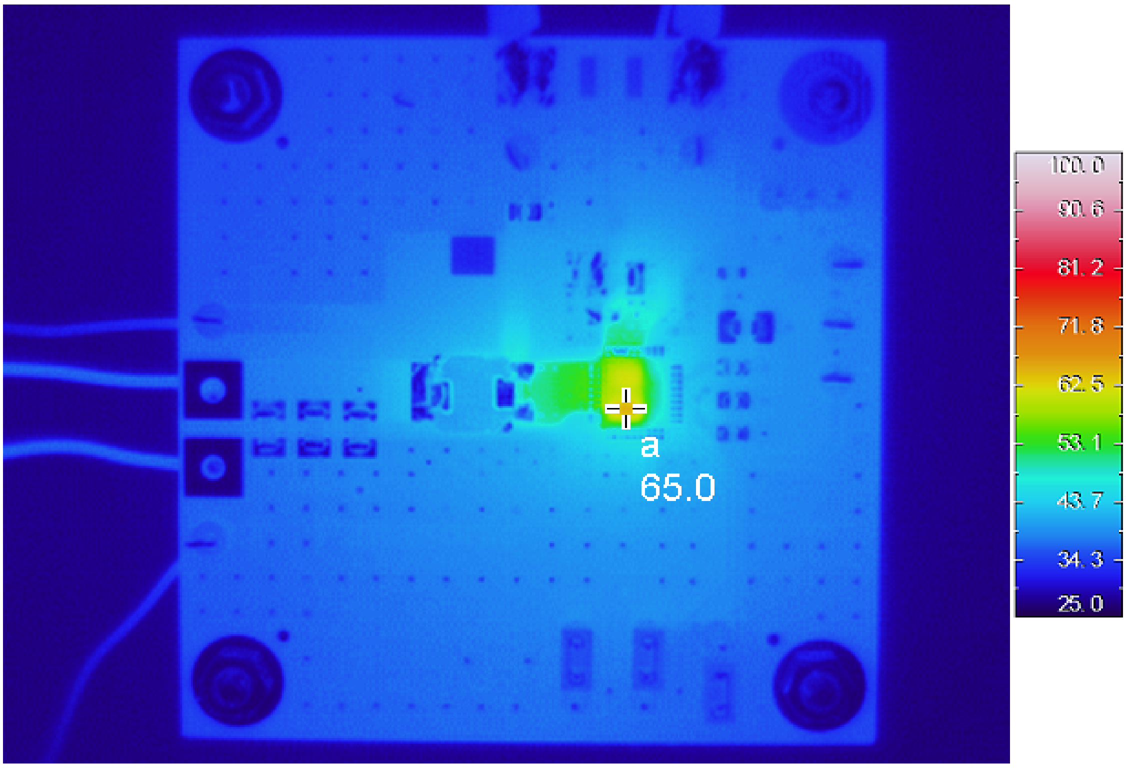




TYPICAL CHARACTERISTICS CURVES (Continued)

(9) Thermal Performance

Condition : VIN=5V , Vout = 1.2V , Frequency = 1000kHz , ILoad = 6A , FCCM Mode



APPLICATIONS INFORMATION

Condition : Vout = 1.2 V, Frequency = 1 MHz, FCCM mode

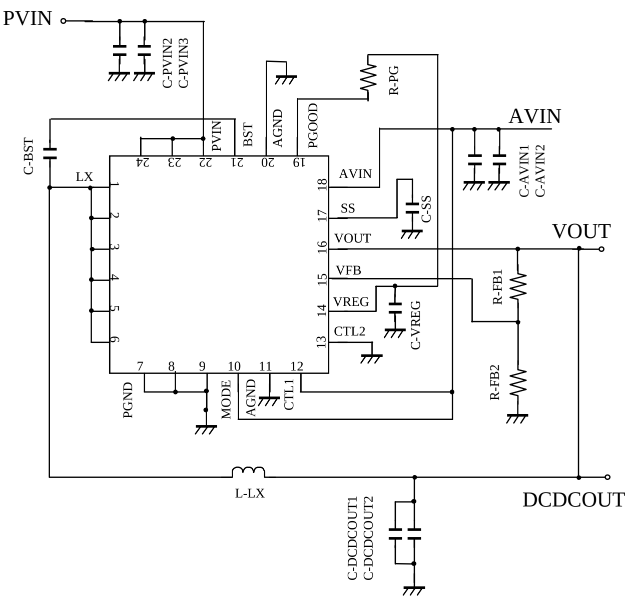


Figure : Application circuit

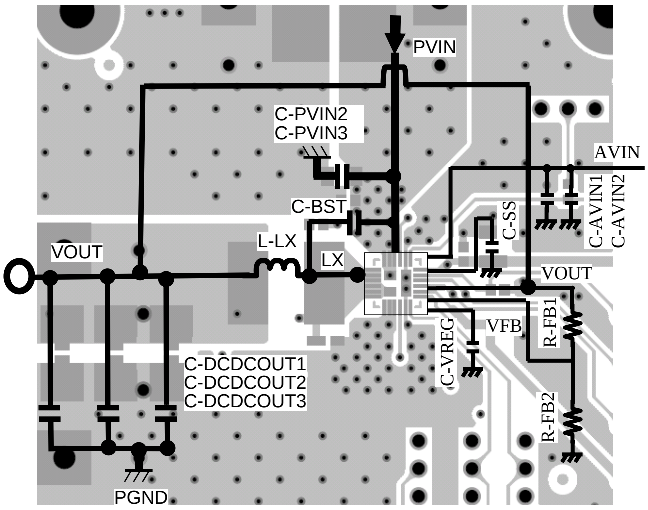


Figure : layout

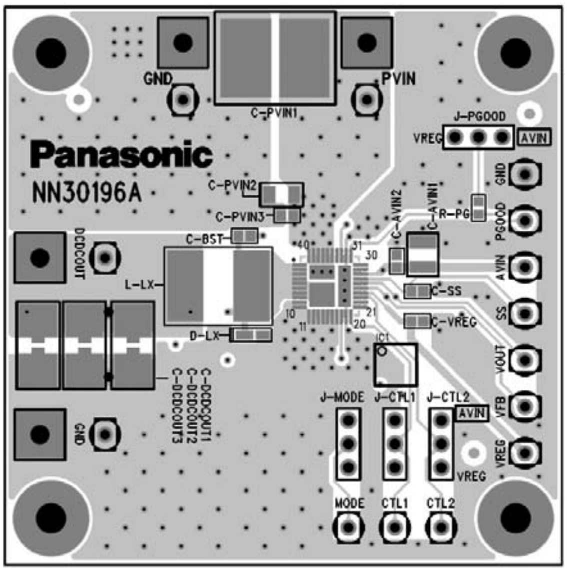


Figure : Top Layer with silk screen
(Top View) with Evaluation board

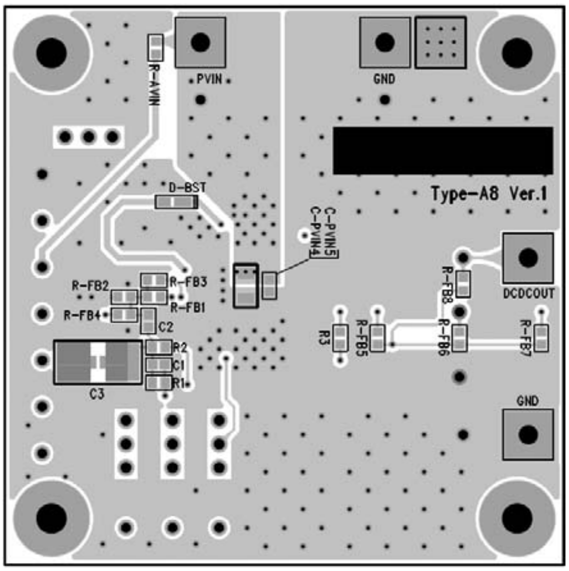


Figure : Bottom Layer with silk screen
(Bottom View) with Evaluation board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

APPLICATIONS INFORMATION (Continued)

Reference Designator	QTY	Value	Manufacturer	Part Number
C-AVIN1	1	10 µF	Murata	GRM21BR71A106KE51L
C-AVIN2	1	0.1 µF	Murata	GRM188R72A104KA35L
C-BST	1	0.1 µF	Murata	GRM188R72A104KA35L
C-DCDCOUT	3	22 µF	Murata	GRM31CR71E226KE15L
C-PVIN2	1	22 µF	Murata	GRM31CR71A226KE15L
C-PVIN3	1	0.1 µF	Murata	GRM188R72A104KA35L
C-SS	1	10 nF	Murata	GRM188R72A103KA01L
C-VREG	1	1.0 µF	Murata	GRM188R71E105KA12L
L-LX	1	1.0 µH	TDK	SPM6530-1R0M120
R-AVIN	1	0	Panasonic	ERJ3GEY0R00V
R-FB1	1	1.0 kΩ	Panasonic	ERJ3EKF1001V
R-FB2	1	1.5 kΩ	Panasonic	ERJ3EKF1501V
R-FB3	1	0	Panasonic	ERJ3GEY0R00V
R-FB6	1	0	Panasonic	ERJ3GEY0R00V
R-FB6	1	0	Panasonic	ERJ3GEY0R00V
R-PG	1	100 kΩ	Panasonic	ERJ3EKF1003V

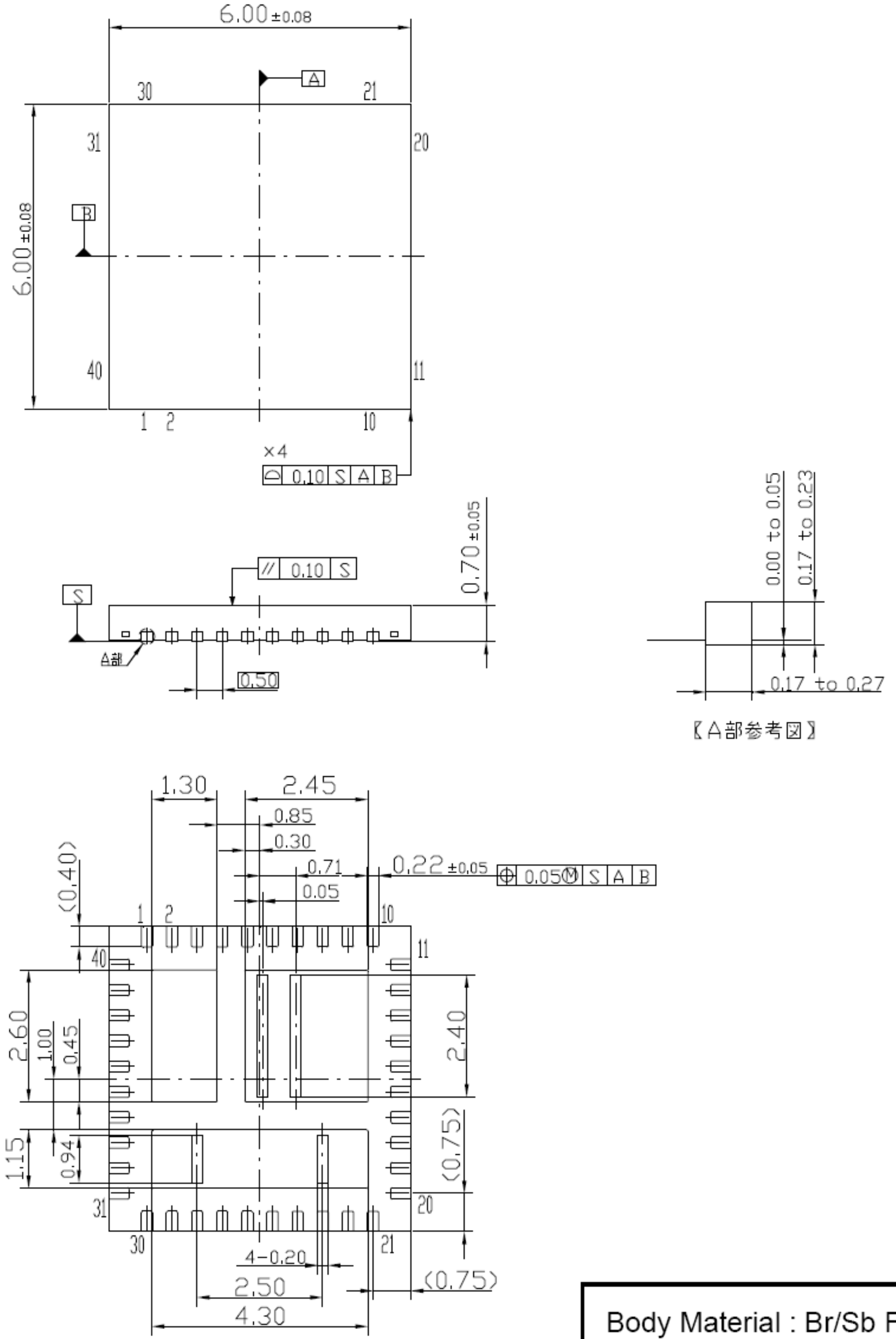
Figure : Recommended component

PACKAGE INFORMATION (Reference Data)

Outline Drawing

Unit : mm

Package Code : HQFN040-A3-0606



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

PACKAGE INFORMATION (Reference Data)

Power dissipation (Supplementary explanation)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity. （Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

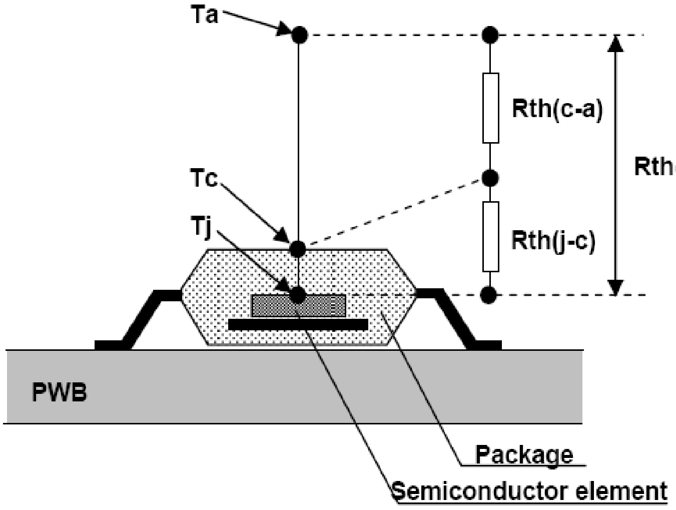


Fig1. Definition image

[Definition formula]

$$Tj = \{Rth(j\text{-}c) + Rth(c\text{-}a)\} \times P + Ta$$
$$= Rth(j\text{-}a) \times P + Ta$$

$$Rth(j\text{-}c) = \frac{Tj - Tc}{P} \quad (°C/W)$$

$$Rth(c\text{-}a) = \frac{Tc - Ta}{P} \quad (°C/W)$$

$$Rth(j\text{-}a) = \frac{Tj - Ta}{P} \quad (°C/W)$$

$$= Rth(j\text{-}c) + Rth(c\text{-}a)$$

P:power(W)

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1.The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

2.When using the LSI for new models, verify the safety including the long-term reliability for each product.

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Be sure to read the notes to descriptions and the usage notes in the book.

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(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.

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