APPLICATION NOTE

Video Amplifier Board with TDA4885 and CR6927

AN97039

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Application Note AN97039

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Video Amplifier Board with TDA4885 and CR6927

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Author(s):

P. Rombout
Philips Semiconductors Systems Laboratory Eindhoven,
The Netherlands.

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Summary

This report describes the video amplifier board with 150 MHz video controller TDA4885 and 140 MHz hybrid active load output amplifier CR6927. The printed circuit board is designed to drive both 15" and 17" colour monitors with 100 MHz bandwidth. AC-coupling to the cathodes is used, which enables a low supply voltage. Together with the choice for the active load module with low static power dissipation, this results an economical board with a small heatsink. This AC-coupling does need additional circuitry, such as a buffer, negative supply for the CR6927 inputs as well as DC-restoration at the cathodes. With the included I^2C-software, functions such as contrast, brightness, OSD contrast, individual gain and individual black-level control are available. The board is capable of receiving signals for beam current limiting and gain modulation. A system description with highlights of TDA4885 and CR6927 is given. Block diagram and schematics of the system is explained. Also, measuring data and various design hints are included. For a description of an DC-coupled application, see Application Note AN96074: 'Video Amplifier Board with TDA4885 and CR1296'.

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1. INTRODUCTION

This report describes the video amplifier demo board with video controller TDA4885 and output amplifier CR6927. It is designed to drive both 15" and 17" colour monitors with 100 MHz. A separate On Screen Display (OSD) generator is present on the board. AC-coupling to the cathodes is used, which means a low output amplifier supply voltage and therefore, a low power dissipation. A DC-restore circuit is implemented with a simple diode clamp and an amplifier with only four transistors for three channels. The active load amplifier CR6927 has a low static power dissipation, but requires a buffer between TDA4885 and its inputs in order to yield a 100MHz bandwidth. Also, a negative supply voltage is needed to drive the CR6927 inputs.

2. SYSTEM DESCRIPTION

The video amplifier system consists of: pre-amplifier, control functions, OSD generator, I²C-bus and output amplifier, as shown in figure 1.

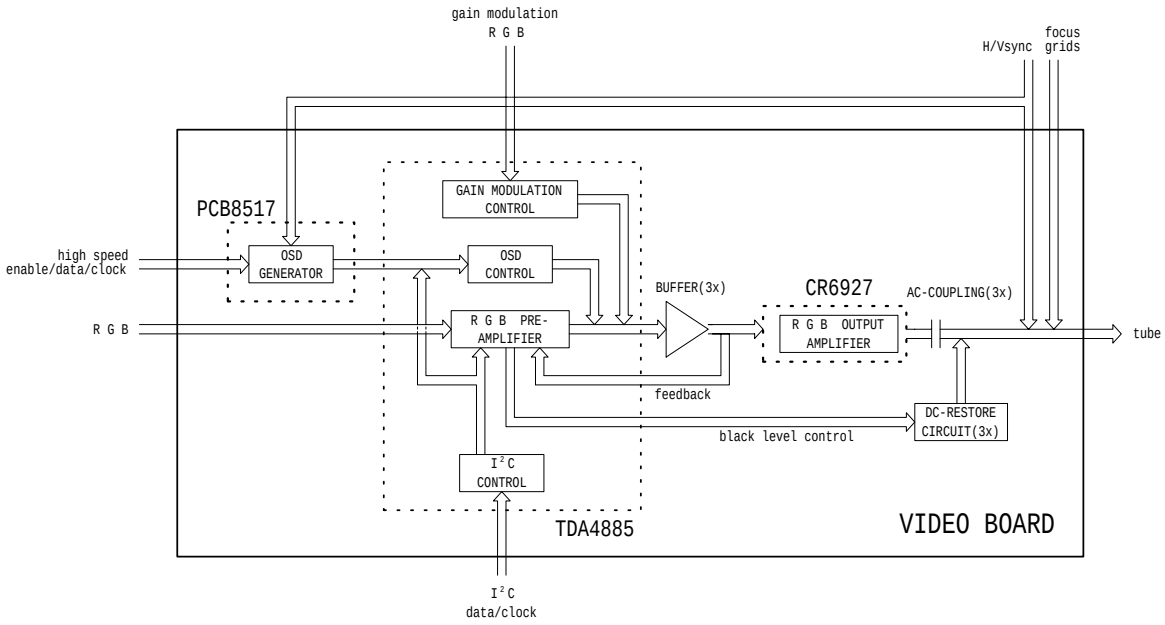


Fig.1 Block Diagram Video Board

Video controller IC TDA4885 and output amplifier hybrid CR6927 are the core of the video board, the rest of the circuitry serves as drive or interface for these devices. The two following subparagraphs will be devoted to the TDA4885 and CR6927. OSD generator PCB8517 will be described in the third subparagraph.

2.1 Video Controller TDA4885

The TDA4885 is a 150 MHz RGB pre-amplifier for colour monitor systems with On Screen Display (OSD) and I²C-bus. It can drive discrete stages as well as hybrid video modules. The pre-amplifier is used with positive feedback from output (or buffer output) for AC-coupling with fixed black-level output. Black-level restore at the cathodes is possible with the aid of three external DAC reference voltages. I²C-bus control software is being delivered on diskette with the video board, appendix 1 shows the software menu with the options mentioned above.

2.1.1 Pinning

Pin description of the TDA4885 is given in table 1. For more characteristics, the TDA4885 data sheet (Ref. 1) can be used for reference.

TABLE 1: Pin Description TDA4885

SYMBOL	PIN	PARAMETERS	DESCRIPTION
FBL	1	1.1 V ≤ threshold ≤ 1.7 V	Fast blanking for OSD insertion
OSD_1	2	-6 ns ≤ delay after FBL ≤ +6 ns, t_{rise}/t_{fall} ≤ 7 ns	OSD input channel 1 (green)
OSD_2	3	"	OSD input channel 2 (red)
OSD_3	4	"	OSD input channel 3 (blue)
CLI	5	1.2 V ≤ threshold ≤ 1.6 V (blanking) 2.6 V ≤ threshold ≤ 3.5 V (clamping)	Vertical blanking input; clamping input
V_{i1}	6	0.7 V referred to black, 4.0 V during input clamping	Signal input channel 1 (green)
V_p	7	8.0 V typ., 7.6 V min, 8.8 V max.	Supply voltage
V_{i2}	8	See pin 6	Signal input channel 2 (red)
GND	9		Ground
V_{i3}	10	See pin 6	Signal input channel 3 (blue)
HFB	11	2.6 V ≤ threshold ≤ 3.5 V (clamping) 1.0 V ≤ threshold ≤ 1.8 V (blanking)	Horizontal flyback input for output clamping and blanking
GM_1	12	open-circuit: 2.0 V; ground: no gain modulation (max. gain); modulated gain: 1 - 3 V. *See figure 4.*	Gain modulation input channel 1 (green)
GM_2	13	See pin 12	Gain modulation input channel 2 (red)
GM_3	14	See pin 12	Gain modulation input channel 3 (blue)
SDA	15	0 V ≤ V_{LOW} ≤ 1.5 V, 3.0 V ≤ V_{HIGH} ≤ 5.0 V	I^2C-bus serial data input
SCL	16	Clock ≤ 100 kHz	I^2C-bus serial clock input
LIM	17	4.5 V: start contrast/OSD contrast reduction, 2.0: max. reduction (-25 dB), 5.0 V open-circuit	Beam current limiting
GND_3	18		Ground channel 3
V_{p3}	19	8.0 V typ., 7.6 V min., 8.8 V max.	Supply channel 3
V_{o3}	20	2.8 V (nom. contrast, max. gain) ≤ V_{o3} ≤ 4.5 V (max. contrast, max. gain) 0.5 V ≤ black level ≤ 2.5 V	Signal output channel 3 Actual black level depends on external feedback network
FB_3	21	4.0 V ≤ FB_3 ≤ 5.8 V negative feedback, 0.7 V positive feedback	Feedback input channel 3

TABLE 1: Pin Description TDA4885

SYMBOL	PIN	PARAMETERS	DESCRIPTION
REF_3	22	$4.0\ V \leq REF_3 \leq 5.8\ V$	Reference voltage channel 3
GND_2	23		Ground channel 2
V_{p2}	24	See pin 19	Supply channel 2
V_{o2}	25	See pin 20	Signal output channel 2
FB_2	26	See pin 21	Feedback input channel 2
REF_2	27	See pin 22	Reference voltage channel 2
GND_1	28		Ground channel 1
V_{p1}	29	See pin 19	Supply channel 1
V_{o1}	30	See pin 20	Signal output channel 1
FB_1	31	See pin 21	Feedback voltage channel 1
REF_1	32	See pin 22	Reference channel 1

2.1.2 Block Diagram

In appendix 2, the internal block diagram of the TDA4885 is depicted. Diagram sections and their functioning are listed in the paragraphs below.

2.1.3 Signal Input Stage

The RGB signal inputs (0.7 V) must be capacitively coupled (10 nF recommended) to the TDA4885 from a low-ohmic source (75 Ω recommended). These AC-coupling capacitors allow level shift and clamping of the input signals to reference black level. Missing input clamping pulses will result in black output signals because internal leakage currents discharge the coupling capacitor. A clipping circuit cuts all signal parts below black level. Video signals can be enabled or disabled by I^2C-bus.

2.1.4 Electronic Potentiometer Stages

Three electronic potentiometer stages are present as 6-bit, I^2C-driven, DACs with the following functions:

CONTRAST CONTROL
This DAC simultaneously adjusts all three input signals related to reference black level with a range of 25 dB.

BRIGHTNESS CONTROL
Video black level can be shifted in relation to reference black level for all three channels simultaneously. A negative setting will shift dark signal parts in ultra black and a positive setting will change background from black to grey.

GAIN CONTROL
Gain is an individually controlled white point adjustment, that controls video signals related to reference black level over a range of 7 dB. It affects the complete grey scale. It is used to compensate for the sensitivity of the R/G/B guns and phosphors (the three colours need a different drive for a white picture). With gain control, Accu Colour can be implemented.

2.1.5 Output Stage

The output RGB signals are amplified to 2.8 V_{pp} (12 dB) at nominal contrast and maximum gain. At maximum contrast and gain settings, output voltage is 4.5 V_{pp} (16 dB). Reference black level is controllable from 0.5 to 2.5 V. Total output voltage range is limited from 0.5 to Vp-2.0 V.

2.1.6 Pedestal Blanking

Output signals can be blanked to ultra black level by setting pedestal blanking (bit PEDST=1), which adds 0.45 V during clamping. This is necessary for AC-coupling applications with a passive clamp diode circuit as DC-restoration to prevent unwanted clamping during video overshoots. With pedestal blanking, the clamping pulse surely is the highest voltage, and black level is restored during clamping only.

2.1.7 Output Clamping, Feedback References and DAC Outputs

Output clamping stabilises the reference black level at the output. Without clamping pulses, output signals will go to switch-off voltage because the integrated storage capacitors will discharge. In case of AC-coupling, the buffer output (emitter) voltage is fed back to the IC. Without the buffer, the TDA4885 output is directly connected to its feedback pin. During output clamping, this feedback voltage is compared to 0.7 V. Output control range during clamping is 0.5 V to 2.5 V. Figure 2 depicts output signal with variable gain, contrast and brightness.

2.1.8 Horizontal Clamping and Vertical Blanking Pulses

Threshold for input line clamping is 3 V and for vertical blanking 1.4 V. Vertical blanking is only enabled when the input signal is present for a certain minimum time between 1.4 V and 3 V. During vertical blanking, signal and brightness blanking are activated and possible pedestal blanking. Input signals have to be at black level during the input clamping pulse. Figure 3 gives a timing diagram for clamping/blanking pulses.

2.1.9 Horizontal Flyback Pulses

Horizontal flyback pulse HFB has two levels: 1.4 V at which signal blanking, brightness blanking and possible pedestal blanking are activated and 3 V at which additionally the output clamped feedback loop is activated.

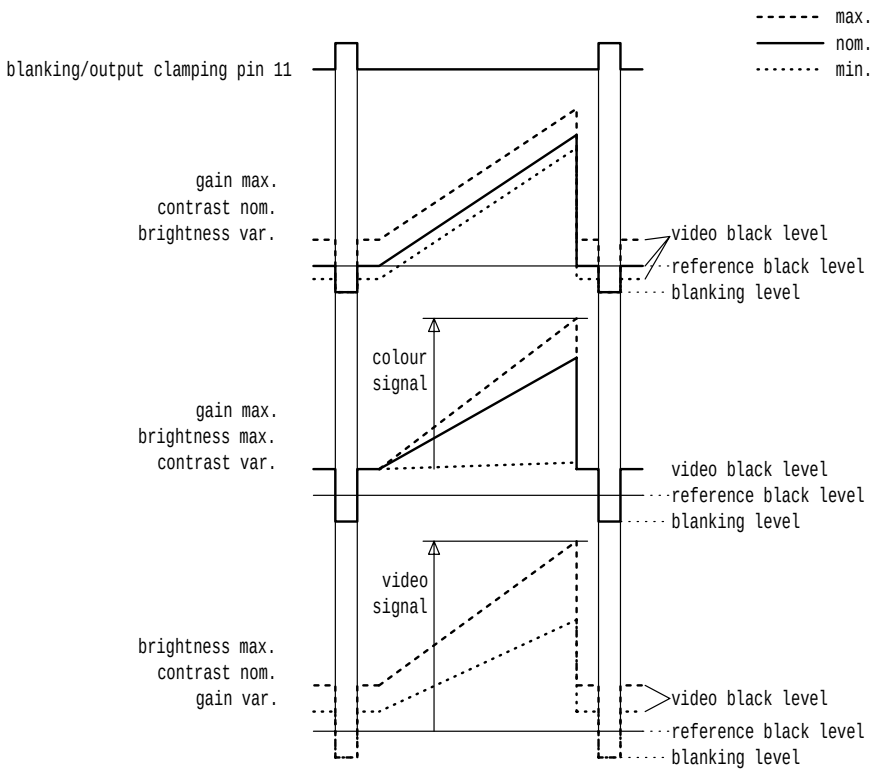


Fig.2 Signal Output TDA4885

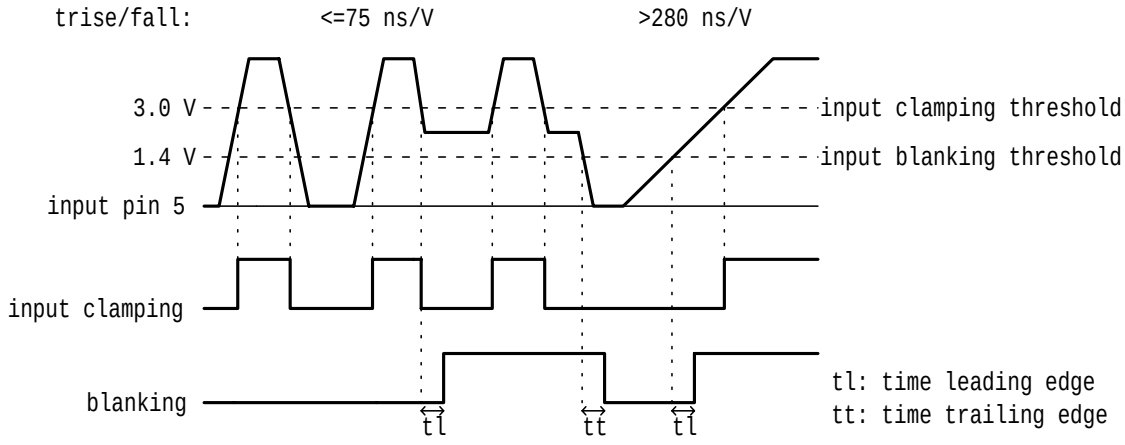


Fig.3 Timing diagram clamping and blanking pin 5

2.1.10 OSD and OSD Contrast

If fast blanking input at pin FBL rises above its 1.4 V threshold, video input signals are blanked and OSD signals enabled. Amplification of inserted signals OSD1 to -3 can be controlled by a 4-bit I^2C-driven DAC 'OSD contrast' with a range of 12 dB. OSD signals track with brightness and gain control as normal signals, but is independend of video contrast. It is possible to enable/disable OSD signals by I^2C-bus.

2.1.11 Beam Current Limiting

Beam current limiting by means of contrast reduction is possible with an external voltage at pin LIM. Maximum overall voltage gain of contrast and OSD contrast control can be reduced by 26 dB (4.5 V: start of reduction, 2.0 V: maximum reduction).

2.1.12 Gain Modulation

Gain modulation is possible in order to achieve brightness uniformity over the screen by applying appropriate waveforms to the input pins GM1, GM2 and GM3.
Open-circuit pins are at 2.0 V and yield a gain reduction of 20%. A symmetrical gain modulation is achieved by a signal input of 1.0 to 3.0 V. This will modulate the open-circuit gain with -18% to +18%. If this feature is not used, the pins should be grounded for maximum voltage gain. Figure 4 clarifies the effect of the gain modulation input range.

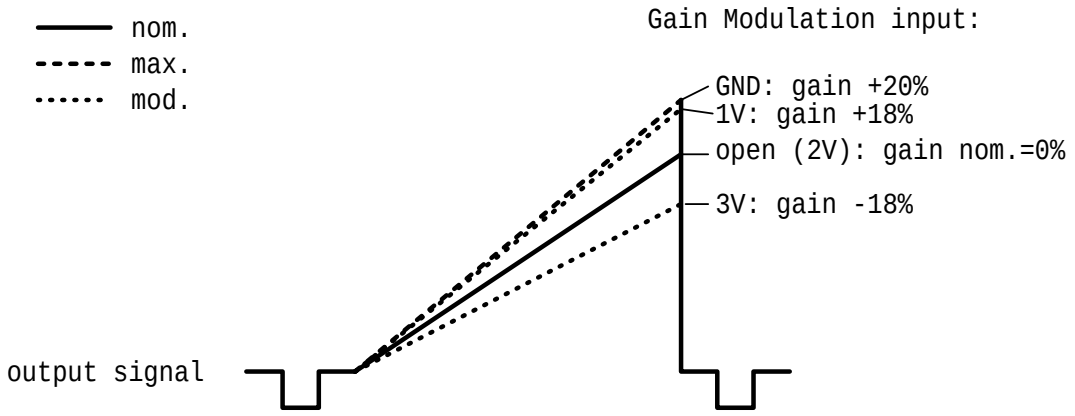


Fig.4 Output Signal Modulated Gain

2.1.13 I^2C-bus Control

An I^2C-bus receiver is present for the following functions:
- Contrast control with 6-bit DAC (25 dB);
- Brightness control with 6-bit DAC (10-30% of nominal signal amplitude);
- OSD contrast control with 4-bit DAC (12 dB);
- Gain adjustment with 6-bit DAC for each channel (7 dB);
- Black level adjustment with 8-bit DAC for each channel;
- Control register for:
  - feedback polarity
  - RGB video on/off
  - OSD on/off
  - pedestal blanking on/off.

Registers are set to logic '0' after power-up and internal power-on reset of I^2C-bus.

2.2 Output Amplifier CR6927

The video output amplification is achieved by hybrid module CR6927. This is a three channel (class AB active load) amplifier with a small-signal bandwidth of 140 MHz and an open loop voltage gain of 180. A feedback resistor R_{fb} is applied internally, which means the closed loop gain can adjusted by the input resistor R_{in} (see figure 5).

2.2.1 Pinning

Table 2 gives a pin description of the CR6927, more characteristics can be found in its data sheet (Ref. 2).

TABLE 2: Pin Description CR6927

SYMBOL	PIN	PARAMETERS	DESCRIPTION
V_{s1}	1	75 V - 90 V max.	Signal Supply channel 1 (blue)
V_{i1}	2	1.5 V typ.	Signal Input channel 1
GND	3		Ground
V_{o1}	4	$\frac{1}{2}V_{s1}$ typ.	Signal Output channel 1
V_{s2}	5	See pin 1	Signal Supply channel 2 (red)
V_{i2}	6	See pin 2	Signal Input channel 2
GND	7		Ground
V_{o2}	8	See pin 4	Signal Output channel 2
V_{s3}	9	See pin 1	Signal Supply channel 3 (green)
V_{i3}	10	See pin 2	Signal Input channel 3
GND	11		Ground
V_{o3}	12	See pin 4	Signal Output channel 3

2.2.2 Internal Circuit

The simplified internal circuit of one channel of the module is depicted in figure 5.

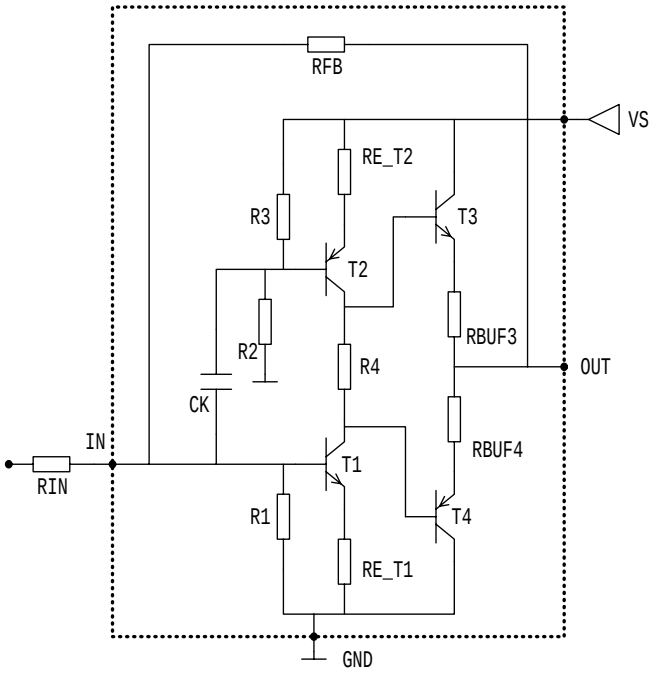


Fig.5 Internal Circuit Video Hybrid CR6927

The closed loop gain A is determined by R_{in} (for instance 326Û of this application):

$$A = \frac{A_0}{1 + A_0 * \frac{R_{in}}{R_{fb}}} \approx \frac{R_{fb}}{R_{in}} \qquad \text{Equ. 1}$$

$$= \frac{4k3}{326} = 13.2$$

2.3 OSD Generator PCB8517

The PCB8517 is a stand-alone OSD generator, controlled by the microcontroller on the deflection board via a three-wire high-speed serial interface. Horizontal and vertical position on screen, as well as character height, colour and font can be programmed. The on-chip PLL oscillator adjust character size to the current graphic mode. Additional information is specified in its data sheet (Ref. 3).

2.3.1 Pinning

Pinning of the PCB8517 is shown in table 3 below.

TABLE 3: Pin Description PCB8517

SYMBOL	PIN	PARAMETERS	DESCRIPTION
GND_A	1		Analog Ground
VCO	2		Voltage Controlled Oscillator
BIAS	3		Bias Current Internal Oscillator
V_{sA}	4	4.75 V min, 5.0 V typ., 5.25 V max.	Analog Supply
HS	5		Horizontal Sync Pulse
ENN	6		Serial Interface Enable, active low
SDI	7		Serial Interface Data
SCK	8		Serial Interface Clock
V_{sD}	9	See pin 4	Digital Supply
VS	10		Vertical Sync Pulse
HTONE	11		Halftone, not used in this application
FB	12		Fast Blanking
B	13		Blue Channel Output
G	14		Green Channel Output
R	15		Red Channel Output
GND_D	16		Digital Ground

3. SYSTEM SCHEMATICS

This paragraph will explain the depicted schematics of the video board. The two main building blocks of the board are the TDA4885 and CR6927 with peripheral components that will be described first. Supply will be treated in more detail in paragraph 5.2 on design hints. PCB lay-out will be explained and finally power and heatsink calculations for the CR6927 are given.

3.1 Application Circuit

Schematics of the circuit around the TDA4885 and CR6927 is depicted in appendix 3. The video board also interconnects the horizontal and vertical sync pulses from monitor input to deflection board and signals like heater, Vg1 etc. from deflection board to picture tube. The monitor alignment procedure is included (adjusting black-level, white point etc.) in appendix 4.

3.1.1 TDA4885 Application

* OSD inputs: generated by the separate OSD-generator PCB8517. These inputs are coupled via a 100 Ω resistor to PCB8517.
* Clamping and blanking inputs, connected via 100 Ω to CON2. These signals are generated on the deflection board.
* RGB-inputs: these signals are 0-0.7 V and connected via a 75 Ω cable, which means a 75 Ω terminator must be present at the input on the video board. A 10 nF capacitor with a 33 Ω series resistor connects the incoming signal to the input pins.
* Supply voltage 8 V from voltage stabilizer uA7808 (IC3), decoupled locally with a chip capacitor.
* Gain modulation inputs, connected via 100 Ω to connector CON3. If this feature is unused, the pins can grounded.
* SDA/SCL I^2C-bus inputs, generated by I^2C-controller on deflection board. Pull-up resistors are present on deflection board. Signals come in via connector CON1 and 220 Ω series resistors.
* Beam Current Limiter (BCL), generated on deflection board from CON2 via 100 Ω. This signal must force the open-pin voltage of 5 V down to a range of 4.5 to 2.0 V when beam current must be limited. A 10 nF capacitor is used to filter possible noise that might cause interference. A pull-up resistor ensures a voltage greater than 4.5 V in case beam current limiting must not be activated.
* Channel outputs: coupled to the CR6927 via a buffer (BFG35). All channels have separate ground and supply voltage.
* Feedback from emitter of BFG35 buffer. The TDA4885 is set to positive feedback (AC-coupling) and feedback black level during the clamp pulse is controlled at 0.7 V.
* External feedback reference voltages, used for the DC-restoration circuit in AC-coupling applications.

3.1.2 CR6927 Application

* RGB channel inputs, require a voltage swing of about 3-4 V_{pp} (dependent on closed loop gain) around 1.5 V, connected through R_{in}, that will determine the closed loop gain (see equation 1). In order to shift the input signals to the levels, delivered by the pre-amp, pull-down resistors R*08 haven been added.

* Output pins, connected via coupling capacitor and a flash resistor to the cathodes. A clamping diode pulls the cathode voltage to a DC-restore value every horizontal flyback. This diode also leads possible flashes on the cathodes away from the video amplifier's outputs. The diode (BAV21) must be able to withstand the flash current that is limited by the flash resistor (47 Ω, for calculations see appendix 5).
* Supply voltage (78 V) from deflection board and ground for each channel, decoupled locally by a chip capacitor.

3.1.3 PCB8517

* High speed serial bus with enable, clock and data line, driven by the microcontroller on deflection board via 100Ω. Pull-up resistors (4k7) are also applied.
* H/V sync pulse inputs, connected via 100Ω to the H/V connectors.
* Phase Locked Loop (PLL) filter input and BIAS input for the Voltage Controlled Oscillator.
* 5 V analog and digital supply voltage and ground, separately decoupled.
* RGB and Fast Blanking (FB) outputs, connected via 100Ω to TDA4885 OSD inputs.

3.1.4 Buffer

A buffer transistor (BFG35) is used to increase the sink and source current for the output stage. The feedback pin of the TDA4885 must be connected to the emitter of this emitter follower in order to minimize smearing. Since the buffer is connected to a negative supply, the feedback pin must be set to > 300mV during start-up to avoid latch-up. This is done by connecting a divider to the feedback pin of the TDA4885 with a pull-up resistor to +8 V and a resistor to the emitter of the buffer.

3.1.5 DC-Restoration Circuit

The DC-restoration circuit must be a temperature independent DC-amplifier. This amplifier is fed by the TDA4885 reference voltages (range 4.0-5.8 V). These voltages are amplified to the desired black-levels at the cathodes (with a range of the maximum 17" tube cut-off voltage difference of 25 V). This is implemented by creating a temperature-dependent voltage at the emitter of the three amplifiers. The DC-amplifiers are closed loop connected transistors in order to achieve a stabile DC output. With only four transistors, it is possible to achieve a three-channel temperature-stabile accurate DC-amplifier.

3.1.6 Heater and grid voltages

Voltages for heater and grids 1 and 2 of the CRT are generated on the deflection board. The grid voltages Vg1 and Vg2 are coupled to the CRT by a 2.7 kΩ series resistor and a 1 nF high-voltage capacitor is connected to ground. Heater voltage is via a 1 Ω resistor and a 10 μH inductor connected to the heater, heater ground is connected by a 10 μH series inductor. Both heater and heater ground are decoupled by a 1.5 nF capacitor to ground. Spikes are caused by fast voltage swings on the cathodes and are, without decoupling capacitors, picked up by the heater and grids. The inductors and 2.7 kΩ resistors ensure that this is the route of least impedance.

Note: The Vg1 voltage, applied to pin 8 of connector 2 must be approximately -50 V, with a superimposed vertical blanking pulse of at least 10 V.

3.2 Printed Circuit Board

In designing the video Printed Circuit Board (PCB), care has to be taken that all connections are as short as possible and connectors have to be placed close to the ICs' input pins. All channel inputs of the TDA4885 are placed at one side (pins 1-16) and outputs at the other (pins 17-32), which makes layout design easy: the inputs enter on one side of the board, followed by TDA4885 that drives CR6927 and at the other side the CRT-socket. The choice was made for a double-sided board to avoid oscillations. With a double-sided board, one side is used as ground plane. This enables short ground returns, reducing EMI. The use of SMD components in combination with leaded components ensures the shortest connection possible between inputs, ICs and outputs. Especially the local decoupling of supply voltages with capacitors 10-100 nF must be close to the corresponding pins, which means it is best to use SMD components. Lay-out of the board is depicted in appendix 6, followed by the components list in appendix 7.

3.3 Heatsink CR6927

The video hybrid module dissipates too much power to conduct to free air. This means a heatsink must be fixed to its mounting base. Figure 6 shows the thermal resistances and corresponding local temperatures.

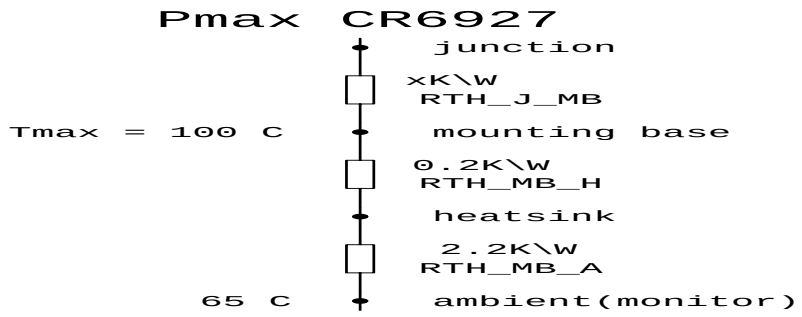


Fig.6 Thermal Resistances Video Module

The maximum power dissipated by the CR6927 is 16.8 Watts (appendix 8 includes calculations that lead to this value). The thermal resistance between mounting base and heatsink is assumed 0.2 °C\W. It is specified that the operating temperature of the CR6927 mounting base is ≤ 100 °C, in order to keep the junction temperatures of the internal transistors within safe limits. The required thermal resistance is specified in equation 2.

$$R_{th}(h-a) = \frac{\Delta T(mb-a)}{P_{max}} - R_{th}(j-h)$$

$$= \frac{100-65}{16.8} - 0.2 = 1.9\ \frac{K}{W}$$

Equ. 2

The mounting base is first fixed to an aluminium block, that is connected to the print. The actual heatsink is mounted to this block, as shown in the cross-section of figure 7. The heat must be conducted well from the block to the heatsink, if necessary with heat-conducting paste.

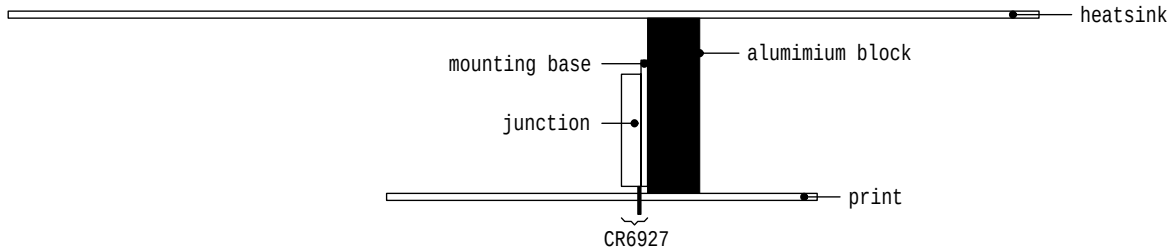


Fig.7 Construction Heatsink on CR6927

The area of the heatsink (2mm thick aluminium) is defined by equation 3.

$$A = \frac{1}{R_{therm} * k}$$

Equ. 3

In which: $k = 1.5*10^{-3}$ W\Kcm^2, for aluminium heatsink 2mm thickness with about the calculated area
A = heatsink area in cm^2
R_{therm} = thermal resistance from heatsink to ambient

With the previously calculated values: A = 1\(1.5*10^{-3} * 1.9) = 350 cm^2, the size of the heatsink is chosen at 13 * 23 =299 cm^2. This is smaller than calculated, but the worst case situation on which this calculation is based is not likely to occur. If necessary, a larger heatsink can be chosen.

4. MEASURING DATA

4.1 Video Performance

Video performance is specified by rise/fall times and DC-voltages at the cathodes. Measurements have been carried out in an actual monitor (15" Mk 2, see Ref. 4). Load capacitance is defined by:

$$C_{load} = C_{tube} + C_{flashdiode} + C_{socket} + C_{print} + C_{sparkgap} \quad \text{Equ. 4}$$

$$= 5.5 + 1.25 + 1.0 + 0.75 + 0.5 = 8.95\ pF$$

The (reference) black-levels on the cathodes can be adjusted between 50 V and 75 V (measured) with the three DAC registers of the TDA4885. This range is sufficient to compensate for the difference of cut-off voltages of one tube.

Figure 8 shows the cathode waveform of a 50 V_{pp} voltage swing at nominal brightness (an Astro video generator is used as a signal source).

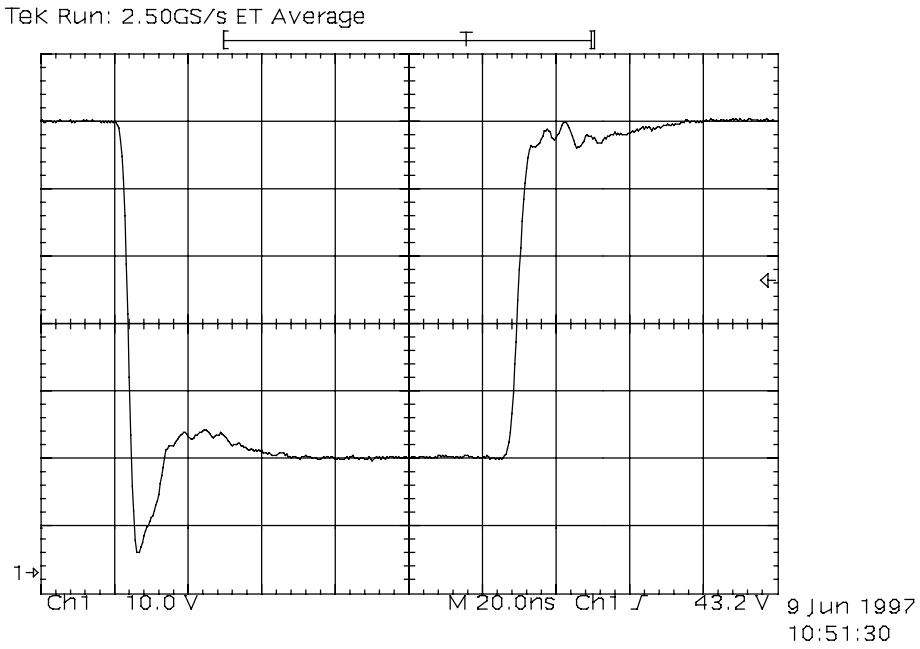


Fig.8 Cathode Voltage Video Board

Rise and fall times (time between 10% and 90% of voltage swing) at the cathodes are measured with a Tektronix TDS520 500MHz oscilloscope using a high-frequency calibrated Tektronix P5100 100x 2.4 pF probe. The corresponding input signal of the TDA4885 is generated by a PM585 pulse generator with rise/fall times smaller than 1 ns. These conditions yield a rise time of 4.4 ns and a fall time of 3.5 ns, at a voltage swing from 15 to 65 V. Overshoot of the white to black transition is below 5%, overshoot from black to white is more than 10%. Bandwidth of this system is calculated by $B = 0.35 \backslash t_{fall}$. Fall time (black to white transition) is the most critical transition time, because it is best visible on screen. Overall system bandwidth is:
$B_{system} = 0.35 \backslash (3.5 * 10^{-9}) = 100$ MHz. The board can be used for pixel rates up to 200 MHz.

4.2 Temperature

Measurements have proved that most power is dissipated in CR6927 when displaying a 100 MHz pixel on/off picture. Temperature measurements have been carried out with the heatsink construction and size as described in paragraph 3.3. The first row of table 4 shows data with a pixel on/off picture at maximum contrast (V_{pp} = 50.4 V) and nominal brightness. The ΔT of this measurement remains the same at a higher ambient temperature. The second row of this table shows the mounting base temperature of CR6927 at the maximum ambient temperature of 65°C, which is the internal monitor temperature.

TABLE 4: Temperature CR6927

	$T_{ambient}$ [°C]	$T_{mounting\ base}$ [°C]	ΔT [°C]
Measured	23.5	57.4	35.7
Calculated	65.0	98.7	35.7

It appears from table 4 that the heatsink is sufficiently large for this worst case situation when placed inside a monitor. It should be noted that it takes the heatsink about half an hour to heat up. This means this worst case temperature of 98.7 °C is not likely to occur, because an on/off picture is hardly ever displayed for half an hour.

5. DESIGN HINTS

When developing a printed circuit board for the TDA4885 and/or the CR6927, certain design rules and hints have to be taken into account. The most critical items are highlighted in the following subparagraphs.

5.1 Ground Routing

A printed circuit video amplifier board that has to operate at frequencies higher than 40 MHz, a double-sided board is needed. The copper in this second side should be used as much as possible as a ground plane. If only ground tracks are used, signal loops will be created. Through these loops, ground currents flow that can easily cause oscillations. In case of a ground plane on one board side, there are hardly any loops which means the chance on ground currents to cause oscillations is limited. The plane also shields the board from electro-magnetic radiation from and to the environment (EMI). This plane, however, does create parasitic capacitance to the signal paths. In order to avoid parasitic capacitance to high-frequency video signal paths, the plane area directly near these signal paths should be cleared.

5.2 Supply

Low voltage supplies (+11 V and -18 V) must enter the board via a series resistor (about 1-10 Ω) and be controlled by a voltage stabilizer or zener diode. The stabiliser should be decoupled by a capacitor (100-330 nF) on both input and output. Output must be stabilised by an elcap of 10 - 68 µF. From this point, the supply voltage must be led to the corresponding voltage pins via a 1-10 Ω series resistor. These supply pins must be locally decoupled by a (chip) capacitor of about 100 nF, placed as close as possible to the pin itself.
For the high voltage supply of 78 V of the CR6927, similar rules must be followed, only for the series resistors, it is recommended to use 1 Ω. This is necessary in order to reduce supply variations by high peak currents. This is not necessary for the +185 V supply, it enters the board via 100Ω, because high peak currents do not occur.

5.3 Buffer

A buffer between pre- and output amplifier is applied, because the maximum sink and source current of the TDA4885 outputs are 12 and 15 mA respectively. The CR6927 needs a higher current in order to achieve its maximum rise and fall times. The necessary current can be calculated by equation 5, based on the fall time (video black to white transition), which is best visible on screen.

$$I = \frac{V_{pp(10\%-90\%)} * C_{load}}{t_{fall}} \qquad \text{Equ. 5}$$

More information on the internal capacitance (2.4 pF) is given in appendix 8.
A fall time of 3.5 ns (measured from 10% to 90% of the voltage swing) and a maximum voltage swing of 50 V_{pp} (40 V 10%-90%), this yields:

$$I = \frac{40 * 2.4p}{3.5n} = 27.4mA$$

The buffer is an emitter follower (npn transistor BFG35) with an emitter resistor to -8 V supply, that will determine the sink and source current. During white video level of the TDA4885 output, the buffer current must be at least 26.3 mA. Video white level for a 50 V_{pp} output swing is:
$V_{clamp}+V_{pedestal}+V_{signal}$ = 0.7+0.45+4.0 = 5.15 V. The emitter resistor value has to be:

$$R_e = \frac{V_e - V_-}{I_e} = \frac{5.15 + 8}{27.4m} = 480\,\Omega \qquad \text{Equ. 7}$$

This minimal value could be experimentally increased (current decreased) until a noticeably slower fall time is reached.
If it is chosen not to implement a buffer in trade of slower transition times, this feedback pin can be connected directly to the TDA4885 output pin.

Note: If the emitter of this buffer is fed back to the TDA4885 and is connected to a negative supply (via a resistor), this may cause a latch-up situation. Therefore, the feedback pin must be set to > 300mV during start-up. This is achieved by a divider from +8 V (resistors R*24/R*11) to the buffer's emitter, which sets the feedback pin to about 1 V during start-up.

5.4 Black Level Control

Black level (at the cathodes) control is achieved by a clamp diode DC-restore circuit. The clamp diode restores the cathode voltage to a defined black level during the clamp pulse. The defined black level is created by Three DC-amplifiers, driven by the external reference voltages V_{ref} of the TDA4885. A range of 50 V-75 V is chosen, because the lowest level may not be negative during video, but the level should also be as low as possible, in order to allow Vg1 to be as little negative as possible. The three DC-amplifiers (T*02, where '*' stands for channel 1, 2 or 3) receive a temperature-compensated voltage at their emitters. The transistors are connected in a feedback circuit, in which ΔV_{ref} is approximately amplified by $R_{fb}\backslash R_{in}$ = R*20\R*21 = 91k\5k6 = 16 times. The output voltage range must cover the maximum cut-off voltage difference of the cathodes, which is 25 V for 17" tubes. Cathode voltage will be 8-10 V lower, because the emitter voltage of T*02 is set at 8-10 V. The resistors R*19 at the collector are applied to limit the collector-emitter voltage of T*02.

5.5 Speed-up

In order to achieve the best possible rise and fall times, a speed-up circuit has to be applied over R_{in} of the CR6927. The input circuit consists of two series RC-combinations. The value of R_{in} is divided in a large and small part. Speed-up capacitors C*03 and C*04 speed up the slope of the CR6927 output signal by increasing the high-frequency gain. Start values for C*03/C*04 can be calculated by first measuring the CR6927 output time constant ($\tau_o \approx$ 20-25 ns), this is done by only connecting a resistor as input network. The time constant, created by C*03 * R*09 and C*04 * R*10 must then be made equal to this value (where $\tau_o^2 \approx \{(C*03*R*09)^2 + (C*04*R*10)^2\}$).
Mostly, the created time constant(s) must be decreased in order to limit overshoot. The optimized values for this application are:
- R*09/C*03 = 270E/68pF;
- R*10/C*04 = 56E/82pF.

Note: The calculations above are just a guideline and optimal values are obtained experimentally.

5.6 Accu Colour

With Accu Colour, white colour temperature is adjustable. This colour temperature is adjustable by the gain setting of the three R/G/B channels. The TDA4885 has individual gain control with a range of 7 dB. This is needed for three functions:

1- Absolute sensitivity channels: proportion beam current that is necessary for the separate R/G/B guns in order to achieve white with a certain colour temperature.
2- Spread sensitivity channels: spread on the absolute sensitivity mentioned above.
3- Accu Colour.

The first function could be implemented in hardware by applying different input resistors at the input pins of the CR6927 three colour channels. This enables an individually adjustable gain. If the gain modulation pins are not used, gain adjustment can be applied at these pins (see paragraph 5.6 here below).

The second function of gain adjustment of the TDA4885 is the compensation for the spread on channel sensitivity. This function needs 3 dB at maximum.

The third function is Accu Colour and for this, the TDA4885 leaves a 4 dB control range. This range will be sufficient for adjusting colour temperature from, for instance, 3500 K to 7000 K or 5000 K to 10,000 K.

5.7 Gain Modulation

Some picture tubes have a relatively large decrease of light output towards the edges. By applying a dynamic waveform to the gain modulation inputs (pin 12, 13 and 14 of TDA4885), this light output decrease can be compensated. In a simple application, a parabolic waveform of horizontal frequency can be applied to the three pins simultaneously. For this, the HFOCUS signal from deflection controller TDA4855 is suitable. Only the left/right loss on the display is then compensated. In a high performance application, top/bottom losses can also be compensated by applying three separately adjustable signals from an X/Y wave form generator or a parabola generator, such as deflection controller TDA4854.

If brightness uniformity is not implemented, the gain modulation pins can be used for gain adjustment. This can be achieved by either a DC-potentiometer or an external DAC (for instance from Pulse Width Modulation output of μC). In this way, the gain adjustment DAC's of the TDA4885 are free for an enlarged Accu Colour user range.

5.8 Smearing Compensation

If the video board is applied without any compensation networks, it shows some visual smearing. Therefore, two smearing compensation networks are implemented on the board:

- An RC-series network, parallel to the input network of the CR6927, for the compensation of the TDA4885 smearing. This is a smearing that shows an undershoot (D≈7-8%) with time constant $\tau_{s,1}$≈50 ns. The value of compensation resistor R*23 is calculated in equation 8.

$$R_{*23} = \frac{100\%}{D} * R_{in} = \frac{100\%}{D} * (R*09 + R*10)$$
$$= \frac{100\%}{7.5\%} * (270 + 56) = 4k3$$

Equ. 8

The value for C*11 must be: $\tau_{s,1}$\R*23 = 50ns\4k3 = 12pF.

- An RC-series network, from output to input of the CR6927 in order to compensate its own smearing. This is an overshoot smearing (D≈2%) with time constant $\tau_{s,2}$≈15µs. The value for compensation resistor R*14 must be calculated by equation 9:

$$R*14 = \frac{100\%}{D} * R_{fb(int)}$$
$$= \frac{100\%}{2\%} * 4k3 = 220k$$

Equ. 9

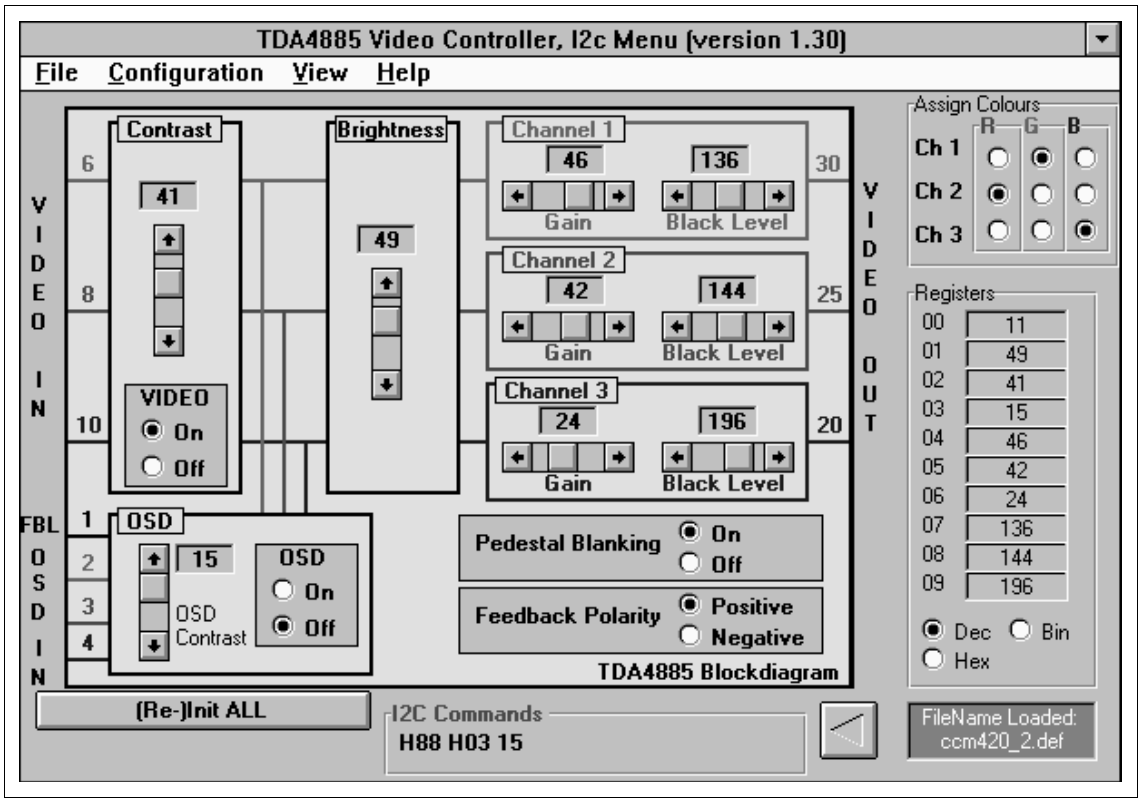
The RC-combination must match the smearing time constant:
C*07 = $\tau_{s,2}$\R*14 = 15µs\220k = 68pF.

Note: These compensation values are start values, the final values must be obtained experimentally.

6. REFERENCES

Ref. 1: Data sheet TDA4885, issued 1996 March 13.
Ref. 2: Data sheet CR6927, issued 1996 February 29.
Ref. 3: Data sheet PCB8517, issued 1995 March 7.
Ref. 4: 'PCALE 15" Autosync Monitor Mk2 circuit description' by Han Misdom. Report number AN95086.0, issued 1995 September 5.
Ref. 5: Data sheet 17" tube, data handbook DC01: 'Colour TV Picture Tubes and Assemblies', issued 1994 October.

APPENDIX 1: I²C CONTROL SOFTWARE



Note: Contrary to the example above, feedback polarity should be set 'Positive' for the application, described in this report.

APPENDIX 2a: INTERNAL BLOCK DIAGRAM TDA4885 (left side)

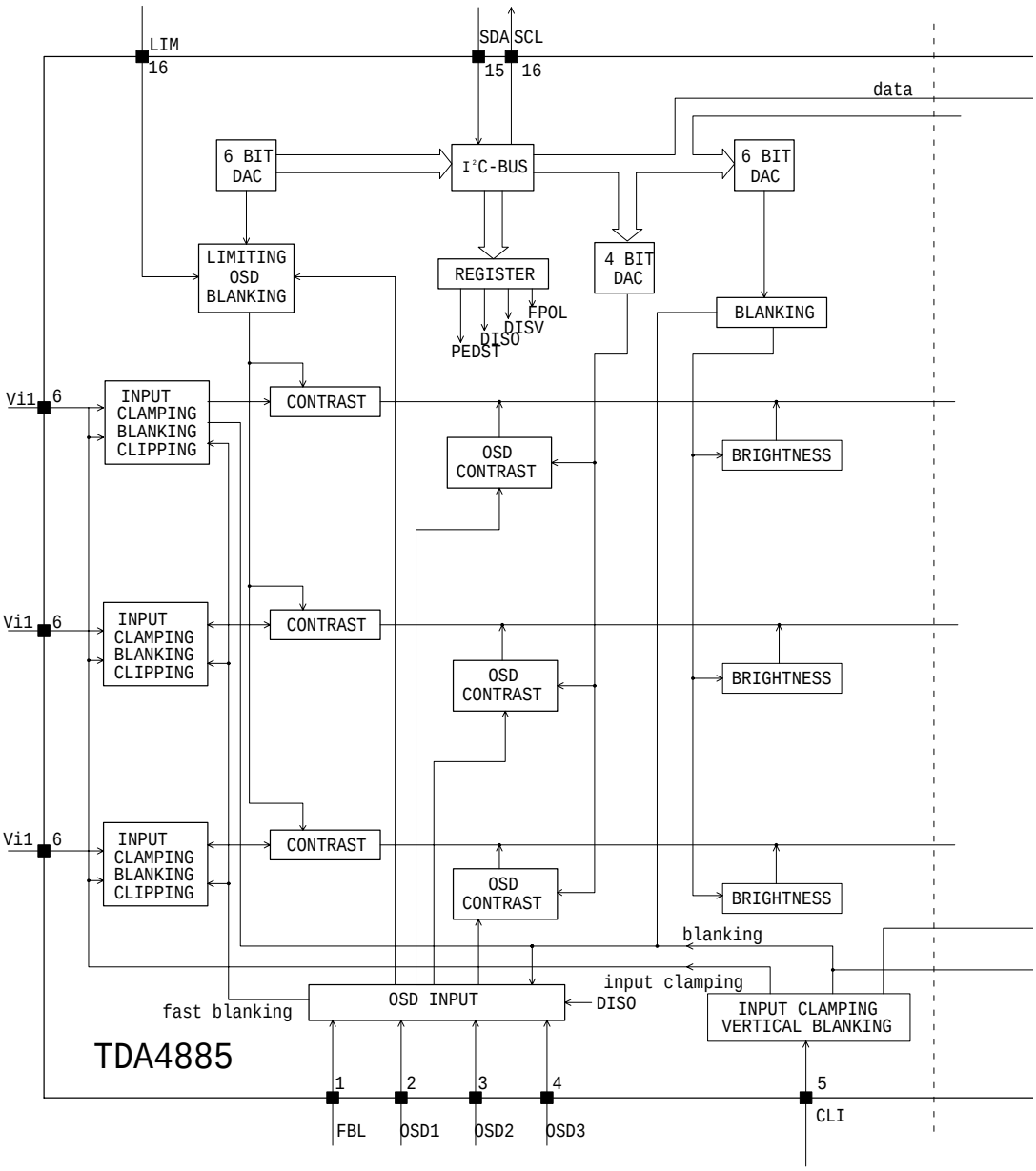


Fig.10 Internal Block Diagram TDA4885 (left side)

APPENDIX 2b: INTERNAL BLOCK DIAGRAM TDA4885 (right side)

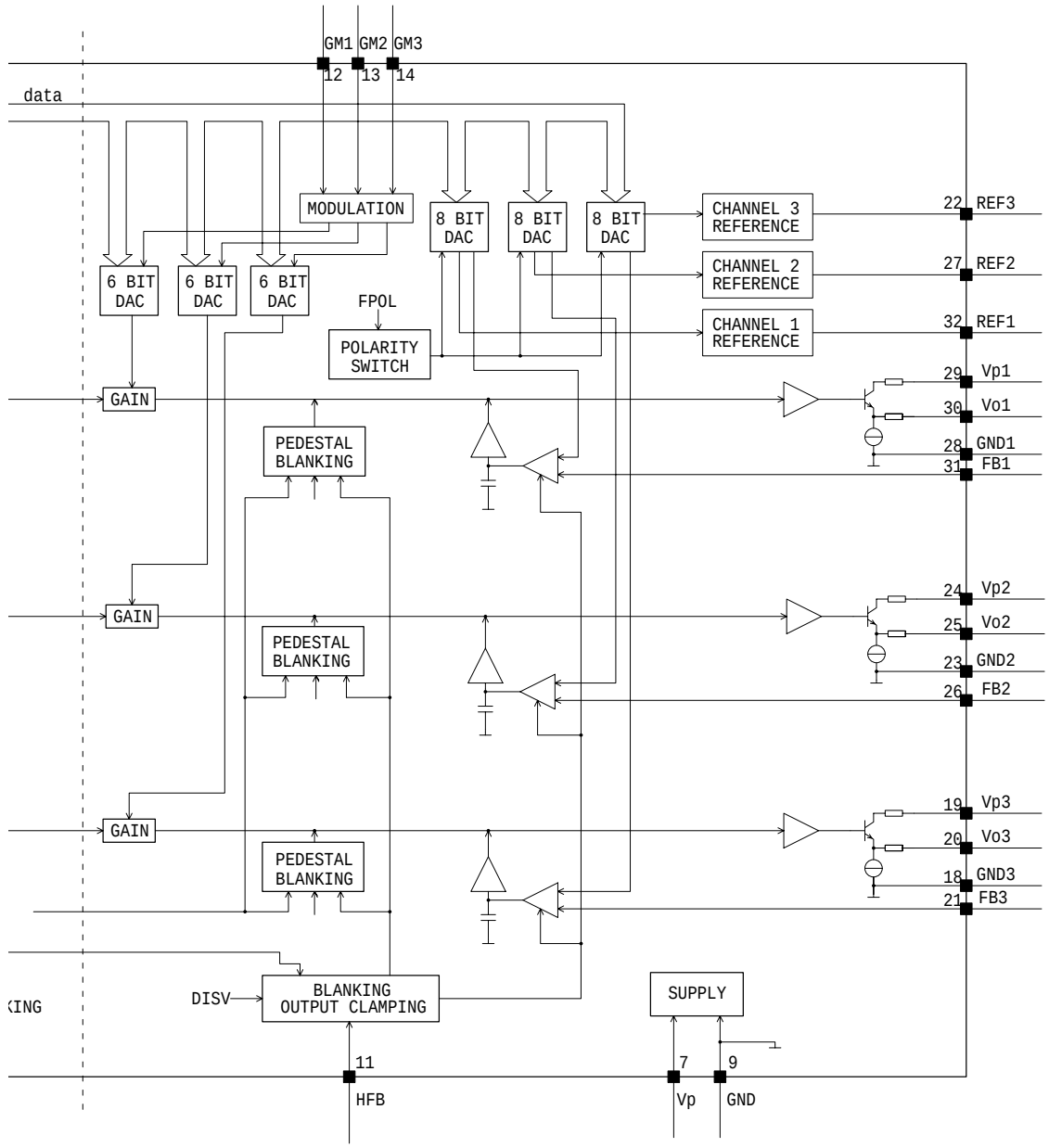
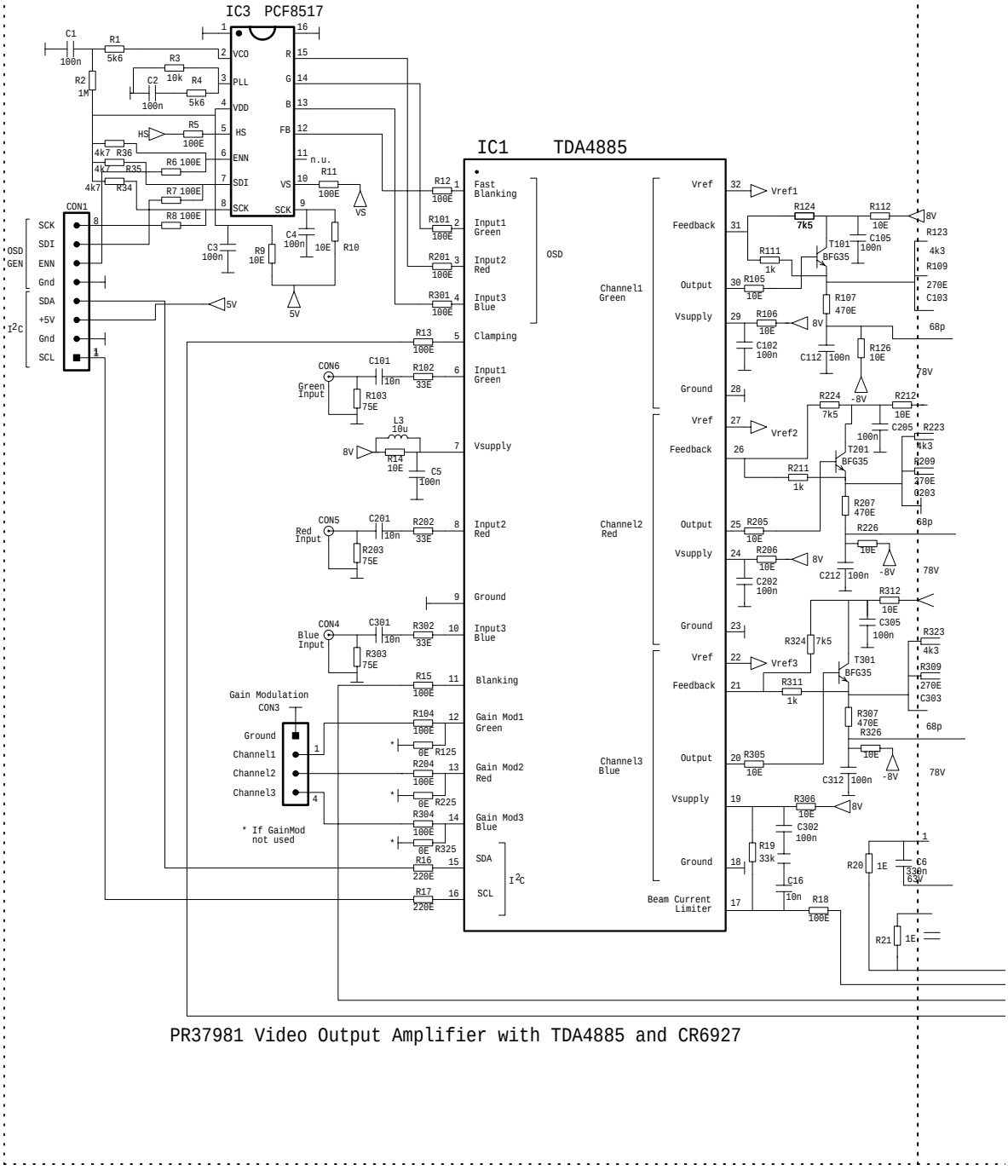


Fig.11 Internal Block Diagram TDA4885 (right side)

APPENDIX 3a: SCHEMATICS SYSTEM (left side)



PR37981 Video Output Amplifier with TDA4885 and CR6927

Fig.12 System Schematics (left side)

APPENDIX 3b: SCHEMATICS SYSTEM (right side)

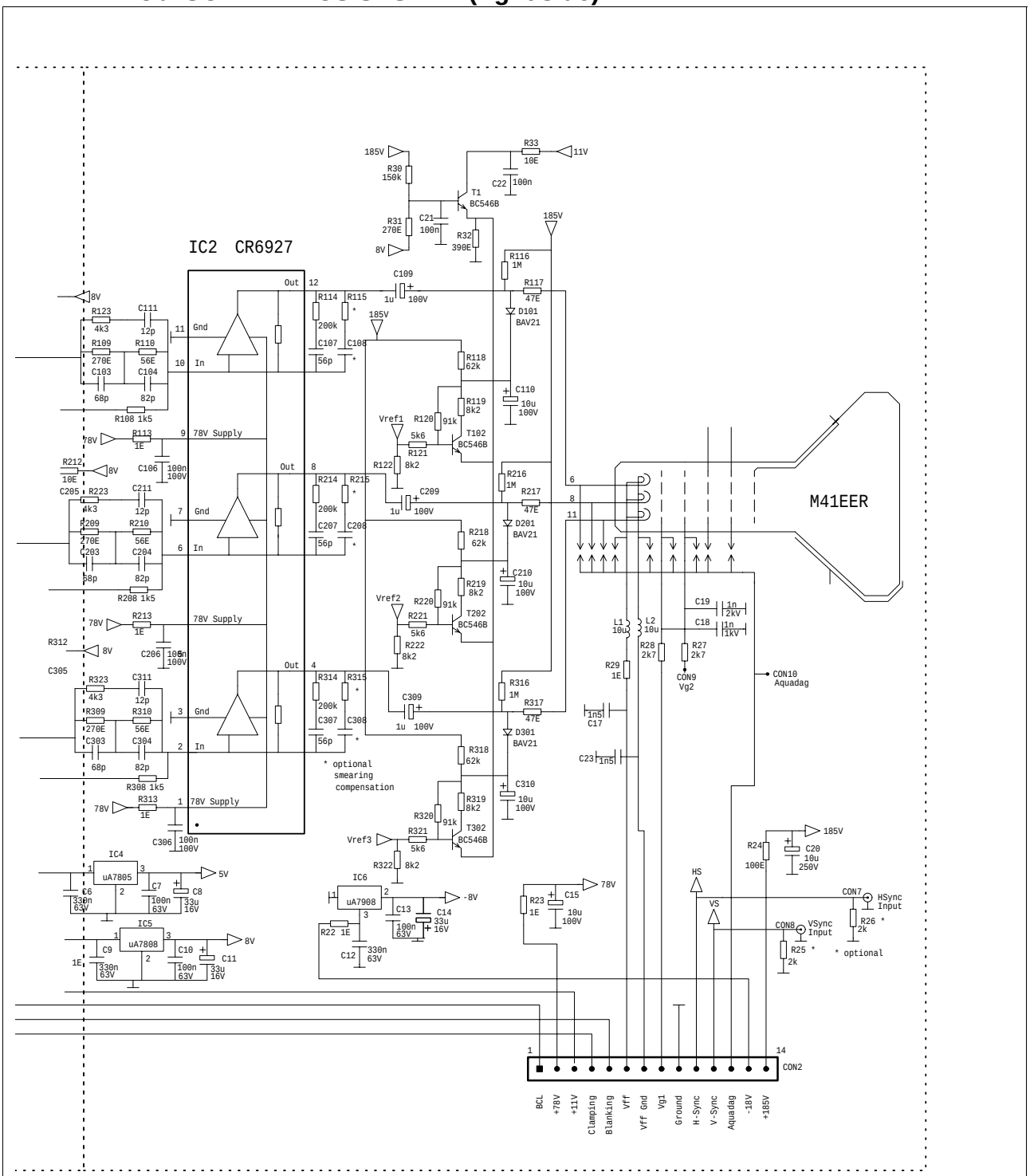


Fig.13 System Schematics (right side)

APPENDIX 4: MONITOR ALIGNMENT PROCEDURE

The cut-off voltage of the three R/G/B guns is different and the monitor must be aligned to compensate for this voltage difference. Most of the following alignment procedure can be done by the TDA4885 software, except Vg2. It is specified for a video board with AC-coupling to the cathodes. Figure 15 clarifies what the several adjustments do to the cathode voltages.

- Set Vg2 to minimum, so that the three CRT cut-off levels are too low;
- Set the three black level DAC's at maximum with positive feedback and with pedestal blanking (DAC=FF, FPOL=1, PEDST=1). Check: $V_{cath} \approx 75$ V.
- Set Contrast and Brightness to nominal values (Contrast: 26hex, Brightness: 10hex);
- Apply video signal test pattern and disable video (DISV=1). The output will be at reference black;
- Increase Vg2 slowly until one colour becomes just visible;
- Decrease cathode voltage of remaining colours by decreasing the corresponding black level DAC until these colours also become just visible;
- Enable video (DISV=0);
- Adjust the three gain DAC's until the desired white point (colour temperature) luminance is obtained.

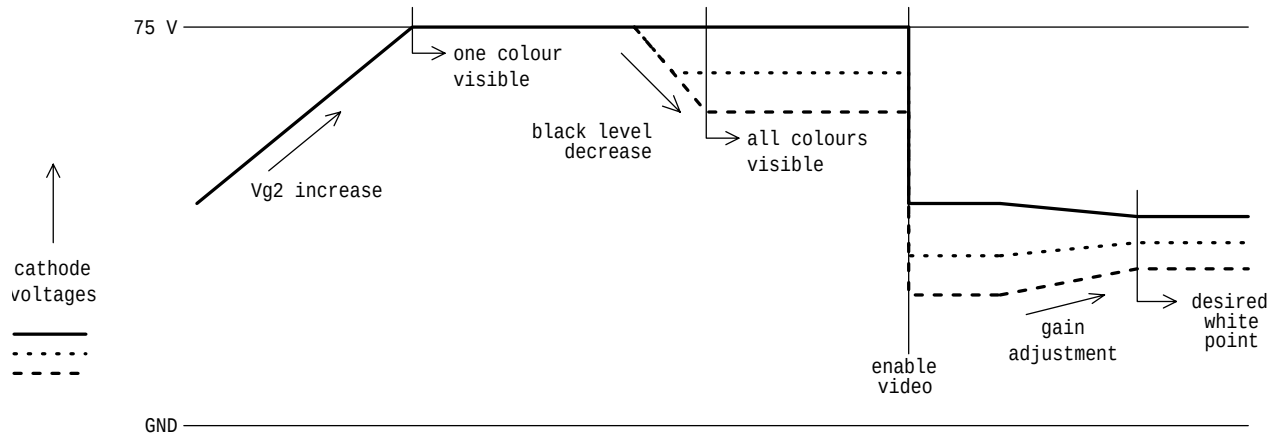


Fig.14 Monitor Alignment.

APPENDIX 5: CALCULATIONS FLASH RESISTOR

Purpose of the flash resistor from coupling capacitor to cathode is to limit flash diode current when a flash occurs without limiting the video bandwidth of the system. Maximum non-repetitive diode current (BAV21) is 1 A for a pulse ≤ 1 s and 5 A for a pulse ≤ 1 µs. If a flash occurs, it is led away from the video stage by the spark-gap and flash diode to the DC-amplifier elcap. The RC-filter that is formed by the flash resistor and the load capacitance (tube) is the limiting factor. Assuming a video bandwidth of 100 MHz, the cross-over frequency of the RC-filter must by larger than 300 MHz. The influence of the RC-filter is then limited to 5%. Load capacitance is about 9 pF (see equation 4), which yields a maximum flash resistor value of:

$$R_{flash,maximum} = \frac{1}{2\pi * f * C_{load}} = \frac{1}{2\pi * 300M * 9p} = 60\,\Omega \qquad \text{Equ. 10}$$

A flashover consists of two phases:

- Before ignition of the spark-gap, a voltage of 2 kV is present for a time < 50 ns. The maximum flash resistor value of 60 Ω limits the diode current to 2 kV\60 Ω ≈ 30 A. This is clearly more then the specified maximum of 5 A. In practice, the inductance of wires and print tracks limits the diode current to less than 30 A and the BAV21 can withstand this very short pulse.
- After ignition of the spark-gap, a voltage of 150 V is present for a time < 1 µs. Now, a current from the voltage of 150 V - 50 V (minimum elcap voltage) = 100 V must be limited to ≤ 5 A. This means the flash resistor must have a minimum value of 100 \ 5 = 20 Ω. A value of 47 Ω is chosen (safety margin).

APPENDIX 6a: LAY-OUT PRINTED CIRCUIT BOARD (component side)

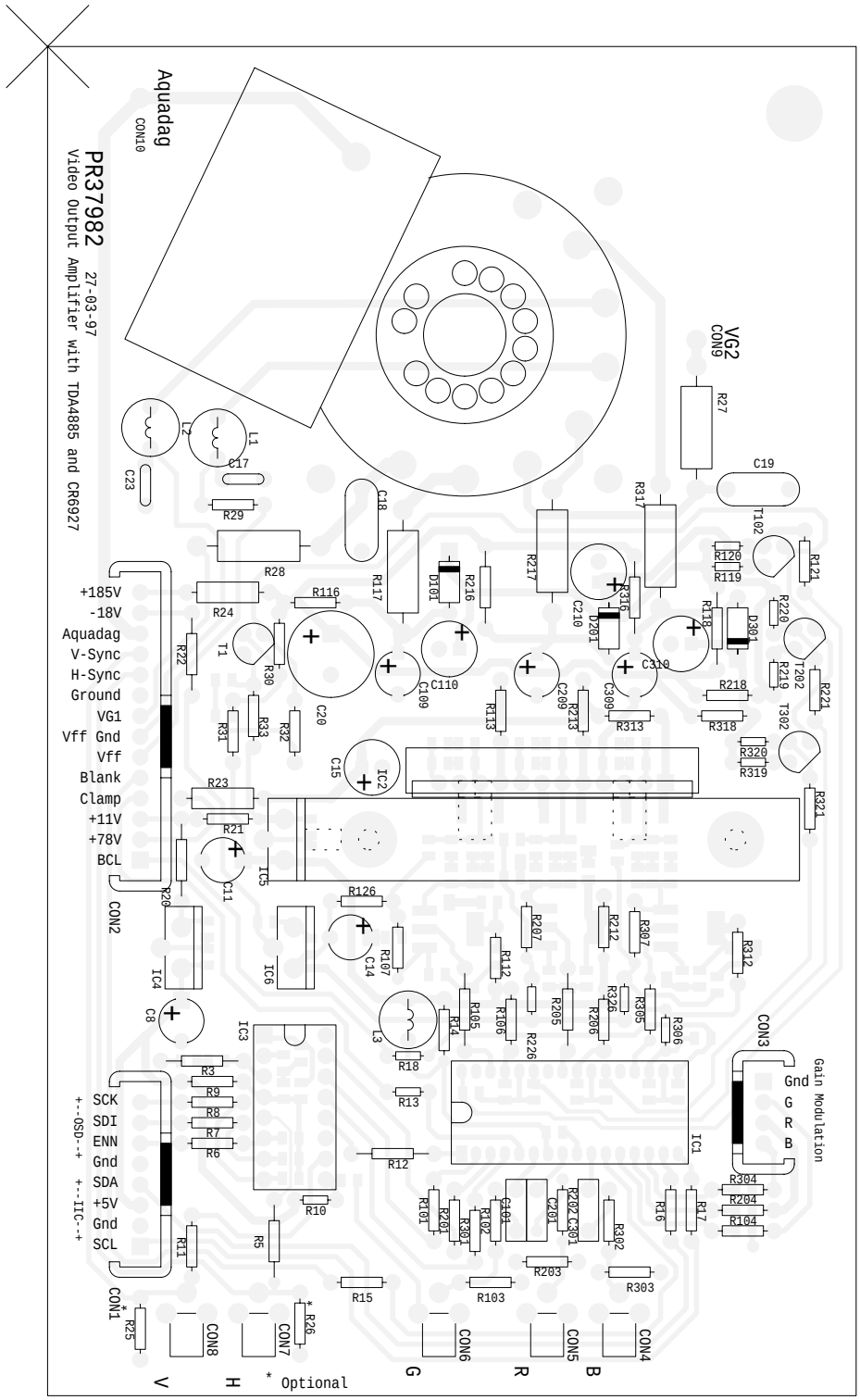


Fig.15 PCB Lay-out and Component Placement Component Side

APPENDIX 6b: LAY-OUT PRINTED CIRCUIT BOARD (solder side)

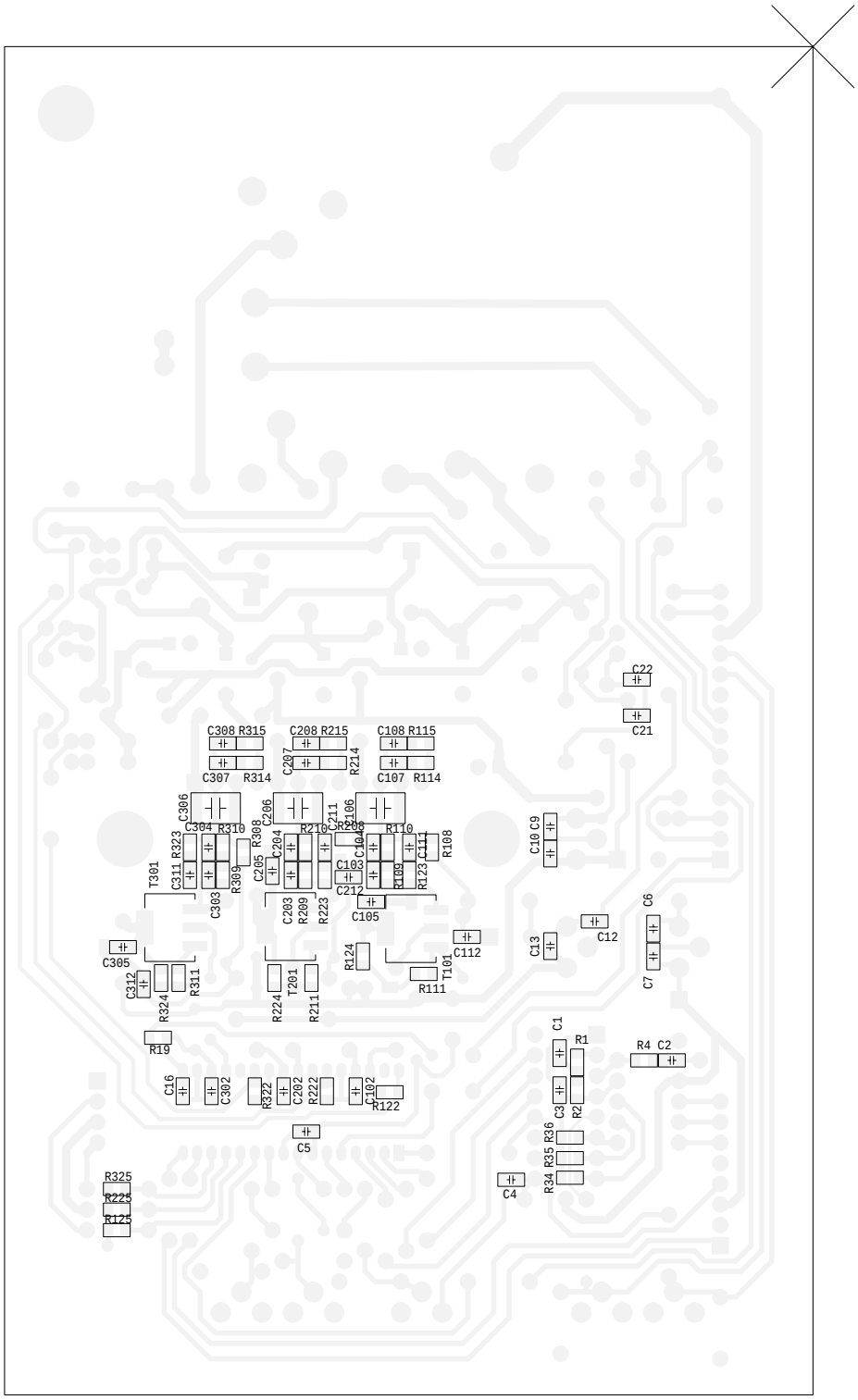


Fig.16 PCB Lay-out and Component Placement Solder Side

APPENDIX 7: COMPONENTS LIST

Nbr.	Value/Range	Type	12NC/info
R117	47E AB	AB6E	
R217	47E AB	AB6E	
R317	47E AB	AB6E	
R27	2k7 AB	AB6E	
R28	2k7 AB	AB6E	
C108	*	C0805	Not placed
C208	*	C0805	Not placed
C308	*	C0805	Not placed
C111	12p	C0805	2222-861-12129
C211	12p	C0805	2222-861-12129
C311	12p	C0805	2222-861-12129
C107	56p	C0805	2222-861-12569
C207	56p	C0805	2222-861-12569
C307	56p	C0805	2222-861-12569
C103	68p	C0805	2222-861-12689
C203	68p	C0805	2222-861-12689
C303	68p	C0805	2222-861-12689
C104	82p	C0805	2222-861-12829
C204	82p	C0805	2222-861-12829
C304	82p	C0805	2222-861-12829
C16	10n	C0805	2222-590-16627
C1	100n	C0805	2222-910-16649
C2	100n	C0805	2222-910-16649
C3	100n	C0805	2222-910-16649
C4	100n	C0805	2222-910-16649
C5	100n	C0805	2222-910-16649
C7	100n	C0805	2222-910-16649
C10	100n	C0805	2222-910-16649
C13	100n	C0805	2222-910-16649
C21	100n	C0805	2222-910-16649
C22	100n	C0805	2222-910-16649
C102	100n	C0805	2222-910-16649
C105	100n	C0805	2222-910-16649
C112	100n	C0805	2222-910-16649
C202	100n	C0805	2222-910-16649
C205	100n	C0805	2222-910-16649
C212	100n	C0805	2222-910-16649
C302	100n	C0805	2222-910-16649
C305	100n	C0805	2222-910-16649
C312	100n	C0805	2222-910-16649
C6	330n	C0805	2222-910-16656
C9	330n	C0805	2222-910-16656
C12	330n	C0805	2222-910-16656

Nbr.	Value/Range	Type	12NC/info
C106	100n 100V	C1812	2222-614-16649
C206	100n 100V	C1812	2222-614-16649
C306	100n 100V	C1812	2222-614-16649
C101	10n	C2E	2222-370-41103
C201	10n	C2E	2222-370-41103
C301	10n	C2E	2222-370-41103
C18	1n 1kV	C3EE4	
C19	1n 2kV	C3EE4	
C17	1n5	CC2E	2222-630-03152
C23	1n5	CC2E	2222-630-03152
CON4	CoaxH 75E	COAXCONH	
CON5	CoaxH 75E	COAXCONH	
CON6	CoaxH 75E	COAXCONH	
CON7	CoaxH 75E	COAXCONH	
CON8	CoaxH 75E	COAXCONH	
CON2	Stoko14	CON14	
CON3	Stoko4	CON4	
CON1	Stoko8	CON8	
*	HOSIDEN213	CRT_DAF	
IC3	PCF8517	DIL16	9352-996-00112
D101	BAV21	DO35	9331-892-10153
D201	BAV21	DO35	9331-892-10153
D301	BAV21	DO35	9331-892-10153
C15	10u 100V	E1E6	2222-300-39109
C110	10u 100V	E1E6	2222-300-39109
C210	10u 100V	E1E6	2222-300-39109
C310	10u 100V	E1E6	2222-300-39109
C20	10u 250V	E2E10	2222-044-63109
C109	1u 100V	E2E5	2222-037-59108
C209	1u 100V	E2E5	2222-037-59108
C309	1u 100V	E2E5	2222-037-59108
C8	68u 16V	E2E5	2222-030-35689
C11	68u 16V	E2E5	2222-030-35689
C14	68u 16V	E2E5	2222-030-35689
R115	*	R0805	Not Placed
R215	*	R0805	Not Placed
R315	*	R0805	Not Placed
R125	0E	R0805	Not Placed
R225	0E	R0805	Not Placed
R325	0E	R0805	Not Placed
R110	56E	R0805	2322-730-**569
R210	56E	R0805	2322-730-**569
R310	56E	R0805	2322-730-**569
R109	270E	R0805	2322-730-**271
R209	270E	R0805	2322-730-**271

Nbr.	Value/Range	Type	12NC/info
R309	270E	R0805	2322-730-**271
R111	1k	R0805	2322-730-**102
R211	1k	R0805	2322-730-**102
R311	1k	R0805	2322-730-**102
R308	1k2	R0805	2322-730-**122
R108	1k5	R0805	2322-730-**152
R208	1k5	R0805	2322-730-**152
R223	4k3	R0805	2322-730-**432
R123	4k3	R0805	2322-730-**432
R323	4k3	R0805	2322-730-**432
R34	4k7	R0805	2322-730-**472
R35	4k7	R0805	2322-730-**472
R36	4k7	R0805	2322-730-**472
R1	5k6	R0805	2322-730-**562
R4	5k6	R0805	2322-730-**562
R124	7k5	R0805	2322-730-**752
R224	7k5	R0805	2322-730-**752
R324	7k5	R0805	2322-730-**752
R122	8k2	R0805	2322-730-**822
R222	8k2	R0805	2322-730-**822
R322	8k2	R0805	2322-730-**822
R19	33k	R0805	2322-730-**333
R114	200k	R0805	2322-730-**204
R214	200k	R0805	2322-730-**204
R314	200k	R0805	2322-730-**204
R2	1M	R0805	2322-730-**105
IC1	TDA4885	SDIL32	9350-308-00112
R21	1E	SFR16	2322-180-**108
R29	1E	SFR16	2322-180-**108
R113	1E	SFR16	2322-180-**108
R213	1E	SFR16	2322-180-**108
R313	1E	SFR16	2322-180-**108
R9	10E	SFR16	2322-180-**109
R14	10E	SFR16	2322-180-**109
R33	10E	SFR16	2322-180-**109
R106	10E	SFR16	2322-180-**109
R112	10E	SFR16	2322-180-**109
R126	10E	SFR16	2322-180-**109
R206	10E	SFR16	2322-180-**109
R212	10E	SFR16	2322-180-**109
R305	10E	SFR16	2322-180-**109
R312	10E	SFR16	2322-180-**109
R102	33E	SFR16	2322-180-**339
R202	33E	SFR16	2322-180-**339
R302	33E	SFR16	2322-180-**339

Nbr.	Value/Range	Type	12NC/info	
R103	75E	SFR16	2322-180-**759	
R203	75E	SFR16	2322-180-**759	
R303	75E	SFR16	2322-180-**759	
R6	100E	SFR16	2322-180-**101	
R7	100E	SFR16	2322-180-**101	
R8	100E	SFR16	2322-180-**101	
R11	100E	SFR16	2322-180-**101	
R15	100E	SFR16	2322-180-**101	
R101	100E	SFR16	2322-180-**101	
R104	100E	SFR16	2322-180-**101	
R201	100E	SFR16	2322-180-**101	
R204	100E	SFR16	2322-180-**101	
R301	100E	SFR16	2322-180-**101	
R304	100E	SFR16	2322-180-**101	
R16	220E	SFR16	2322-180-**221	
R17	220E	SFR16	2322-180-**221	
R31	270E	SFR16	2322-180-**271	
R32	390E	SFR16	2322-180-**391	
R107	470E	SFR16	2322-180-**471	
R207	470E	SFR16	2322-180-**471	
R307	470E	SFR16	2322-180-**471	
R25	2k	SFR16	2322-180-**202	Not placed
R26	2k	SFR16	2322-180-**202	Not placed
R121	5k6	SFR16	2322-180-**562	
R221	5k6	SFR16	2322-180-**562	
R321	5k6	SFR16	2322-180-**562	
R218	62k	SFR16	2322-180-**623	
R318	62k	SFR16	2322-180-**623	
R30	150k	SFR16	2322-180-**154	
R116	1M	SFR16	2322-180-**105	
R10	10E	SFR16_2E	2322-180-**109	
R226	10E	SFR16_2E	2322-180-**109	
R306	10E	SFR16_2E	2322-180-**109	
R326	10E	SFR16_2E	2322-180-**109	
R13	100E	SFR16_2E	2322-180-**101	
R18	100E	SFR16_2E	2322-180-**101	
R119	8k2	SFR16_2E	2322-180-**822	
R219	8k2	SFR16_2E	2322-180-**822	
R319	8k2	SFR16_2E	2322-180-**822	
R120	91k	SFR16_2E	2322-180-**913	
R220	91k	SFR16_2E	2322-180-**913	
R320	91k	SFR16_2E	2322-180-**913	
R20	1E	SFR16_4E	2322-180-**108	
R22	1E	SFR16_4E	2322-180-**108	
R105	10E	SFR16_4E	2322-180-**109	

Nbr.	Value/Range	Type	12NC/info
R205	10E	SFR16_4E	2322-180-**109
R12	100E	SFR16_4E	2322-180-**101
R5	100E	SFR16_4E	2322-180-**101
R3	10k	SFR16_4E	2322-180-**103
R118	62k	SFR16_4E	2322-180-**623
R216	1M	SFR16_4E	2322-180-**105
R316	1M	SFR16_4E	2322-180-**105
R23	1E	SFR25	2322-181-**108
R24	100E	SFR25	2322-181-**101
T101	BFG35	SOT223	9339-199-10115
T201	BFG35	SOT223	9339-199-10115
T301	BFG35	SOT223	9339-199-10115
IC2	CR6927	SOT347	9340-400-20127
L1	10u	SPOEL2E	
L2	10u	SPOEL2E	
L3	10u	SPOEL2E	
IC4	uA7805	TO220	
IC5	uA7808	TO220	
IC6	uA7908	TO220	
T1	BC546B	TO92	9332-377-801**
T102	BC546B	TO92	9332-377-801**
T202	BC546B	TO92	9332-377-801**
T302	BC546B	TO92	9332-377-801**

APPENDIX 8: POWER DISSIPATION CR6927

In order to calculate the necessary heatsink size for the video module, the maximum power dissipation of the video module has to be calculated. The power dissipation of an active load amplifier can be calculated by adding static and dynamic power. Static power is dissipated in the emitter resistors, the bias resistors R1, R2 and R3 (see figure 5) and Rfb. The DC current I_{DC} is specified in its data sheet to be 30mA (V_{sup} = 78 V) for one channel. Equation 11 below calculates static power of one channel:

$$P_{stat} = I_{DC} * V_{sup} = 30m * 78 = 2.3W$$

Dynamic power is mainly dissipated in the buffer transistors and depends on output voltage swing, load and internal capacitance and switching frequency. Equation 12 defines dynamic power dissipation of one colour channel.

$$P_{dyn} = V_{pp} * C_{load,dissipating} * f_{switch} * V_{dd} * (1 - b) \quad \text{Equ. 12}$$

Where b is the blanking factor, during this part of a line time, there is no video signal. Power dissipating load capacitance is defined in equation 4 of paragraph 4.1 and internal (of buffer transistors CR6927) capacitance is 2.4 pF, adding up to: 8.95pF + 2.4pF = 11.35 pF. Maximum voltage swing is 50 V, $C_{load,dissipating}$ = 11.35 pF and f_{switch} = 100 MHz. Equation 13 specifies the maximum dynamic power for one channel:

$$P_{dyn,max}(pixel\ on/off) = 50 * 11.35p * 100M * 78 * (1 - 0.25) = 3.3W \quad \text{Equ. 13}$$

Total maximum power dissipation is the sum of static and dynamic power dissipation, yielding:
3 * (2.3+3.3) = 16.8 W.