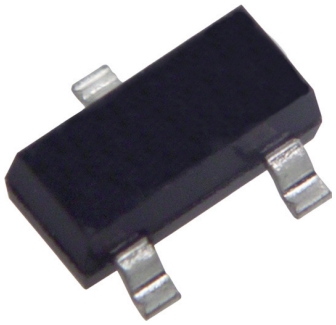
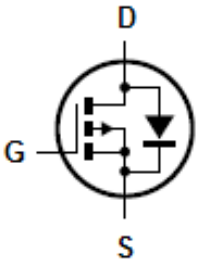
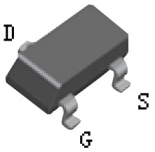
P-Channel Enhancement Mode Vertical D-MOS Transistor







SOT-23

Features:

- Voltage Controlled P-Channel Small signal switch
- High Density Cell Design for Low $R_{DS(ON)}$
- High Saturation Current

Applications:

- Line Current Interrupter in Telephone Sets
- Relay, High Speed and Line Transformer Drivers

Maximum Ratings:

Ratings at 25°C unless otherwise specified.

Parameter	Symbol	Value	Units
Drain-source voltage	V_{DS}	-50	V
Gate-source voltage	V_{GSO}	±20	V
Drain current continuous (Note 1) Pulse	I_D	-130 -520	mA
Power dissipation (Note 1)	P_D	0.36	W
Derate above 25°C		2.9	mW/°C
Thermal resistance, Junction-to-ambient	$R_{\theta JA}$	350	°C/W
Operating junction and storage temperature	T_J, T_{stg}	-55 to +150	°C
Maximum Lead Temperature For Soldering Purposes, 1/16” from case for 10 seconds	T_L	300	°C

Notes:

(1) $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.

Electrical Characteristics:

Ratings at 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250µA	-50	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	I_D = –250 µA,Referenced to 25°C	-	-48	-	mV/°C
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-1mA	-0.8	-1.7	-2	V
Gate threshold voltage temperature coefficient	$\Delta V_{GS(th)} / \Delta T_J$	I_D = –1mA, Referenced to 25°C	-	3	-	mV/°C
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS}=-50V, V_{GS}=0V	-	-	-15	µA
		V_{DS}=-50V, V_{GS}=0V T_J= 125°C	-	-	-60	µA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = -5V, I_D = -0.1A	-	1.2	10	Ω
		V_{GS} = -5V, I_D = -0.1A, T_J=125°C	-	1.9	17	
On-state drain current	$I_{D(on)}$	V_{GS}=-5V, V_{DS}=-10V	-0.6	-	-	A
Forwards transfer admittance	$\|y_{fs}\|$	V_{DS}=-25V, I_D=-0.1A	0.05	0.6	-	S
Input capacitance	C_{ISS}	V_{DS}=-25V, V_{GS}=0V, f=1MHz	-	73	-	pF
Output capacitance	C_{OSS}		-	10	-	
Reverse transfer capacitance	C_{RSS}		-	5	-	
Gate resistance	R_G	V_{GS}=-15mV, f=1MHz	-	9	-	Ω
Turn-on delay time	$t_{D(ON)}$	V_{DD}=-30V, I_D=-0.27A, V_{GS}=-10V, R_{GEN}=6Ω	-	2.5	5	ns
Turn-on rise time	t_r		-	6.3	13	
Turn-off delay time	$t_{D(OFF)}$		-	10	20	
Turn-off fall time	t_f		-	4.8	9.6	
Total gate charge	Q_g	V_{DS}=-25V, I_D=-0.1A, V_{GS}=-5 V	-	0.9	1.3	nC
Gate-source charge	Q_{gs}		-	0.2	-	
Gate-drain charge	Q_{gd}		-	0.3	-	
Maximum continuous drain-source diode forward current	I_S	-	-	-	-0.13	A
Drain-source diode forward voltage	V_{SD}	V_{GS}=0V, I_S=-0.26A (Note 2)	-	-0.8	-1.4	V
Diode reverse recovery time	t_{rr}	I_F=-0.1A di_F/dt =100A/µs (Note 2)	-	10	-	nS
Diode reverse recovery charge	Q_{rr}	-	-	3	-	nC

Notes:

(2) Pulse Test: Pulse Width ð300us, Duty Cycle ≤2%.

Typical Characteristics:

T_A = 25°C unless otherwise specified

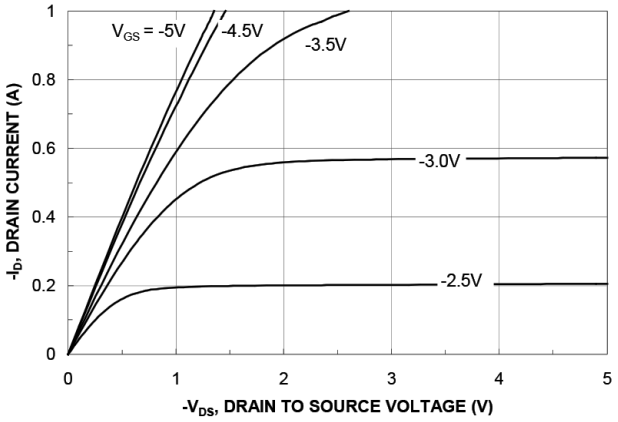


Figure 1. On-Region Characteristics.

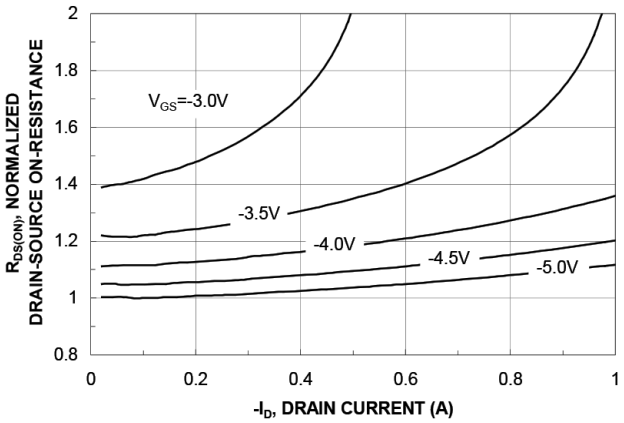


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

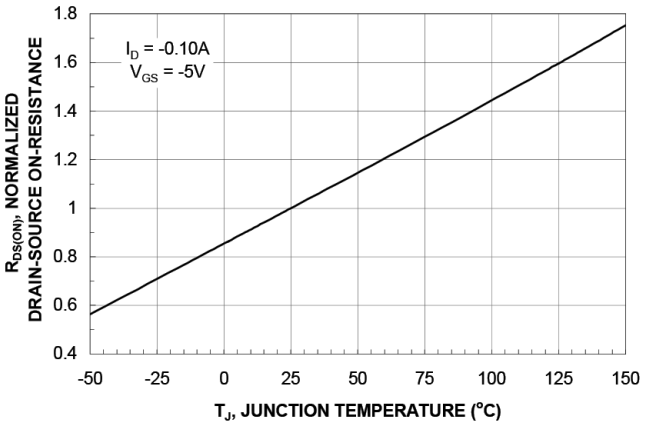


Figure 3. On-Resistance Variation with Temperature.

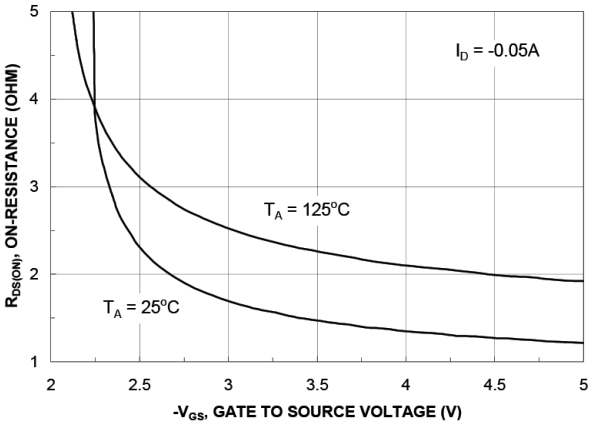


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

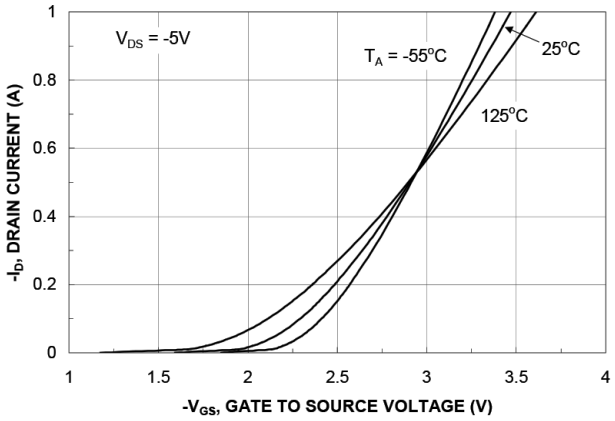


Figure 5. Transfer Characteristics.

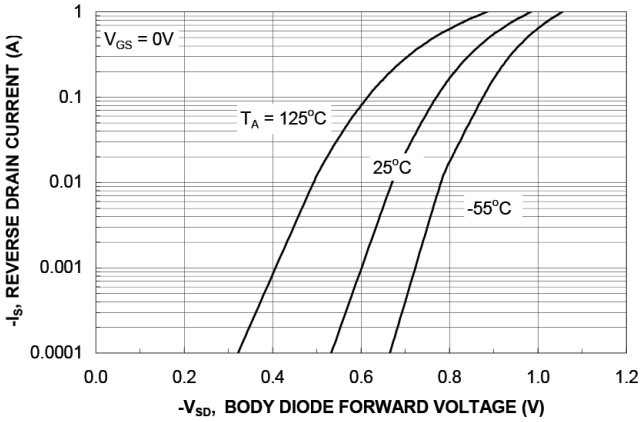


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

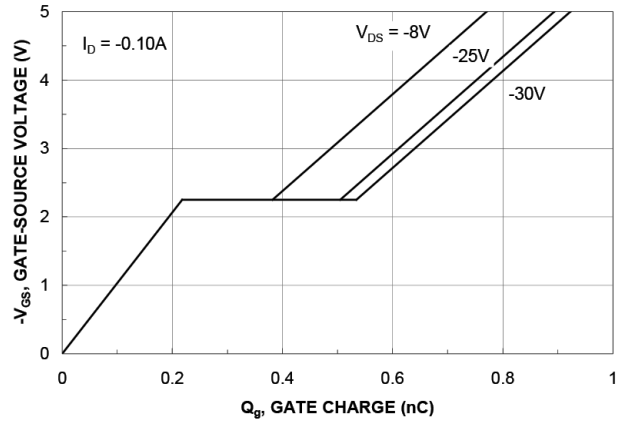


Figure 7. Gate Charge Characteristics.

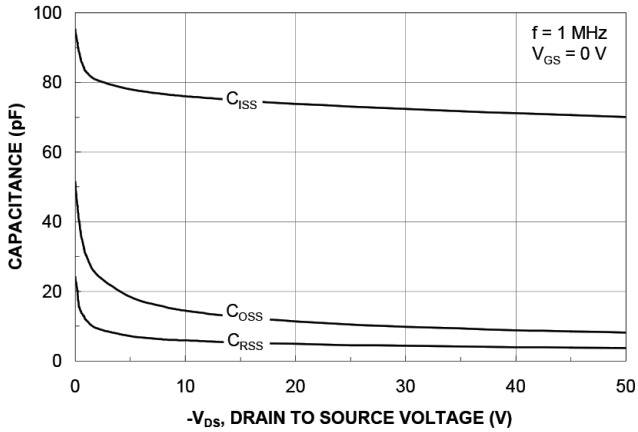


Figure 8. Capacitance Characteristics.

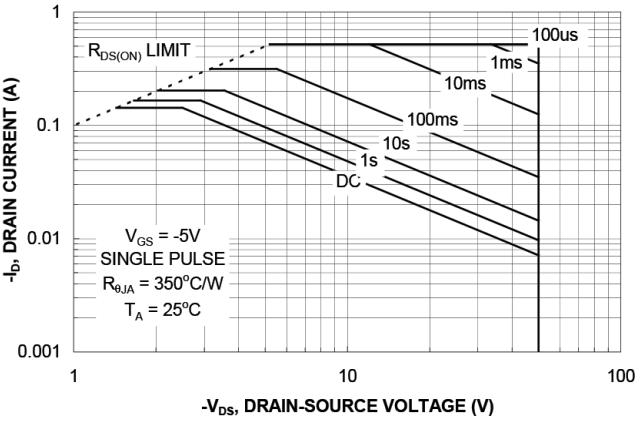


Figure 9. Maximum Safe Operating Area.

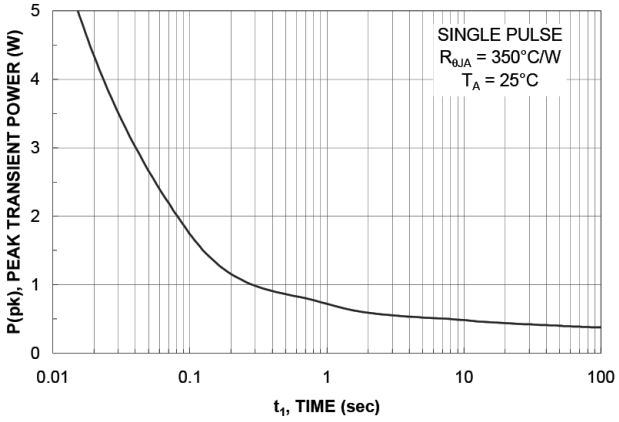


Figure 10. Single Pulse Maximum Power Dissipation.

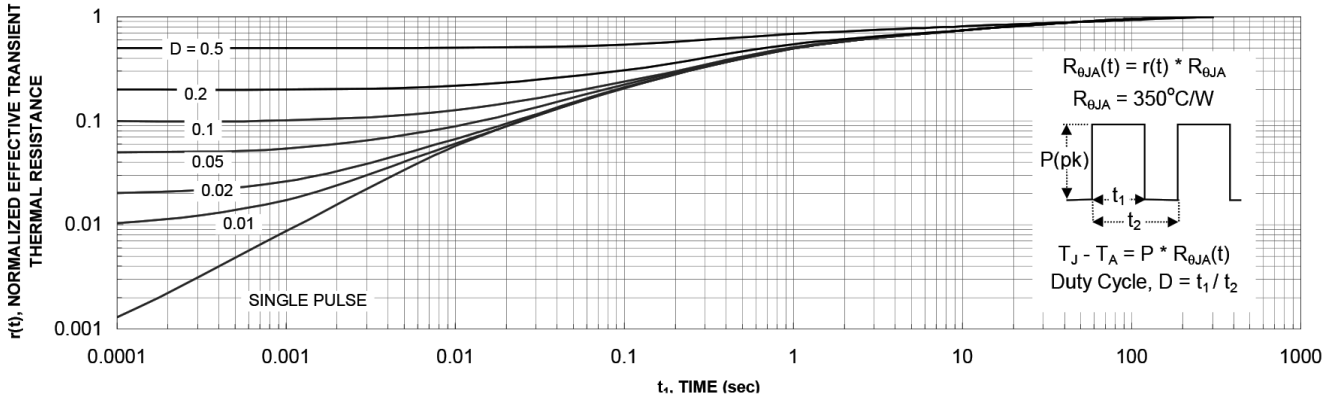


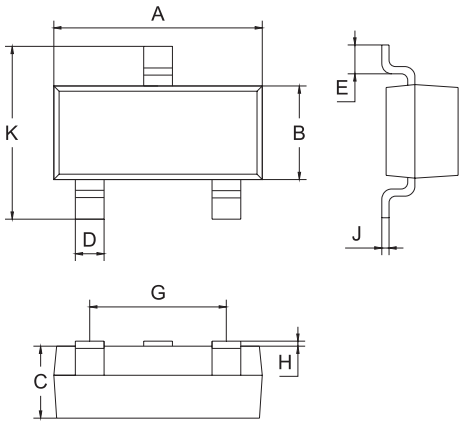
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a.
Transient thermal response will change depending on the circuit board design.

P-Channel Enhancement Mode Vertical D-MOS Transistor

Package Outline:

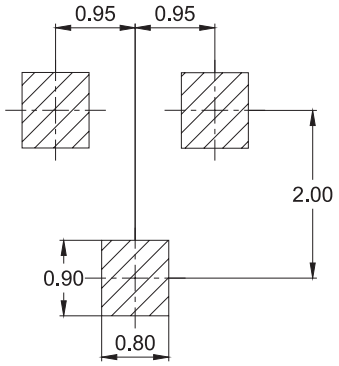
Plastic surface mounted package



SOT-23		
Dim.	**Min.**	**Max.**
A	2.7	3.1
B	1.1	1.5
C	1 Typ.	
D	0.4 Typ.	
E	0.35	0.48
G	1.8	2
H	0.02	0.1
J	0.1 Typ.	
K	2.2	2.6

Dimensions : Millimetres

Soldering Footprint:



Dimensions : Millimetres

Package Information:

Device	Package	Shipping
BSS84-7-F	SOT-23	3,000 / Tape & Reel

Part Number Table

Description	Part Number
P-Channel Enhancement Mode Vertical D-MOS Transistor	BSS84-7-F