

Table 2. Operating Modes

\overline{E}^1	\overline{G}^1	\overline{W}^1	\overline{LB}^1	\overline{UB}^1	Mode	V_{DD} Current	DQL[7:0] ²	DQU[15:8] ²
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper byte read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower byte write	I_{DDW}	D_{In}	Hi-Z
L	X	L	H	L	Upper byte write	I_{DDW}	Hi-Z	D_{In}
L	X	L	L	L	Word write	I_{DDW}	D_{In}	D_{In}

NOTES:

¹ H = high, L = low, X = don't care² Hi-Z = high impedance

Electrical Specifications

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 3. Absolute Maximum Ratings¹

Parameter	Symbol	Value	Unit
Supply voltage ²	V_{DD}	-0.5 to 4.0	V
Voltage on any pin ²	V_{In}	-0.5 to $V_{DD} + 0.5$	V
Output current per pin	I_{Out}	± 20	mA
Package power dissipation ³	P_D	0.600	W
Temperature under bias MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	T_{Bias}	-10 to 85 -10 to 85 -45 to 95 -45 to 110	°C
Storage temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	H_{max_write}	15 25 25 25	Oe
Maximum magnetic field during read or standby	H_{max_read}	100	Oe

NOTES:

- ¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
- ² All voltages are referenced to V_{SS} .
- ³ Power dissipation capability depends on package characteristics and use environment.

Electrical Specifications

Direct Current (dc)

Table 5. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{kg(I)}$	—	—	± 1	μA
Output leakage current	$I_{kg(O)}$	—	—	± 1	μA
Output low voltage ($I_{OL} = +4 \text{ mA}$) ($I_{OL} = +100 \mu\text{A}$)	V_{OL}	—	—	0.4 $V_{SS} + 0.2$	V
Output high voltage ($I_{OH} = -4 \text{ mA}$) ($I_{OH} = -100 \text{ mA}$)	V_{OH}	2.4 $V_{DD} - 0.2$	—	—	V

Table 6. Power Supply Characteristics

Parameter	Symbol	Typ	Max	Unit
ac active supply current — read modes ¹ ($I_{Out} = 0 \text{ mA}$, $V_{DD} = \text{max}$)	I_{DDR}	55	80	mA
ac active supply current — write modes ¹ ($V_{DD} = \text{max}$) MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	I_{DDW}	105 105 105 105	155 155 165 165	mA
ac standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) (no other restrictions on other inputs)	I_{SB1}	18	28	mA
CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$)	I_{SB2}	9	12	mA

NOTES:

¹ All active current measurements are measured with one address transition per cycle.

Table 7. Capacitance¹

Parameter	Symbol	Typ	Max	Unit
Address input capacitance	C_{In}	—	6	pF
Control input capacitance	C_{In}	—	6	pF
Input/output capacitance	$C_{I/O}$	—	8	pF

NOTES:

¹ $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 8. ac Measurement Conditions

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B

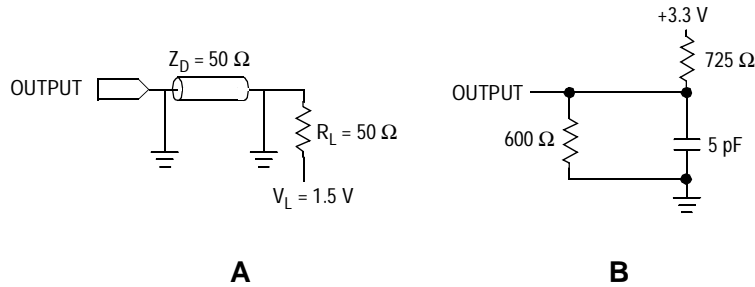


Figure 3. Output Load for ac Test

Timing Specifications

Read Mode

Table 9. Read Cycle Timing^{1, 2}

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	—	ns
Address access time	t_{AVQV}	—	35	ns
Enable access time ³	t_{ELQV}	—	35	ns
Output enable access time	t_{GLQV}	—	15	ns
Byte enable access time	t_{BLQV}	—	15	ns
Output hold from address change	t_{AXQX}	3	—	ns
Enable low to output active ^{4, 5}	t_{ELQX}	3	—	ns
Output enable low to output active ^{4, 5}	t_{GLQX}	0	—	ns
Byte enable low to output active ^{4, 5}	t_{BLQX}	0	—	ns
Enable high to output Hi-Z ^{4, 5}	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z ^{4, 5}	t_{GHQZ}	0	10	ns
Byte high to output Hi-Z ^{4, 5}	t_{BHQZ}	0	10	ns

NOTES:

- ¹ \bar{W} is high for read cycle.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ Addresses valid before or at the same time \bar{E} goes low.
- ⁴ This parameter is sampled and not 100% tested.
- ⁵ Transition is measured ± 200 mV from steady-state voltage.

Write Mode

Table 10. Write Cycle Timing 1 (\overline{W} Controlled)^{1, 2, 3, 4, 5}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁶	t_{AVAV}	35	—	ns
Address set-up time	t_{AVWL}	0	—	ns
Address valid to end of write (\overline{G} high)	t_{AVWH}	18	—	ns
Address valid to end of write (\overline{G} low)	t_{AVWH}	20	—	ns
Write pulse width (\overline{G} high)	t_{WLWH} t_{WLEH}	15	—	ns
Write pulse width (\overline{G} low)	t_{WLWH} t_{WLEH}	15	—	ns
Data valid to end of write	t_{DVWH}	10	—	ns
Data hold time	t_{WHDX}	0	—	ns
Write low to data Hi-Z ^{7, 8, 9}	t_{WLQZ}	0	12	ns
Write high to output active ^{7, 8, 9}	t_{WHQX}	3	—	ns
Write recovery time	t_{WHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of \overline{E} low and \overline{W} low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁴ After \overline{W} , \overline{E} , or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁶ All write cycle timings are referenced from the last valid address to the first transition address.
- ⁷ This parameter is sampled and not 100% tested.
- ⁸ Transition is measured ± 200 mV from steady-state voltage.
- ⁹ At any given voltage or temperature, t_{WLQZ} max < t_{WHQX} min.

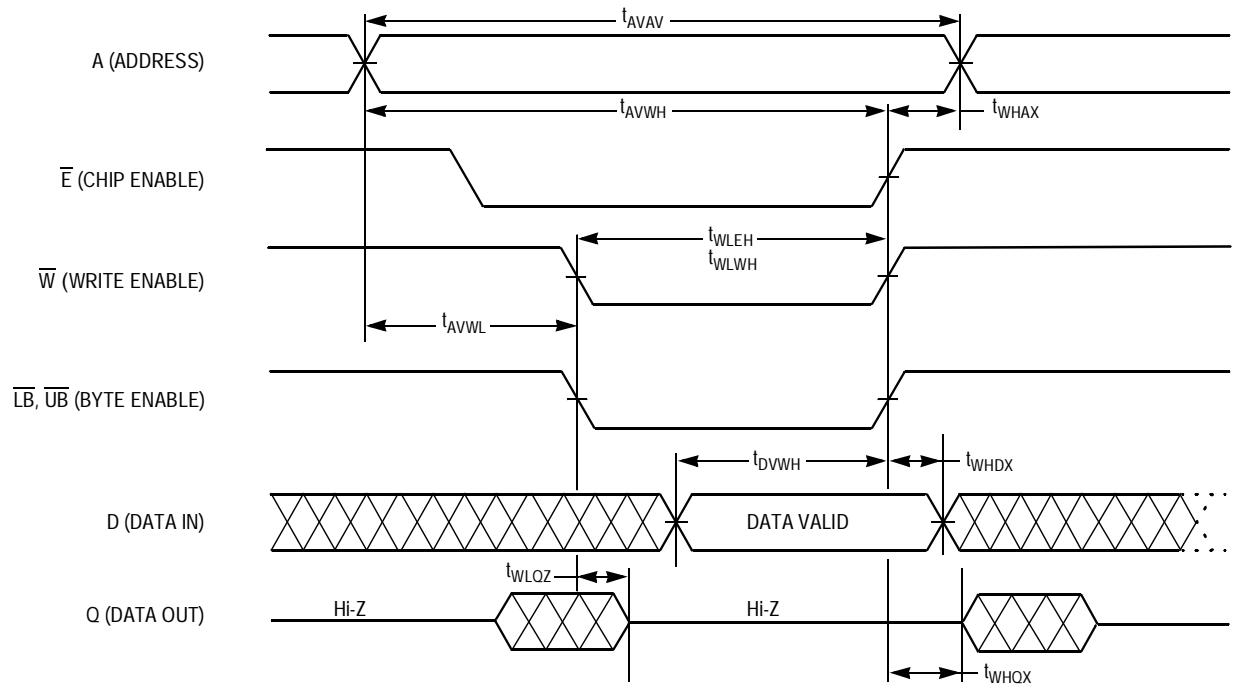


Figure 6. Write Cycle 1 (\overline{W} Controlled)

Table 11. Write Cycle Timing 2 (\overline{E} Controlled)^{1, 2, 3, 4, 5}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁶	t_{AVAV}	35	—	ns
Address set-up time	t_{AVEL}	0	—	ns
Address valid to end of write (\overline{G} high)	t_{AVEH}	18	—	ns
Address valid to end of write (\overline{G} low)	t_{AVEH}	20	—	ns
Enable to end of write (\overline{G} high)	t_{ELEH} t_{ELWH}	15	—	ns
Enable to end of write (\overline{G} low) ^{7, 8}	t_{ELEH} t_{ELWH}	15	—	ns
Data valid to end of write	t_{DVEH}	10	—	ns
Data hold time	t_{EHDX}	0	—	ns
Write recovery time	t_{EHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of \overline{E} low and \overline{W} low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁴ After \overline{W} , \overline{E} , or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁶ All write cycle timings are referenced from the last valid address to the first transition address.
- ⁷ If \overline{E} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁸ If \overline{E} goes high at the same time or before \overline{W} goes high, the output will remain in a high-impedance state.

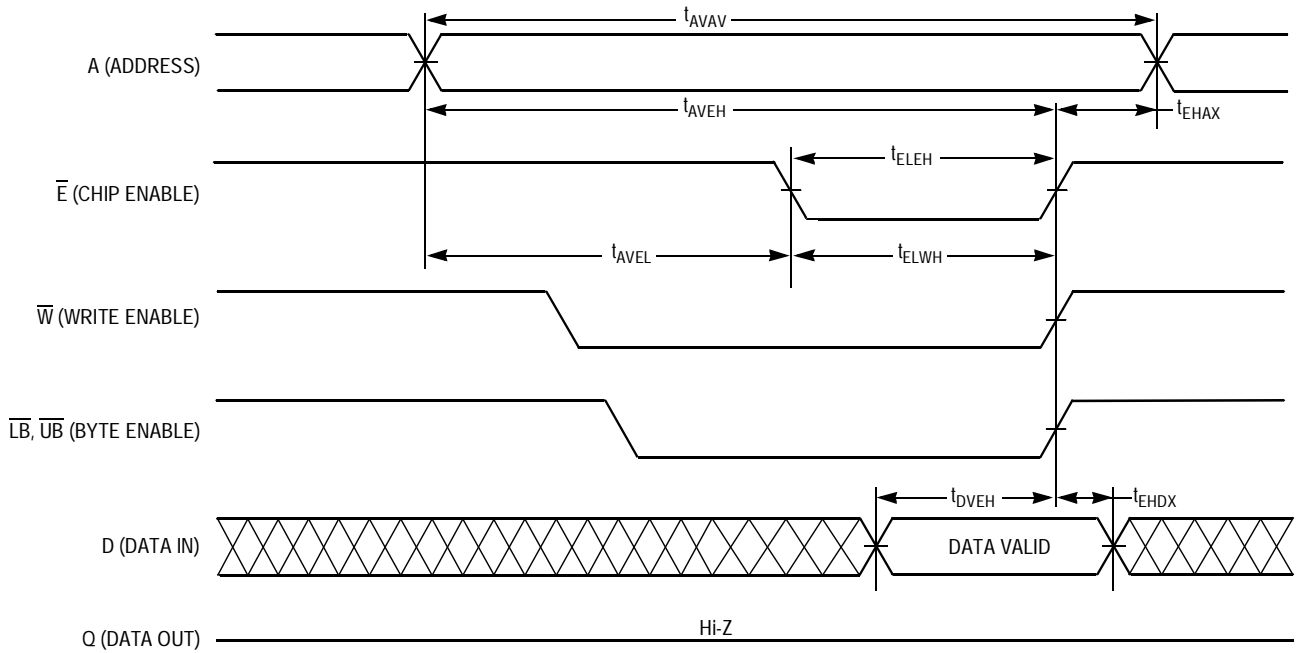


Figure 7. Write Cycle 2 (\bar{E} Controlled)

Table 12. Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled)^{1, 2, 3, 4, 5, 6}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁷	t_{AVAV}	35	—	ns
Address set-up time	t_{AVBL}	0	—	ns
Address valid to end of write ($\overline{\text{G}}$ high)	t_{AVBH}	18	—	ns
Address valid to end of write ($\overline{\text{G}}$ low)	t_{AVBH}	20	—	ns
Byte pulse width ($\overline{\text{G}}$ high)	t_{BLEH} t_{BLWH}	15	—	ns
Byte pulse width ($\overline{\text{G}}$ low)	t_{BLEH} t_{BLWH}	15	—	ns
Data valid to end of write	t_{DVBH}	10	—	ns
Data hold time	t_{BHDX}	0	—	ns
Write recovery time	t_{BHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high-impedance state.
- ⁴ After $\overline{\text{W}}$, $\overline{\text{E}}$, or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
- ⁶ The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁷ All write cycle timings are referenced from the last valid address to the first transition address.

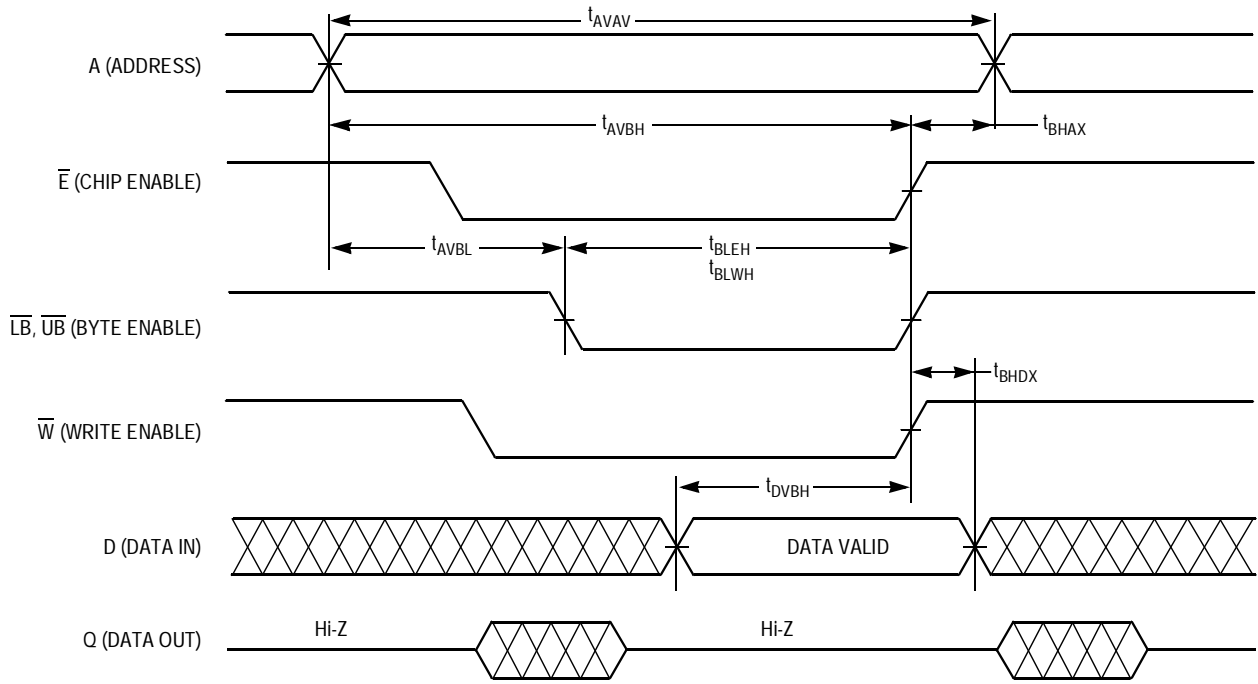


Figure 8. Write Cycle 3 ($\overline{LB}/\overline{UB}$ Controlled)

Ordering Information

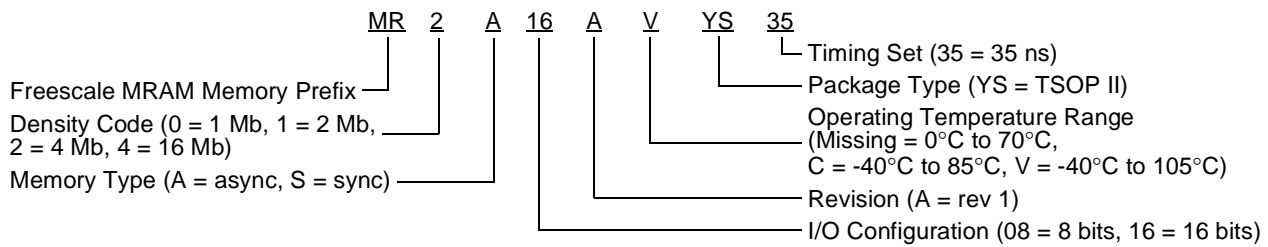
This product is available in Commercial, Industrial, and Extended temperature versions.

Freescale's semiconductor products can be classified into the following tiers: "Commercial", "Industrial" and "Extended." A product should only be used in applications appropriate to its tier as shown below. For questions, please contact a Freescale sales representative.

- **Commercial** — Typically 5 year applications - personal computers, PDA's, portable telecom products, consumer electronics, etc.
- **Industrial, Extended** — Typically 10 year applications - installed telecom equipment, workstations, servers, etc. These products can also be used in Commercial applications.

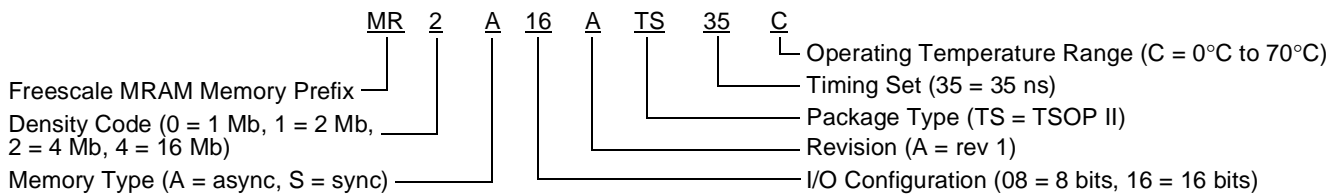
Current Part Numbering System (New Commercial, Industrial and Extended devices)

(Order by Full Part Number)



Legacy Part Numbering System (Legacy Commercial devices)

(Order by Full Part Number)



Package Information

Table 13. Package Information

Device	Pin Count	Package Type	Designator	Case No.	Document No.	RoHS Compliant
MR2A16A	44	TSOP Type II	TS/YS ¹	924A-02	98ASS23673W	True

NOTES:

¹ TS and YS are both valid package codes for TSOP packages. The package is identical for both TS and YS codes.

Revision History

Revision History

Revision	Date	Description of Change
4	18 Jun 2007	Added new Industrial and Extended temperature product information; updated part ordering information; changed to 2 ms delay after power up; power supply characteristics values updated to TBD for industrial and extended temperature devices.
5	21 Sep 2007	Changed MR2A16ATS35C product description to Legacy Commercial. Added the New Commercial temperature product (MR2A16AYS35) information. Table 3: MR2A16AYS35 H _{max_write} = 25 Oe. Table 4: MR2A16AYS35 has a 2 ms power up waiting period. Table 6: Applied values to TBD's in IDD specifications.
6	12 Nov 2007	Table 2: Changed IDDA to IDDR or IDDW. Table 13: Added note indicating that TS and YS are both valid package codes. Current Part Numbering System: Added commercial (missing letter) temperature range.

Mechanical Drawing

The following pages detail the package available to MR2A16A.

Archived Archived Archived Archived Archived Archived

Archived Archived Archived Archived Archived Archived Archived Archived Archived Archived Archived

