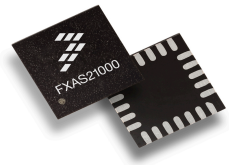
Xtrinsic 3-Axis Digital Rate Gyroscope

FXAS21000

FXAS21000 is a small, low-power, 3-axis yaw, pitch, and roll angular rate gyroscope. The full-scale range is adjustable from ±200°/s to ±1600°/s. It features both I^2C and SPI interfaces.

FXAS21000 is capable of measuring angular rates up to ±1600°/s, with output data rates (ODR) from 1.5625 to 200 Hz. The device may be configured to generate an interrupt when a user-programmable angular rate threshold is crossed on any one of the enabled axes.

FXAS21000 is available in a plastic QFN package; the device is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.

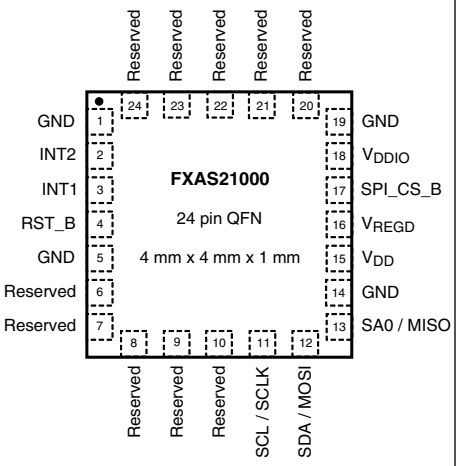


24 QFN
4 mm x 4 mm x 1 mm
Case 2209-01

Features

- 1.95 V to 3.6 V supply voltage; 1.62 V to 3.6 V digital interface voltage
- I^2C and SPI interfaces; I^2C Normal and Fast modes (100 and 400 kHz), SPI at up to 2 MHz (3- and 4-wire modes)
- 192 byte (32 X/Y/Z sample) FIFO buffer with circular and triggered operating modes
- Output data rates (ODR) from 1.5625 to 200 Hz; integrated antialiasing filter ensures that output signal bandwidth = ODR/2
- Angular rate sensitivity of 0.2°/s in ±1600°/s FSR mode
- Low power standby mode
- Rate threshold interrupt
- Integrated self-test function
- No external charge-pump capacitor needed

Top View



Pin Connections

Ordering Information

Part Number	Temperature Range	Package Description	Shipping
FXAS21000CQR1	–40 °C to +85 °C	QFN	Tape and reel

freescale™
Xtrinsic

Table of Contents

1 Typical Applications

- Game controller
- Gyro stabilized electronic compass
- Orientation determination
- Gesture-based user interfaces
- Indoor navigation
- Human machine interface
- Mobile phones
- Toy helicopter
- Virtual reality devices (including glasses)

2 General Description

2.1 Block Diagram

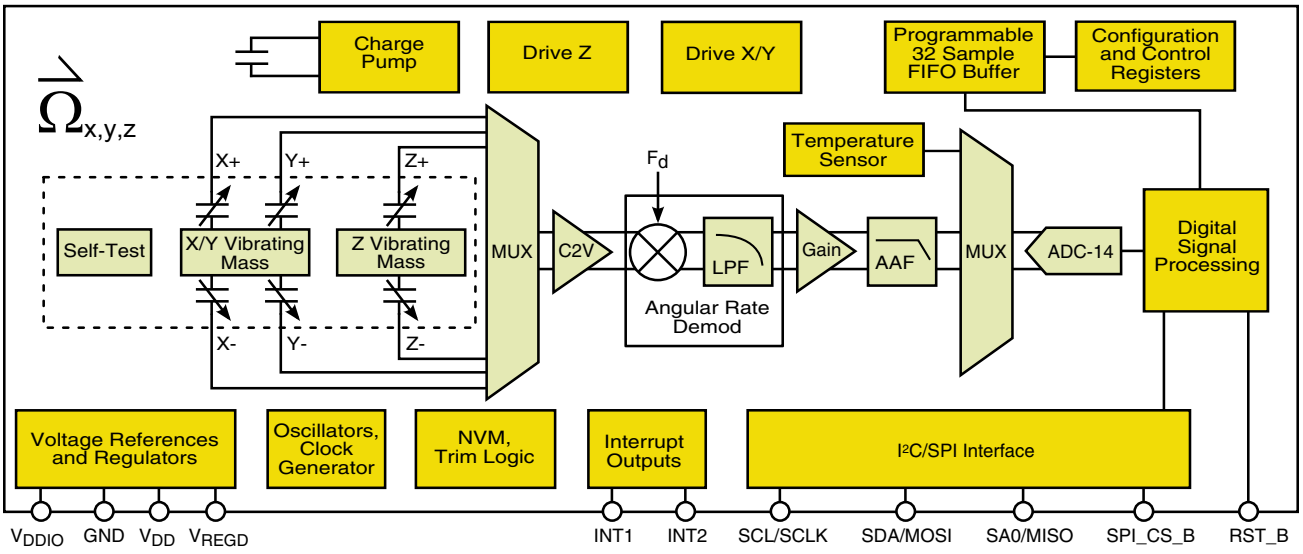


Figure 1. Block Diagram

2.2 Pinout

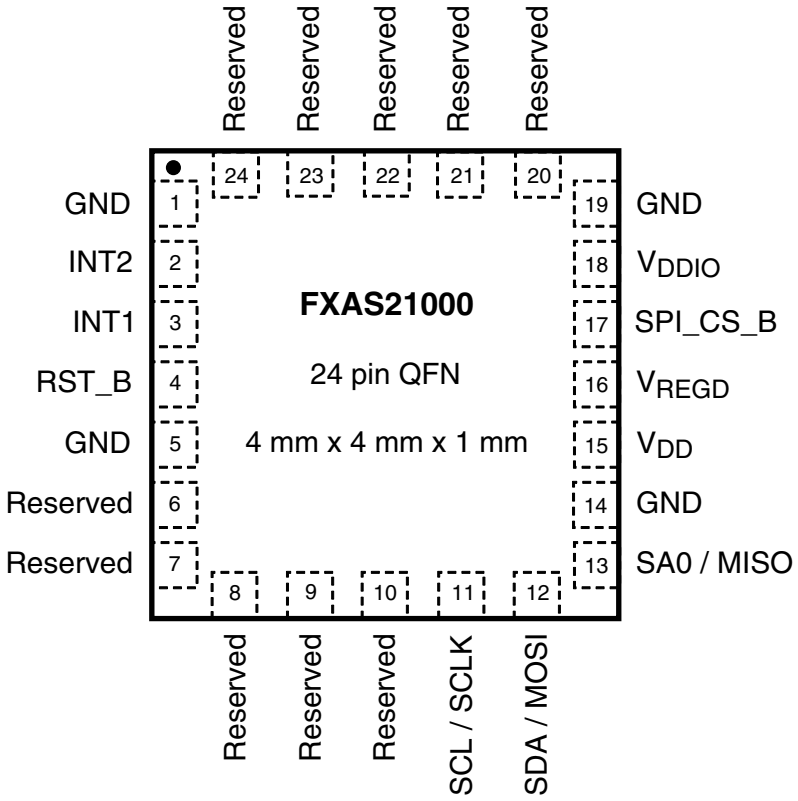


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	GND	Ground
2	INT2	Interrupt Output 2
3	INT1	Interrupt Output 1
4	RST_B	Reset input (active low, connect to V_{DDIO} if unused)
5	GND	Ground
6	Reserved	Reserved - Must be tied to ground
7	Reserved	Reserved - Must be tied to ground
8	Reserved	Reserved - Must be tied to ground
9	Reserved	Reserved - Must be tied to ground
10	Reserved	Reserved - Must be tied to ground
11	SCL/SCLK	I^2C / SPI clock
12	SDA/MOSI/SPI_DIO	I^2C data / SPI 4-wire Master Out Slave In / SPI 3-wire data In/Out[1]
13	SA0/MISO	I^2C address bit0 / SPI 4-wire Master In Slave Out
14	GND	Ground

Table continues on the next page...

Table 1. Pin functions (continued)

Pin	Name	Function
15	V_{DD}	Supply voltage
16	V_{REGD}	Digital regulator output. Please connect a 0.1 uF capacitor between this pin and GND
17	SPI_CS_B	SPI chip select input, active low. This pin must be held logic high when operating in I^2C interface mode (I^2C/SPI_CS_B set high) to ensure correct operation.
18	V_{DDIO}	Interface supply voltage
19	GND	Ground
20	Reserved	Reserved - Must be tied to ground
21	Reserved	Reserved - Must be tied to ground
22	Reserved	Reserved - Must be tied to ground
23	Reserved	Reserved - Must be tied to ground
24	Reserved	Reserved - Must be tied to ground

1. MOSI becomes a bidirectional data pin when FXAS21000 is operated in 3-wire SPI mode with CTRL_REG0[SPIW]=1.

2.3 System Connections

The FXAS21000 offers the choice of connecting to a host processor through either I^2C or SPI interfaces. Figure 3 and Figure 4 show the recommended circuit connection for implementing both options.

2.3.1 Typical Application Circuit—I²C Mode

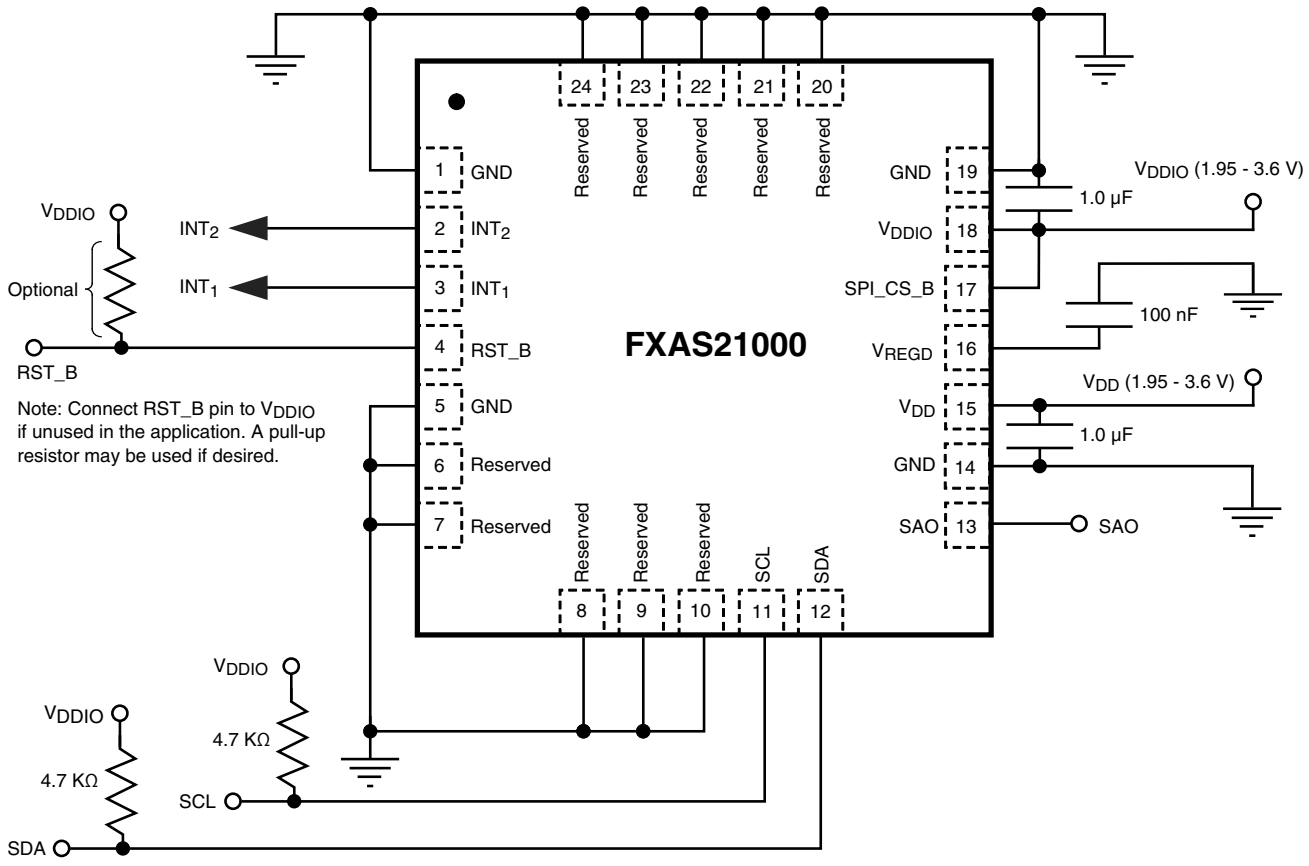


Figure 3. I²C mode electrical connections

2.3.2 Typical Application Circuit—SPI Mode

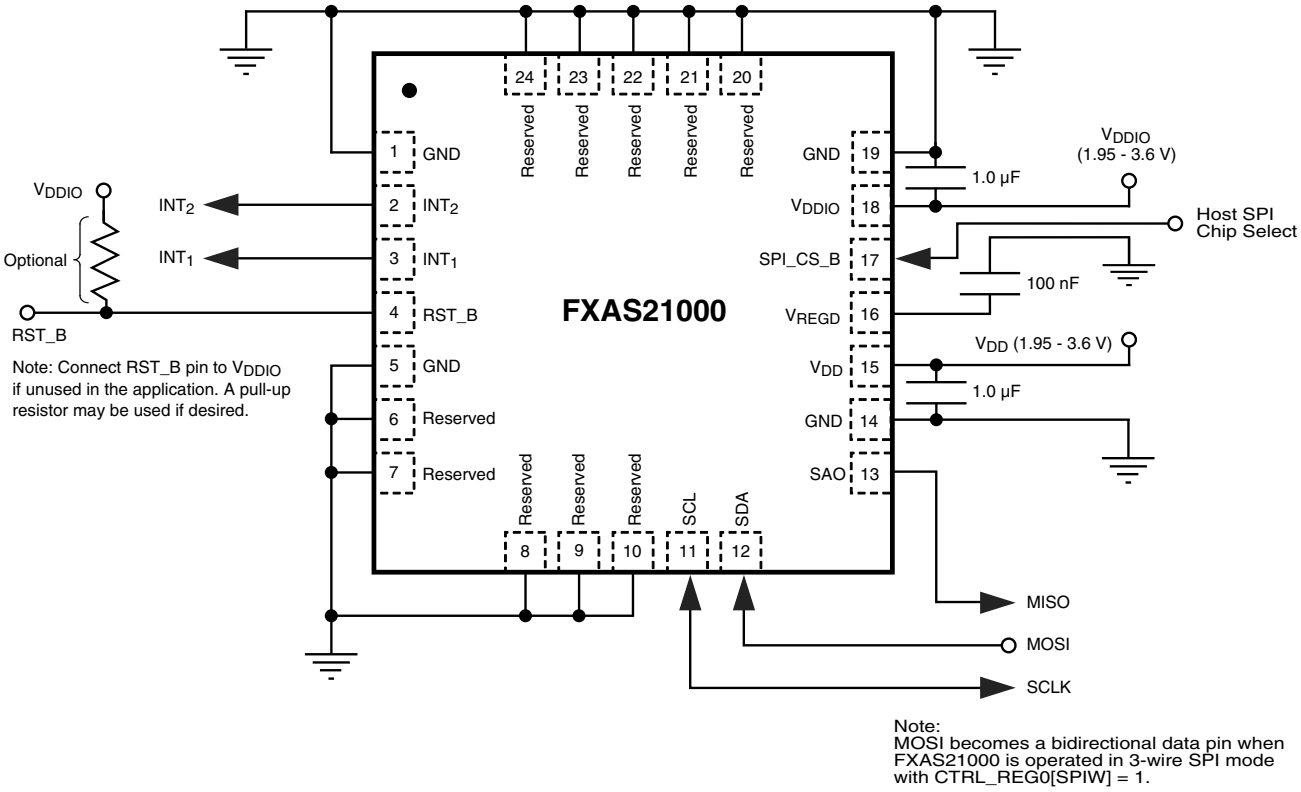


Figure 4. SPI mode electrical connections

2.4 Sensing Direction

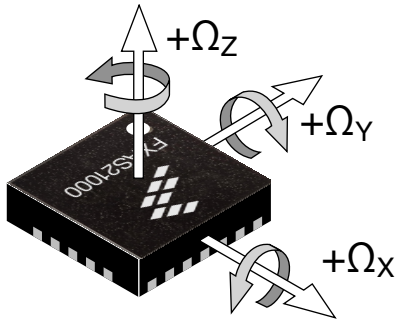


Figure 5. Reference frame for rotational measurement

3 Mechanical and Electrical Specifications

3.1 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either GND or V_{DD}).

Table 2. Absolute maximum ratings

Rating	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.6	V
Interface supply voltage	V_{DDIO}	–0.3	V_{DD} +0.3	V
Input voltage on any control pin (SA0, SCL, SDA)	V_{in}	–0.3	V_{DDIO} +0.3	V
Drop-test height, component	D_{drop}	1.8	—	m
Operating temperature range	T_{OP}	–40	+85	°C
Storage temperature range	T_{STG}	–40	+125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Min	Max	Unit
Human body model (HBM)	V_{HBM}	±2000	—	V
Machine model (MM)	V_{MM}	±200	—	V
Charge device model (CDM)	V_{CDM}	±500	—	V
Latch-up current at T = 85 °C	I_{LU}	±100	—	mA

Caution
This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

	Caution
	This is an ESD sensitive device, improper handling can cause permanent damage to the part.

3.2 Operating Conditions

Table 4. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.95	—	3.6	V
Interface supply voltage	V_{DDIO}	1.62	—	V_{DD} + 0.3	V
Digital high-level input voltage SCL, SDA, SA0, I^2C, RST_B	VIH	0.7 * V_{DDIO}	—	—	V
Digital low-level input voltage SCL, SDA, SA0, I^2C, RST_B	VIL	—	—	0.3 * V_{DDIO}	V
Operating temperature range	Top	–40	+25	+85	°C

3.3 Mechanical Characteristics

Table 5. Mechanical characteristics

Parameter	Symbol	Test Conditions[1]	Min	Typ	Max	Unit
Full-scale range	FS	FS = 00 FS = 01 FS = 10 FS = 11	—	±1600 ±800 ±400 ±200	—	dps
Sensitivity Note: Sensitivity based on XYZ output data registers that are 14-bit left justified data	So	FS = 00 FS = 01 FS = 10 FS = 11	—	0.2 0.1 0.05 0.025	—	dps/LSB
Sensitivity change vs. temperature	TCS	–40 °C ≤ T ≤ 85 °C	—	±0.1	—	%/°C
Initial zero-rate offset	ZRO	Factory calibrated, before board mount	—	±100	—	dps
Zero-rate offset change vs. temperature	TCO	Temperature change < 3 °C/min	—	±0.3	—	dps/°C
Cross axis sensitivity	CAS	—	—	±1	—	%
Sensitivity to linear acceleration	Sa	Acceleration < 3 g	—	±0.5	—	dps/g

Table continues on the next page...

Table 5. Mechanical characteristics (continued)

Parameter	Symbol	Test Conditions[1]	Min	Typ	Max	Unit
Nonlinearity (deviation from linear response)	NL	—	—	±1	—	%FS
Self-test output change	STOC	—	50	—	—	LSB
Output data bandwidth	BW	—	—	ODR/2	—	Hz
Rate noise density	ND	ODR = 100 Hz	—	0.055	—	dps/√Hz
Temperature sensor sensitivity	TSENS	—	—	1	—	°C/LSB

1. V_{DD} = 2.5 V, T = 25 °C unless otherwise noted.

3.4 Electrical Characteristics

Table 6. Electrical characteristics

Parameter	Symbol	Test conditions[1]	Min	Typ	Max	Unit
Current consumption	Idd_{Act}	Probe data on a trimmed oscillator and iref	—	5.8	—	mA
Supply current drain in Standby mode	Idd_{Stby}	Standby mode	—	2	—	µA
Supply current drain in Ready mode	Idd_{Rdy}	Ready mode	—	4.8	—	mA
High-level output voltage INT1, INT2	VOH	IO = 500 µA	0.9 * V_{DDIO}	—	—	V
Low-level output voltage INT1, INT2	VOL	IO = 500 µA	—	—	0.1 * V_{DDIO}	V
Low-level output voltage SDA	VOL_{SDA}	IO = 500 µA	—	—	0.1 * V_{DDIO}	V
Output data rate frequency tolerance	ODR_{TOL}	—	–10	—	+10	% ODR
Signal bandwidth	BW	—	—	ODR/2	—	Hz
Boot time from POR/ Reset to Standby mode	BT	—	—	16	—	µs
Turn-on time 1, Standby to Active mode transition	Ton1	—	—	2/ODR + 250 ms	—	ms
Turn-on time 2, Ready to Active mode transition	Ton2	—	—	2/ODR + 10 ms	—	ms

1. V_{DD} = 2.5 V, T = 25°C unless otherwise noted.

4 Digital Interfaces

The registers embedded inside the FXAS21000 are accessed through either an I^2C or an SPI serial interface. To enable either interface, the V_{DDIO} line must be connected to the interface supply voltage. If V_{DD} is not present and V_{DDIO} is present, FXAS21000 is in shutdown mode and communications on the interface are ignored. If V_{DDIO} is held high, V_{DD} can be powered off and the communications pins will be in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 7. Serial interface pin descriptions

Pin name	Pin description
V_{DDIO}	Digital interface power
I^2C/SPI_CS_B	I^2C/SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI	I^2C serial data/SPI master serial data out slave serial data in
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave out

4.1 I^2C Interface

To use the I^2C interface, the I^2C/SPI_CS_B pin should be connected to V_{DDIO}. The implemented I^2C interface is compliant with I^2C protocol. The 7-bit slave addresses that may be assigned to the FXAS21000 part are 0x20 (with SA0 = 0) and 0x21 (with SA0 = 1). When I^2C/SPI_CS_B is high, the SA0/MISO pin is used to define the LSB of this I^2C address. The key timing constraints are shown in Table 8.

Table 8. Slave timing values

Parameter	Symbol	I^2C Standard Mode[1, 2]		I^2C Fast Mode[1, 2]		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	µs
Hold time (repeated) START condition	$t_{HD;STA}$	4	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	µs
Set-up time for a STOP condition	$t_{SU;STO}$	4	—	0.6	—	µs
SDA data-hold time[2]	$t_{HD;DAT}$	—	—	0.05	0.9[3]	µs

Table continues on the next page...

Table 8. Slave timing values (continued)

Parameter	Symbol	I²C Standard Mode[1, 2]		I²C Fast Mode[1, 2]		Unit
		Min	Max	Min	Max	
SDA valid time	$t_{VD;DAT}$	—	3.45	—	0.9[3]	µs
SDA valid acknowledge time[4]	$t_{VD;ACK}$	—	3.45	—	0.9[3]	µs
SDA setup time	$t_{SU;DAT}$	250	—	100[5]	—	µs
SCL clock low time	t_{LOW}	4.7	—	1.3	—	µs
SCL clock high time	t_{HIGH}	—	—	0.6	—	µs
SDA and SCL rise time	t_r	—	1000	20+0.1C_b[6]	300	ns
SDA and SCL fall time	t_f	—	300	20+0.1C_b[6]	300	ns
Pulse width of spikes on SDA and SCL that must be suppressed by the internal input filter	t_{SP}	—	50	—	50	ns

1. All values refer to VIH (min) and VIL (max) levels.
2. $t_{HD;DAT}$ is the data-hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
4. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. $t_{SU;DAT}$ = maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
6. C_b = total capacitance of one bus line in pF.

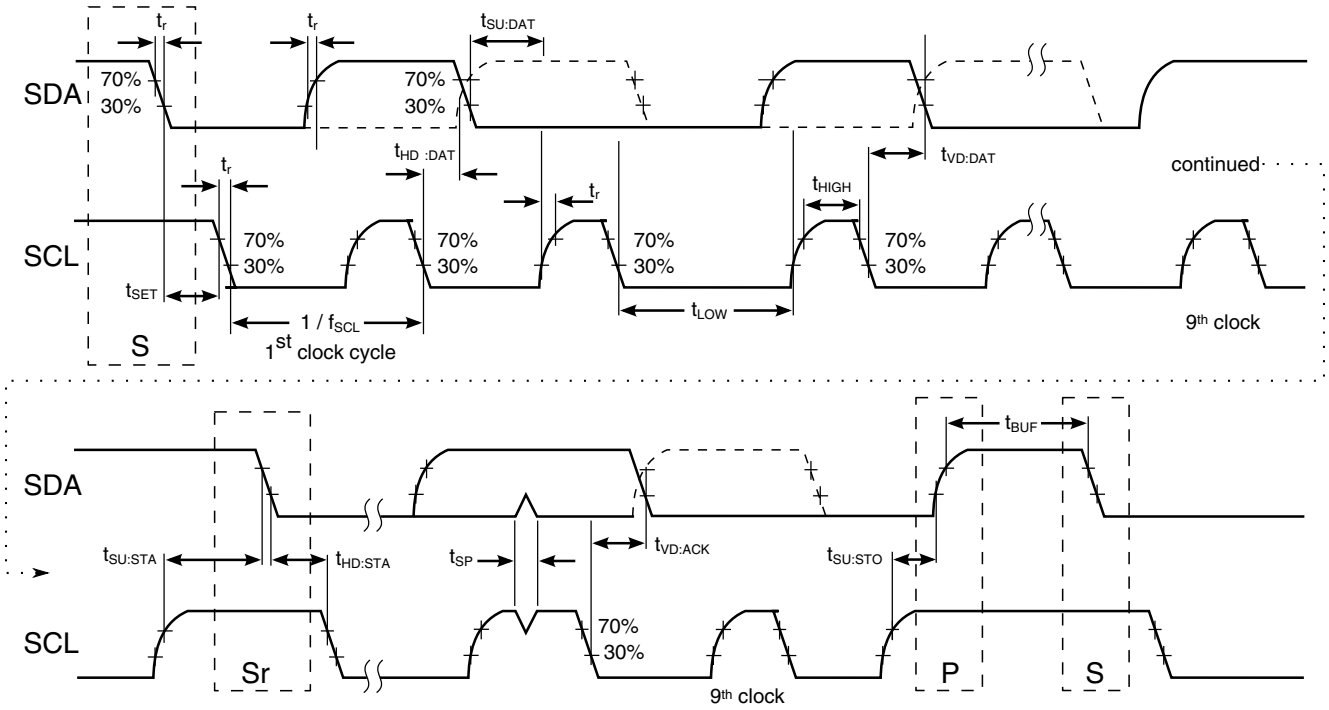


Figure 6. I²C timing diagram

4.1.1 I²C Operation

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The SDA is a bidirectional line used for sending and receiving the data to/from the interface. External pull-up resistors connected to V_{DDIO} are required for SDA and SCL. When the bus is free, both the lines are high. The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pull-up resistor values, and total bus capacitance (trace + device capacitance). For more information, see Table 9.

A transaction on the bus is started through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. Each device in the system compares the first seven bits after the ST condition with its own address. If the two addresses match, the device considers itself addressed by the master. The ninth clock pulse following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer continues only when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching, and not all master devices recognize clock stretching. The FXAS21000 does not support clock stretching.

A LOW-to-HIGH transition on the SDA line while SCL is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer.

Table 9. I²C Address Selection

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0100000 (0x20)	0100001 (0x21)	Factory Default

4.1.2 I²C Read Operations

4.1.2.1 Single-Byte Read

The master (or MCU) transmits an ST to the FXAS21000, followed by the slave address, with the R/W bit set to “0” for a write, and the FXAS21000 sends an acknowledgement. Then, the MCU transmits the address of the register to read and the FXAS21000 sends an acknowledgement. The MCU transmits an SR, followed by the byte containing the slave address and the R/W bit set to “1” for a read from the previously selected register. The FXAS21000 then acknowledges and transmits the data from the requested register. The master does not transmit a no acknowledge (NACK), but transmits an SP to end the data transfer.

4.1.2.2 Multiple-Byte Read

When performing a multiple-byte or burst read, the FXAS21000 increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXAS21000 ACK is received. This continues until a NACK occurs followed by an SP signaling an end of transmission.

4.1.3 I²C Write Operations

4.1.3.1 Single-Byte Write

To start a write command, the MCU transmits an ST to the FXAS21000, followed by the slave address with the R/W bit set to “0” for a write, and the FXAS21000 sends an ACK. Then, the MCU transmits the address of the register to write to, and the FXAS21000 sends an ACK. Then, the MCU transmits the 8-bit data to write to the designated register and the FXAS21000 sends an ACK that it has received the data. Since this transmission is complete, the master transmits an SP to end the data transfer. The data sent to the FXAS21000 is now stored in the appropriate register.

4.1.3.2 Multiple-Byte Write

The FXAS21000 automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXAS21000 ACK is received.

Command	Device Address Bit[6:1]	Device Address Bit[0] (SA0 pin state)	Device Address Bit[6:0]	R/W Bit	Address Byte Transmitted by Master
Read	6'b010000	0	0x20	1	0x41
Write	6'b010000	0	0x20	0	0x40
Read	6'b010000	1	0x21	1	0x43
Write	6'b010000	1	0x21	0	0x42

4.1.3.3 I²C Data Sequence Diagrams

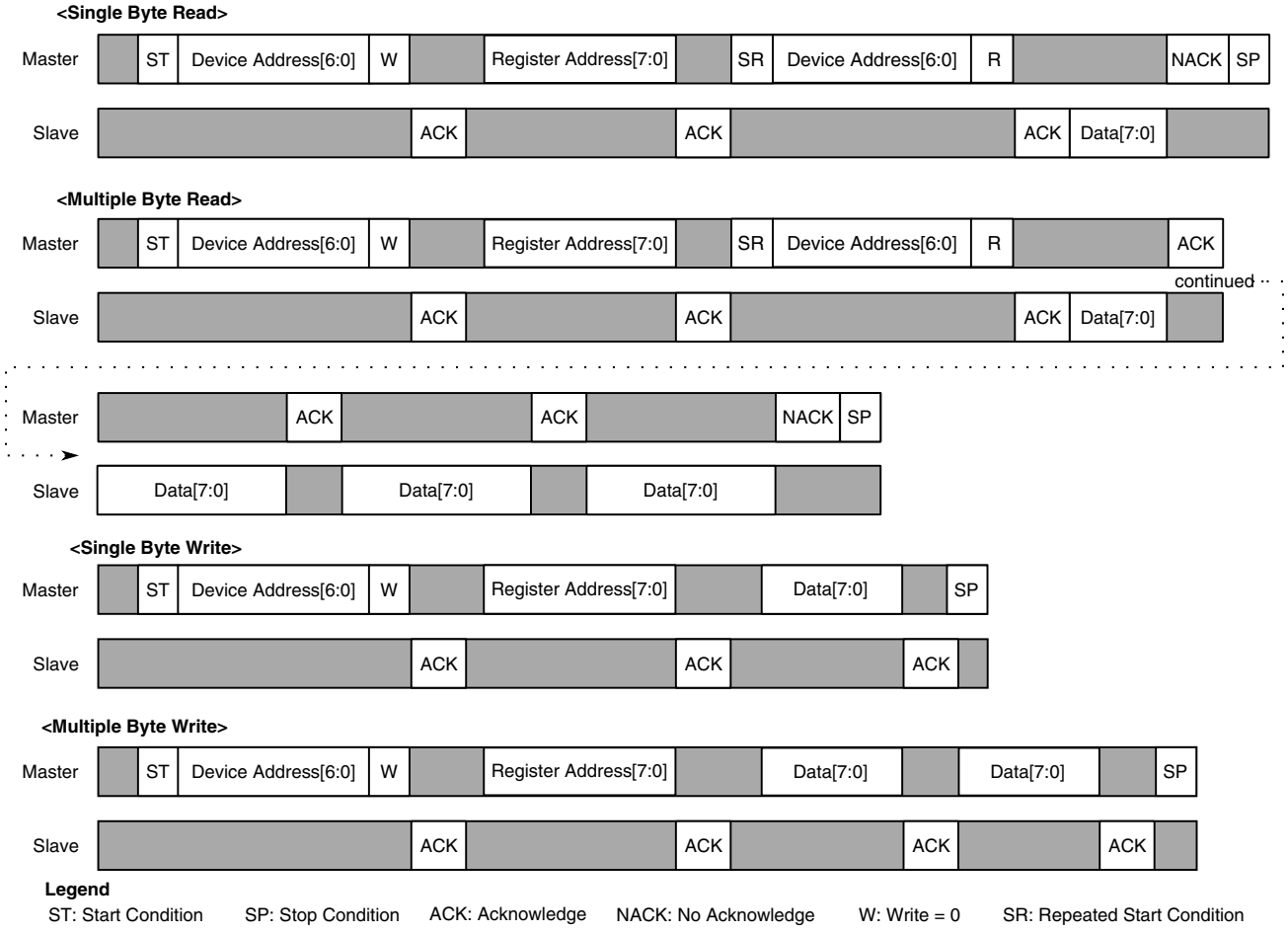


Figure 7. Data sequence diagram

4.2 General SPI Operation (4-Wire Mode)

The SPI_CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction, the master toggles the SPI clock (SCLK). The SCLK polarity is defined as having a base value that is low and the phase where data is captured on the clock's rising edge and data is propagated on a falling edge.[1] Single read and write operations are completed in 16 SCLK cycles or multiples of 8 cycles for multiple read/write operations. The first SCLK cycle uses the first bit on MOSI to determine whether the operation is a read (R/W = 1) or a write, such as R/W=0. The following seven SCLK cycles are the slave register addresses. SCLK cycles and are present on the MOSI line. SCLK cycles nine through 16 are the data that is either read (present on MISO) or to be written (present on MOSI).

The SPI interface implements the point-to-point protocol. Proper bus operation is only guaranteed when the FXAS21000 part is the only SPI slave on the bus.

4.2.1 SPI Write (4-Wire Mode)

A write operation is initiated by transmitting a 0 for the R/W bit. Then, the 7-bit register address, ADDR[6:0](MSB first) is encoded in the first byte. Data to be written starts in the second serialized byte (MSB first). Figure 8 shows the bus protocol for the single write operation.

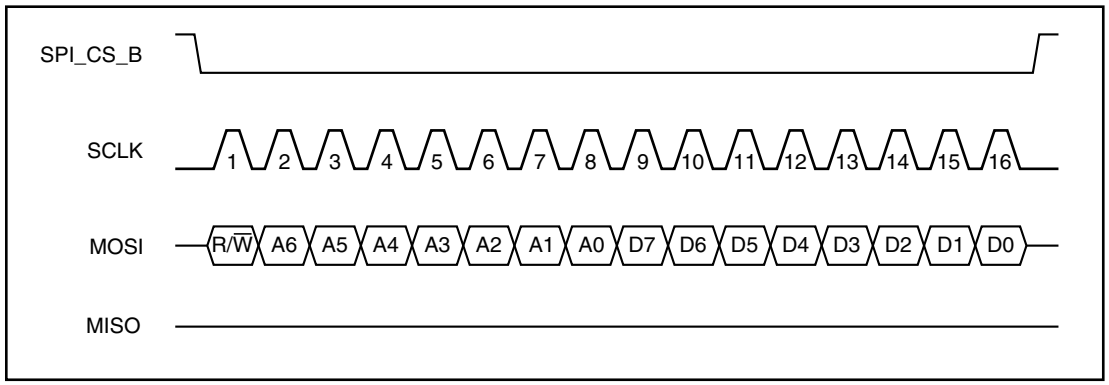


Figure 8. SPI single write operation. R/W = 1

1. From the Freescale SPI protocol definition, the polarity and phase settings are CPOL=0 and CPHA=0.

Multiple write operations performed similar to the single write except bytes are written in multiples of eight SCLK cycles. The register address is auto incremented so that every eighth next clock edges will latch the MSB of the next register. When desired, the rising edge on SPI_CS_B stops the SPI communication.

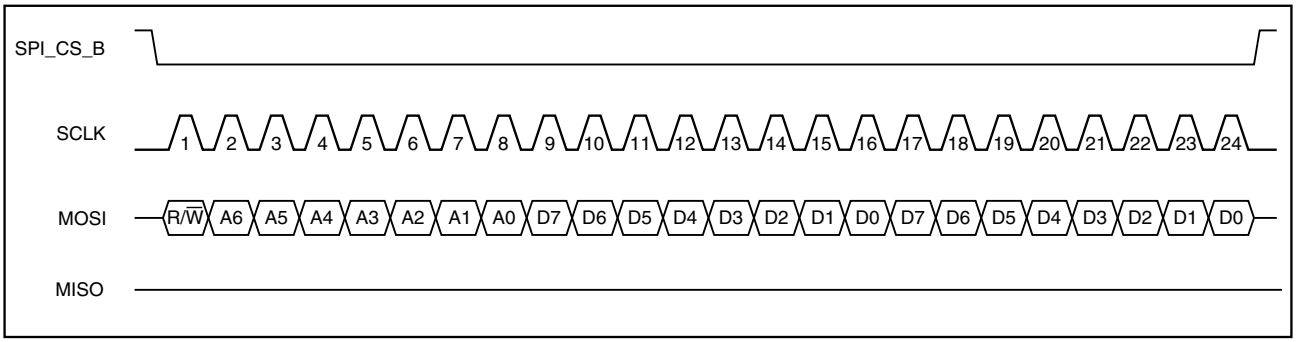


Figure 9. SPI multiple write operation showing 2 bytes written

4.2.2 SPI Single Read (4-Wire Mode)

A READ operation is initiated by transmitting a 1 for the R/W bit. Then the 7-bit register address, ADDR[6:0] is encoded in the first byte. The data is read from the MISO pin (MSB first). Figure 10 show the bus protocol for a single read operation.

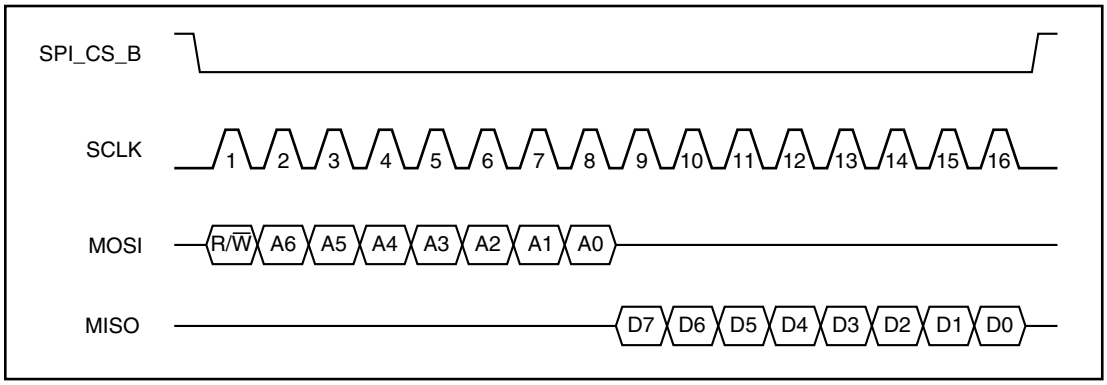


Figure 10. SPI single read operation. R/W = 1

Multiple read operations are performed similar to single read except bytes are read in multiples of eight SCLK cycles. The register address is auto incremented so that every eighth next clock edges will latch the MSB of the next register. When desired, the rising edge on SPI_CS_B stops the SPI communication.

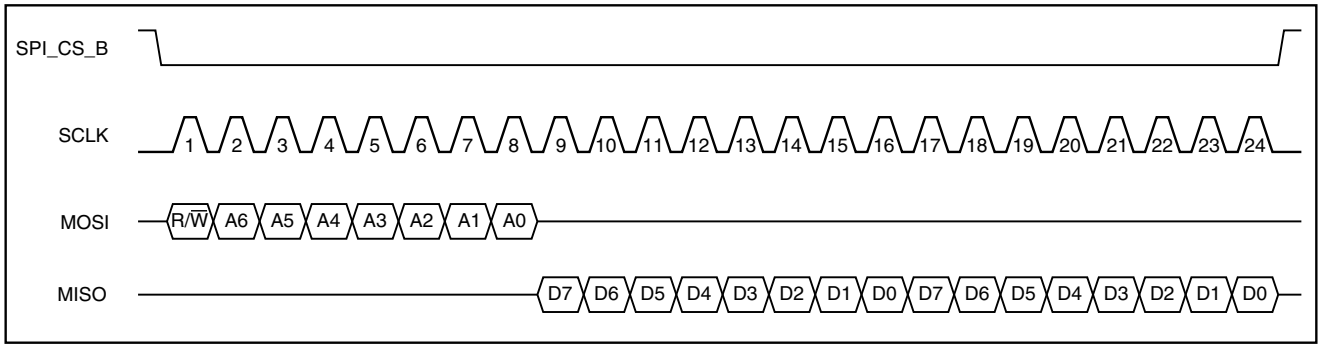


Figure 11. SPI multiple read operation showing 2 bytes written

4.2.3 SPI 3-Wire Mode

The FXAS21000 can be configured to operate in 3-wire mode. In this mode the only signal pins used are SPI_CS_B, SCLK, and MOSI; the MISO pin is not used. 3-wire mode is selected by setting the SPIW bit in CTRL_REG0.

Read operations in 3-Wire mode are different than read operations in 4-Wire mode.

- At the end of the address cycle of read operations in 3-Wire mode, the MOSI pin switches from SI to SO
- Multiple read operations in 3-wire mode use auto-increment
- Multiple read operations in 3-wire mode return data on the MOSI pin

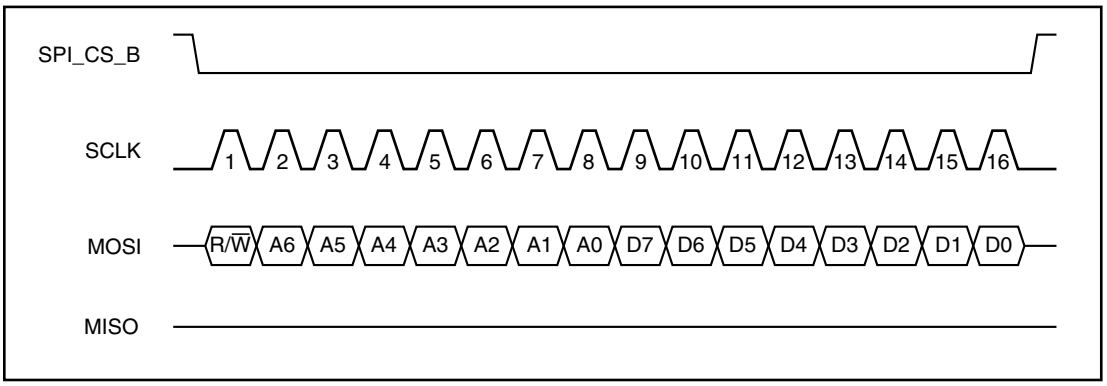


Figure 12. SPI 3-Wire single read operation

Write operations in 3-wire mode are identical to write operation in 4-wire mode since the MISO pin is not used in either mode of operation.

5 Modes of Operation

The device may be placed into one of three functional modes:

- **Standby:** Some digital blocks are enabled; I^2C/SPI communication with FXAS21000 is possible.
- **Active:** All blocks are enabled (digital and analog), the device is actively measuring the angular rate at the ODR specified in CTRL_REG1 (0x13).
- **Ready:** The drive circuits are running, but no measurements are being made.

The functional mode is selected using CTRL_REG1 (0x13). After a power-on-reset (POR) or triggered reset event (software or hardware pin), the device performs a boot sequence and loads the registers with their preset values, which are stored within the non-volatile memory (NVM).

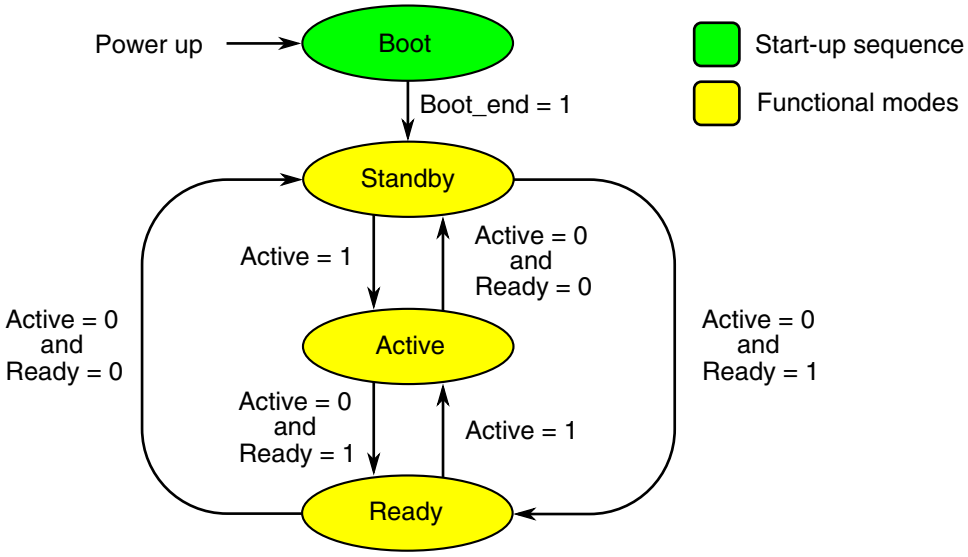


Figure 13. Functional mode diagram

6 Functionality

The FXAS21000 is a low-power, digital-output, 3-axis gyroscope with both I^2C and SPI interfaces. The functionality includes the following:

- 14-bit data left justified in 2's complement format
- Configurable full scale ranges of ±200, ±400, ±800 and ±1600 dps
- Configurable output data rates from 1.5625 to 200 Hz
- Internal low-pass filter cutoff of 200 Hz and configurable high-pass filter cutoff
- Embedded rate detection with programmable debounce
- 14-bit configurable, 32-sample FIFO
- 2 external pins that are configurable to trigger on data-ready or FIFO events
- Self-test function for indication of device health
- Single control bit for zero-rate compensation

Data for each axis must be read from the respective data registers two bytes at a time; for example, one byte for most significant byte and one byte for least significant. Combining these two bytes results in a 16-bit 2's complement signed integer with the sign bit in bit location #15 and the least significant bit in bit location #2. See the tables below.

Bit	**15**	14	13	12	11	10	9	8
Data bit	**D13**	D12	D11	D10	D9	D8	D7	D6
	Sign bit							

Bit	7	6	5	4	3	**2**	1	0
Data bit	D5	D4	D3	D2	D1	**D0**	X	X
						LSB		

The conversion from counts to unit of dps is done by first converting the 16-bit signed integer to 14-bit left-justified signed integer. This can be done by dividing the counts by 4 then multiplying by the appropriate sensitivity value for the currently selected full-scale range. See Table 32 for nominal sensitivity values.

6.1 FIFO Data Buffer

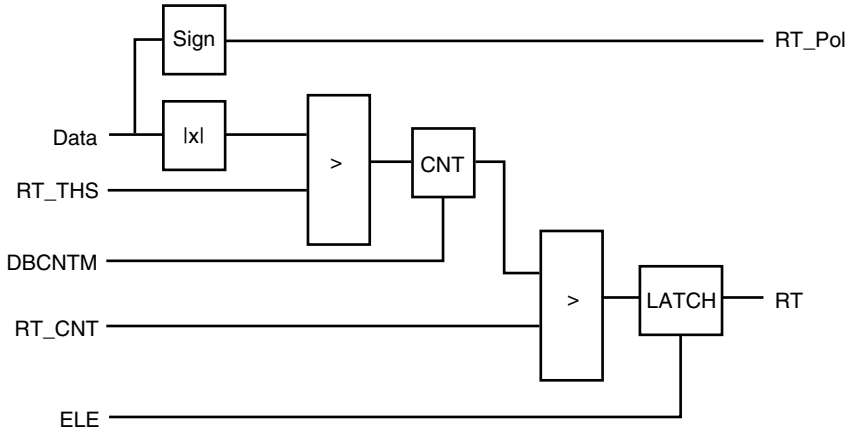
FXAS21000 contains a 32-sample FIFO data buffer that is useful for reducing the frequency of transactions on the I^2C/SPI bus. The FIFO can also provide system level power savings by allowing the host processor/MCU to go into a sleep/low-power mode while the FXAS2100 collects up to 32 samples of 3-axis angular rate data.

The FIFO is configured to operate in Circular Buffer mode or Stop mode, depending on the settings made in the F_SETUP (0x09) register. The Circular Buffer mode allows the FIFO to be filled with a new sample replacing the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This is useful in situations where the processor is waiting for a specific interrupt to indicate that the data must be flushed to analyze the event.

The FXAS21000 FIFO Buffer has a configurable watermark, allowing an interrupt to be signaled to the processor after a configurable number of samples enter the buffer (1 to 32).

6.2 Rate Threshold Detection Function

The embedded rate detection function can be used to detect an angular rate event that exceeds a programmed threshold on any one of the enabled axes for longer than the programmed debounce time and to trigger an interrupt signal. The function is fully programmable, offering flexibility for the various potential use cases.



Output data rate (Hz)	Counter clock period (ms)	Event duration range
200	5	0 – 1.275
100	10	0 – 2.55
50	20	0 – 5.1
25	40	0 – 10.2
12.5	80	0 – 20.4
6.25	160	0 – 40.8
3.125	320	0 – 81
1.5625	640	0 – 163

The rate threshold (RT) event flag is set in the INT_SOURCE_FLAG (0x0B) register. It is cleared by reading the RT_SRC register. Using CTRL_REG2 (0x14), the device can be configured to generate an external interrupt on either the INT1 or INT2 pin when a rate threshold event condition occurs.

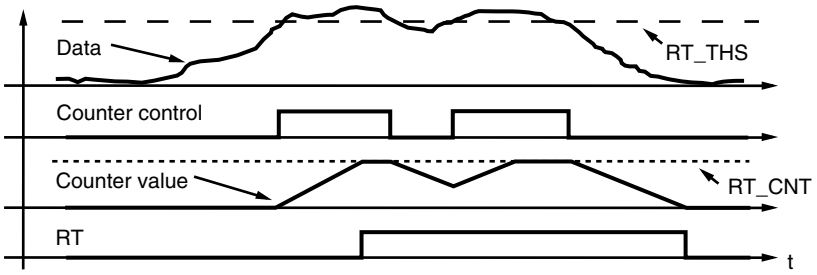


Figure 14. RT example 1

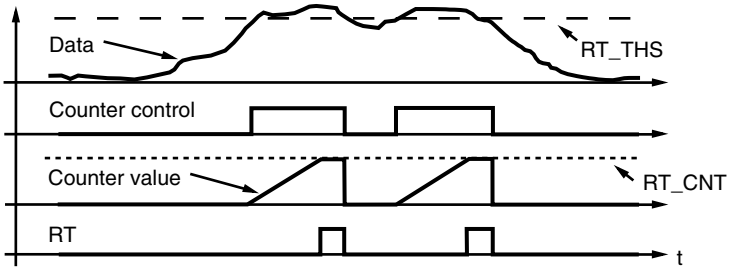


Figure 15. RT example 2

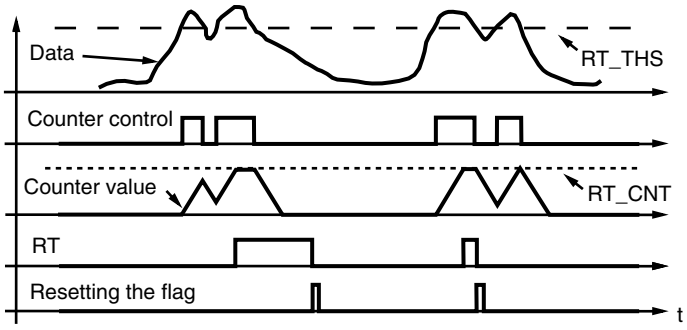


Figure 16. RT example 3

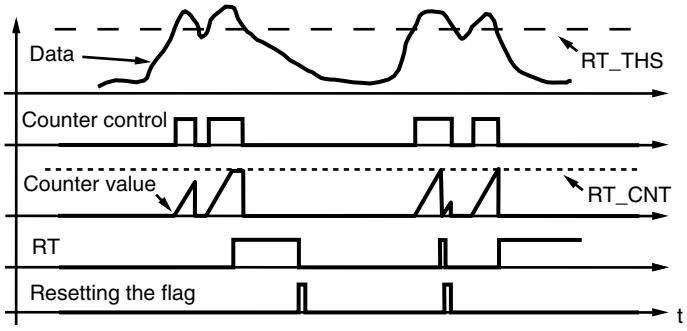


Figure 17. RT example 4

7 Register Descriptions

Table 11. Register address map

Name	Type	Register address	Default value	Comment
STATUS	R	0x00	0x00	Alias for DR_STATUS or F_STATUS
OUT_X_MSB	R	0x01	0x00	14-bit X-axis measurement data bits 13:6
OUT_X_LSB[1,2]	R	0x02	0x00	14-bit X-axis measurement data bits 5:0
OUT_Y _MSB	R	0x03	0x00	14-bit Y-axis measurement data bits 13:6
OUT_Y_LSB[1,2]	R	0x04	0x00	14-bit Y-axis measurement data bits 5:0
OUT_Z_MSB	R	0x05	0x00	14-bit Z-axis measurement data bits 13:6
OUT_Z_LSB[1,2,3]	R	0x06	0x00	14-bit Z-axis measurement data bits 5:0
DR_STATUS	R	0x07	0x00	Data-ready status information
F_STATUS	R	0x08	0x00	FIFO Status
F_SETUP	R/W	0x09	0x00	FIFO setup
F_EVENT	R	0x0A	—	FIFO event
INT_SRC_FLAG	R	0x0B	—	Interrupt event source status flags

Table continues on the next page...

Table 11. Register address map (continued)

Name	Type	Register address	Default value	Comment
WHO_AM_I	R	0x0C	0xD1	Device ID
CTRL_REG0	R/W	0x0D	0x00	Control register 0: Full-scale range selection, high-pass filter control, SPI mode selection
RT_CFG	R/W	0x0E	0x00	Rate threshold function configuration
RT_SRC	R	0x0F	0x00	Rate threshold event flags status register
RT_THS	R/W	0x10	0x00	Rate threshold function threshold value register
RT_COUNT	R/W	0x11	0x01	Rate threshold function debounce counter
TEMP[4]	R	0x12	0x00	Device temperature in °C
CTRL_REG1	R/W	0x13	0x00	Control register 1: Operating mode, ODR selection, self-test and reset control
CTRL_REG2	R/W	0x14	0x00	Control register 2: Interrupt configuration settings

1. Data output LSB registers only contain valid data after a read of the corresponding axis MSB data register.
2. The two least significant bits of each axes data LSB are not used. Data must be right shifted by two bits in the user application to obtain a properly scaled 16-bit 2's compliment rate value.
3. After this register is read, the next read register by the auto-increment process is STATUS at 0x00.
4. This register is reset only by a hard reset (POR or assertion of the RST_B pin). A soft reset will not reset this register.

7.1 STATUS (Address 0x00)

The STATUS register content depends on the FIFO mode setting. It is a copy of either DR_STATUS (0x07) or F_STATUS (0x08). This allows for easy reading of the relevant status register before reading the current sample. For more information, see DR_STATUS (0x07) or F_STATUS (0x08) register definitions.

7.2 OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB (0x01–0x06)

X-, Y-, and Z-axis sample data are represented in 14-bit, 2's complement format. The output data registers are either updated at the output data rate (F_MODE = 00) or alternately point to the first sample stored in the FIFO buffer (F_MODE > 00). Using the burst-read mode, the data is read in the following order: OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB and then OUT_Z_LSB.

Table 12. OUT_X_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	XD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 13. OUT_X_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	XD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

Table 14. OUT_Y_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	YD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 15. OUT_Y_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	YD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

Table 16. OUT_Z_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	ZD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 17. OUT_Z_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	ZD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

7.3 DR_STATUS (0x07)

This DR_STATUS register provides the sample data acquisition status and reflects the real-time updates to the OUT_X, OUT_Y, and OUT_Z registers.

ZYXOW is set to 1 whenever new X-, Y-, and Z-axis data is acquired before completing the retrieval of the previous set. ZYXOW is cleared after the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read.

ZOW (and respectively YOW, XOW) is set to 1 whenever a new Z-axis (and respectively Y-axis, X-axis) acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. ZOW (and respectively YOW, XOW) is cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read.

ZYXDR signals that a new acquisition for any of the channels is available. ZYXDR is cleared when the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read.

ZDR (and respectively **YDR**, **XDR**) is set to 1 whenever a new Z-axis (and respectively Y-axis, X-axis) data acquisition is completed. ZDR (and respectively YDR, XDR) is cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read.

Table 18. DR_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
Write								
Reset	0	0	0	0	0	0	0	0

Table 19. DR_STATUS field descriptions

Field	Description
ZYXOW	X-, Y-, Z-axis data overwrite 0: No data overwrite has occurred 1: X, Y, and Z data overwrite occurred before the previous data was read

Table continues on the next page...

Table 19. DR_STATUS field descriptions (continued)

Field	Description
ZOW	Z-axis data overwrite 0: No data overwrite has occurred 1: Z-axis data overwrite occurred before the previous data was read
YOW	Y-axis data overwrite 0: No data overwrite has occurred 1: Y-axis data overwrite occurred before the previous data was read
XOW	X-axis data overwrite 0: No data overwrite has occurred 1: X-axis data overwrite occurred before the previous data was read
ZYXDR	X-, Y-, and Z-axis data available 0: No new data is ready 1: New data is ready
ZDR	Z-axis new data available 0: No new Z-axis data is ready 1: New Z-axis data is ready
YDR	Z-axis new data available 0: No new Y-axis data is ready 1: New Y-axis data is ready
XDR	Z-axis new data available 0: No new X-axis data is ready 1: New X-axis data is ready

7.4 F_STATUS (0x08)

If the FIFO is enabled, the F_STATUS status register indicates the current status of the FIFO. When the FIFO is enabled, the STATUS register at address 0x00 also contains the contents of the F_SETUP (0x09) register to facilitate the emptying of the FIFO by the host processor.

A FIFO overflow event, such as F_CNT = 32, asserts the F_OVF flag.

A FIFO sample count greater than or equal to the sample count watermark (determined by the F_WMRK field in register F_SETUP (0x09)) asserts the F_WMKF event flag. F_OVF and F_WMKF flags are cleared when this register is read. Reading F_STATUS also clears the SRC_FIFO bit in the INT_SOURCE_FLAG (0x0B) register.

The F_CNT[5:0] bits indicate the number of samples currently stored in the FIFO. A count value of 6'b000000 indicates that the FIFO is empty.

Table 20. F_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	F_OVF	F_WMKF	F_CNT[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 21. F_Status field descriptions

Field	Description
F_OVF	FIFO overflow flag 0: No overflow detected 1: Overflow detected
F_WMKF	FIFO watermark flag 0: No watermark detected 1: Watermark detected
F_CNT[5:0]	FIFO sample counter

7.5 F_SETUP (0x09)

This register is used to configure the FIFO. The FIFO update rate is set by the selected system ODR (DR bits in CTRL_REG1 (0x13)). The FIFO read pointer is incremented whenever the Z-axis data is read.

NOTE

To avoid the loss of data, the user must burst-read all six bytes of sample data (three axes) in a single I^2C or SPI transaction.

F_MODE is used to select the FIFO operating mode. In the Circular Buffer mode, the oldest sample is discarded and replaced by the newest sample when the buffer is full, such as F_STATUS[F_CNT] = 32. In the Stop mode, the FIFO will stop accepting new samples when the buffer is full (i.e. F_STATUS[F_CNT] = 32). The FIFO operating

mode cannot be switched between Circular and Stop modes while the FIFO is enabled. To change the FIFO operating mode, the device must first be disabled by setting F_MODE[1:0] = 00.

The FIFO is cleared whenever the FIFO is disabled. Disabling the FIFO also clears the F_OVF, F_WMKF, and F_CNT bits in the F_STATUS (0x08) register.

F_WMRK[5:0] is used to set the watermark level. A FIFO sample count exceeding the watermark level does not stop the FIFO from accepting new data. To suppress FIFO watermark event flag generation, F_WMRK[5:0] can be set to 0x00.

Table 22. F_Setup register

Bit	7	6	5	4	3	2	1	0
Read	F_MODE[1:0]		F_WMRK[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 23. F_SETUP field descriptions

Field	Description
F_MODE[1:0]	00: FIFO is disabled 01: Circular Buffer mode 1x: Stop mode
F_WMRK[5:0]	FIFO sample count watermark setting. Default value 6'b000000.

7.6 F_EVENT (0x0A)

This register is used to monitor the system state and FIFO event.

F_EVENT indicates if either F_WMKF or F_OVF flags are set. The F_STATUS register must be read to determine which event occurred.

FE_TIME[4:0] is the number of samples acquired since a FIFO event flag (overflow or watermark) was asserted. It is reset when F_STATUS (0x08) is read.

Table 24. F_Event register

Bit	7	6	5	4	3	2	1	0
Read	0	0	F_EVENT	FE_TIME[4:0]				
Write								
Reset	0	0	0	0	0	0	0	0

Table 25. F_EVENT field descriptions

Field	Description
F_EVENT	FIFO Event 0: FIFO Event not detected 1: FIFO Event was detected
FE_TIME [4:0]	Time elapsed since the event

7.7 INT_SOURCE_FLAG (0x0B)

This register provides the event-flag status for the functions within the device. Reading the INT_SRC_FLAG register does not reset any event-flag source bits; they are reset by reading the appropriate source register.

BOOTEND is asserted as soon as the device boot sequence has completed.

SRC_DRDY is asserted whenever a data-ready event triggers the interrupt. It is cleared under the following conditions:

- Whenever all bits in the DR_STATUS (0x07) are cleared
- Whenever ZYXDR, ZDR, YDR and XDR are cleared
- Whenever ZYXDR is cleared
- Whenever the MSB's of the X, Y, and Z axes sample data are read

SRC_RT indicates that the rate threshold event flag triggered the interrupt. It is cleared by reading RT_SRC register.

SRC_FIFO indicates that the FIFO triggered the interrupt. It is set whenever F_OVF or F_WMKF are set, provided the FIFO interrupt is enabled (INT_EN_FIFO=1). It is cleared by reading the F_STATUS (0x08) register.

Table 26. INT_SRC_ register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	BOOTEND	SRC_FIFO	SRC_RT	SRC_DRDY
Write								
Reset	0	0	0	0	0	0	0	0

Table 27. INT_SRC_FLAG field descriptions

Field	Description
SRC_FIFO	FIFO event source flag
SRC_RT	Rate threshold event source flag
SRC_DRDY	Data ready event source flag Cleared by reading the MSB's of the X, Y, and Z axes sample data
BOOTEND	Boot sequence complete event flag

7.8 WHO_AM_I (0x0C)

The WHO_AM_I register is the device identification register. This register contains the device identifier which is factory programmed to 0xD1.

Table 28. WHO_AM_I

Bit	7	6	5	4	3	2	1	0
Read	1	1	0	1	0	0	0	1
Write								
Reset	1	1	0	1	0	0	0	1

7.9 CTRL_REG0 (0x0D)

Register CTRL_REG0 is used for general control and configuration of the FXAS21000. The bit fields in CTRL_REG0 should be changed only in Standby or Ready modes. Accuracy of the output data is not guaranteed if these bits are changed when the device is in Active mode.

SPIW selects between the 3- or 4-wire SPI interface modes.

SEL[1:0] selects the high-pass filter cutoff frequency. Details of the high-pass filter settings are shown in Table 31.

HPF_EN enables the high-pass filter. Note that the high-pass filter is “initialized” on mode change, ODR change, and assertion of the zero-rate register bit. When enabled, HPF is applied to the angular rate data supplied to the output registers/FIFO and the embedded rate threshold algorithm.

FS[1:0] selects the full scale of the device as per Table 32.

Table 29. CTRL_REG0

Bit	7	6	5	4	3	2	1	0
Read Write	0	0	SPIW	SEL[1:0]		HPF_EN	FS[1:0]	
Reset	0	0	0	0	0	0	0	0

Table 30. CTRL_REG0 field descriptions

Field	Description
SPIW	SPI interface mode selection 0: SPI 4-wire mode 1: SPI 3-wire mode (MOSI is used for IN/OUT signals)
SEL[1:0]	High-pass filter cutoff frequency selection
HPF_EN	High-pass filter enable 0: High-pass filter disabled 1: High-pass filter enabled
FS[1:0]	Full-scale range selection

Table 31. High-pass filter cutoff frequency selection

SEL1	SEL0	Cutoff Frequency in Hz versus ODR							
		200 Hz	100 Hz	50 Hz	25 Hz	12.5 Hz	6.25 Hz	3.15 Hz	1.5625 Hz
0	0	10	5	2.5	1.25	0.625	0.313	0.156	0.078
0	1	8	4	2.0	1.00	0.500	0.250	0.125	0.063
1	0	6	3	1.5	0.75	0.375	0.188	0.094	0.047
1	1	4	2	1.0	0.50	0.250	0.125	0.063	0.031

Table 32. Selectable Full Scale Ranges

FS1	FS0	Range (dps)	Nominal Sensitivity (dps/LSB)
0	0	±1600	0.2
0	1	±800	0.1
1	0	±400	0.05
1	1	±200	0.025

7.10 RT_CFG (0x0E)

The RT_CFG register is used to enable the Rate Threshold interrupt generation.

ELE enables the latch of a threshold crossing event. See Modes of Operation for more details. ZTEFE (respectively YTEFE, XTEFE) are enable bits for rate threshold event detection on the Z (respectively Y, X) axis.

Table 33. RT_ CFG Register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	ELE	ZTEFE	YTEFE	XTEFE
Write								
Reset	0	0	0	0	0	0	0	0

Table 34. RT_CFG field descriptions

Field	Description
ELE	Event latch enable 0: Event flag latch disabled 1: Event flag latch enabled
ZTEFE	Event flag enable on Z rate 0: Z Event detection disabled 1: Z Event detection enabled
YTEFE	Event flag enable on Y rate 0: Event detection disabled 1: Y Event detection enabled
XTEFE	Event flag enable on X rate 0: Event detection disabled 1: X Event detection enabled

7.11 RT_SRC (0x0E)

This register indicates the source of the Rate Threshold event. It also clears the RT_SRC flag in the INT_SOURCE_FLAG (0x0B) register.

EA is asserted whenever a rate threshold event has been detected on one of the axis. It is cleared by reading.

ZRT (respectively YRT, XRT) indicates that a rate event (as defined in Modes of Operation) has been detected on the Z (respectively Y, X) axis. ZRT (respectively YRT, XRT) are cleared when read if they have been latched (ELE = 1).

Z_RT_Pol (respectively Y_RT_Pol, X_RT_Pol) indicates the rate polarity for the event detected on the Z (respectively Y,X) axis.

Table 35. RT_ SRC Register

Bit	7	6	5	4	3	2	1	0
Read	0	EA	ZRT	Z_RT_Pol	YRT	Y_RT_Pol	XRT	X_RT_Pol
Write								
Reset	0	0	0	0	0	0	0	0

Table 36. RT_SRC field descriptions

Field	Description
EA	Event active flag 0: No event flags have been asserted 1: One or more event flags have been asserted
ZRT	Z rate event 0: Z rate lower than RT_THS value 1: Z rate greater than RT_THS event has occurred
Z_RT_Pol	Polarity of Z event 0: Z event was Positive 1: Z event was Negative
YRT	Y rate event 0: Y rate lower than RT_THS value 1: Y rate greater than RT_THS value event has occurred
Y_RT_Pol	Polarity of Y event 0: Y event was Positive 1: Y event was Negative
XRT	X rate Event 0: X rate low than RT_THS value 1: X rate greater than RT_THS value event has occurred
X_RT_Pol	Polarity of X event 0: X event was positive 1: X event was negative

7.12 RT_THS (0x10)

The RT_THS register sets the threshold limit for the detection of the rate and the debounce counter mode. See Modes of Operation for more details.

DBCNTM selects the debounce counter mode.

THS is the 7-bit unsigned number setting the rate threshold. The threshold is given by the following formula:

$$Rate\_threshold = THS * \frac{Full\_scale}{128}$$

Table 37. RT_THS register

Bit	7	6	5	4	3	2	1	0
Read	DBCNTM	THS[6:0]						
Write								
Reset	0	0	0	0	0	0	0	0

Table 38. RT_THS field descriptions

Field	Description
DBCNTM	Debounce counter mode selection 0: Decrementing counter 1: Clearing counter
THS[6:0]	Unsigned 7-bit rate threshold value

7.13 RT_COUNT (0x11)

The RT_COUNT sets the number of debounce counts. See Modes of Operation for more details.

Dn represents the number of counts needed before asserting the rate threshold event flag. It is linked to the event duration through the relationship with the ODR.

Table 39. RT_COUNT register

Bit	7	6	5	4	3	2	1	0
Read	D[7:0]							
Write								
Reset	0	0	0	0	0	0	0	1

Table 40. RT_COUNT field descriptions

Field	Description
D[7:0]	Debounce counter value.

7.14 TEMP (0x12)

The TEMP register contains an 8-bit 2's complement temperature value with a range of –128 °C to +127 °C, with a scaling of 1 °C/LSB. This register is reset only by a hard reset (POR/RST_B pin assertion); a soft reset, such as setting CTRL_REG1[RST] = 1, will not reset this register.

Table 41. TEMP register

Bit	7	6	5	4	3	2	1	0
Read	Temp[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

7.15 CTRL_REG1 (0x13)

The CTRL_REG1 register is used to set generic control of the IC.

NOTE

Control bits in CTRL_REG1 should be changed only in Standby or Ready mode. Accuracy of the data is not guaranteed if these bits are changed when the device is in Active mode.

ZR_cond is used to trigger the offset compensation. For this reason, it is meant to be used only when the IC is in zero rate condition on all axes. Writing a '1' to this bit initiates the internal zero-rate offset calibration. The ZR_cond bit self-clears after the zero-rate offset calculation, and it can only be used once after a hard or soft reset has occurred. In order to use the ZR_cond a second time, the device has to be reset either with a hard or soft reset.

Asserting RST triggers a synchronous reset of the IC. On reset, all registers revert to their default reset values. This bit is self reset after assertion.

ST bit activates the self test function. When ST is set to one, a data output change will occur even if no rate is applied. This allows the host application to check the functionality of the sensor and the entire measurement signal chain.

Table 42. CTRL_REG1 register

Bit	7	6	5	4	3	2	1	0
Read	ZR_cond	RST	ST	DR[2:0]			Active	Ready
Write								
Reset	0	0	0	0	0	0	0	0

Table 43. CTRL_REG1 field descriptions

Field	Description
ZR_cond[1]	Zero-rate condition
RST	Software Reset 0: Device reset disabled 1: Device reset triggered
ST	Self-test enable 0: self test disabled 1: self test triggered
DR[2:0]	Data rate selection
Active	Standby/Active
Ready	Standby/Ready

1. ZR_cond may be written only after 1st sample is available, it uses the current sample for calibration. ZR_cond should not be used when HPF is enabled.

DR[2:0] bits select the output data rate for angular rate samples as per Table 44.

Table 44. Output data rate selection

DR2	DR1	DR0	ODR (Hz)	Period (ms)
0	0	0	200.0	5
0	0	1	100.0	10
0	1	0	50.0	20
0	1	1	25	40
1	0	0	12.5	80
1	0	1	6.25	160
1	1	0	3.125	320
1	1	1	1.5625	640

The Active and Ready bits are used to set the IC state. In Standby mode, the IC is only capable of digital communication on I^2C or SPI. In Ready mode, the IC is ready to measure but no sample acquisition is performed. This state is useful for reducing the power consumption of the IC while also allowing for a fast transition to the Active mode. In Active mode, the IC is fully functional. The Active bit has higher priority than the Ready bit as per Table 45.

Table 45. IC mode

Active	Ready	IC mode
0	0	Standby
0	1	Ready
1	x	Active

7.16 CTRL_REG2 (0x14)

This register enables and assigns the output pin(s) and logic polarities for the various interrupt sources available on FXAS21000.

Table 46. CTRL_REG2 register

Bit	7	6	5	4	3	2	1	0
Read	INT_CFG_FIFO	INT_EN_FIFO	INT_CFG_RT	INT_EN _RT	INT_CFG_DRDY	INT_EN_DRDY	IPOL	PP_OD
Write								
Reset	0	0	0	0	0	0	0	0

Table 47. Interrupt Enable register descriptions

Register	Description
INT_CFG_FIFO	FIFO interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
INT_EN_FIFO	FIFO Interrupt Enable 0: FIFO interrupt disabled 1: FIFO interrupt enabled
INT_CFG_RT	Rate threshold interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin

Table continues on the next page...

Table 47. Interrupt Enable register descriptions (continued)

Register	Description
INT_EN_RT	Rate threshold interrupt enable 0: Rate threshold interrupt disabled 1: Rate threshold interrupt enabled
INT_CFG_DRDY	Data-ready interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
INT_EN_DRDY	Data ready interrupt enable 0: Data-ready interrupt disabled 1: Data-ready interrupt enabled
IPOL	Interrupt logic polarity 0: Active low 1: Active high
PP_OD	INT1 and INT2 pin output driver configuration 0: Push-pull output driver 1: Open-drain output driver

Table 48. INT pin behavior as a function of PP_OD and IPOL bit settings

INT pin configuration	PP_OD	IPOL	INT asserted value	INT deasserted value
CMOS output	0	0	0	1
CMOS output	0	1	1	0
External pull-up resistor added	1	0	0	high-z[1]
External pull-down resistor added	1	1	1	high-z[1]

1. High-z = tri-state (high impedance input) condition; the state of the INT pin will be defined by the external pull-up or pull-down resistor.

NOTE

High-z = tri-state (high impedance input) condition; the state of the INT pin will be defined by the external pull-up or pull-down resistor.

8 Printed Circuit Board Layout and Device Mounting

Printed Circuit Board (PCB) layout and device mounting are critical portions of the total design. The footprint for the surface mount packages must be the correct size as a base for a proper solder connection between the PCB and the package. This, along with the recommended soldering materials and techniques, will optimize assembly and minimize the stress on the package after board mounting.

Freescale application note AN4530, "QFN (Quad Flat Pack No-Lead)" discusses the QFN package used by the FXAS21000.

8.1 Printed Circuit Board Layout

The following recommendations are a guide to an effective PCB layout. See Figure 18 for footprint dimensions.

- The PCB land should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 18.
- No additional via pattern underneath package.
- No components or vias should be placed at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on the NC pads in order to have same length of exposed trace for all pads.
- No copper traces should be on the top layer of the PCB under the package. This will cause planarity issues with board mount. Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

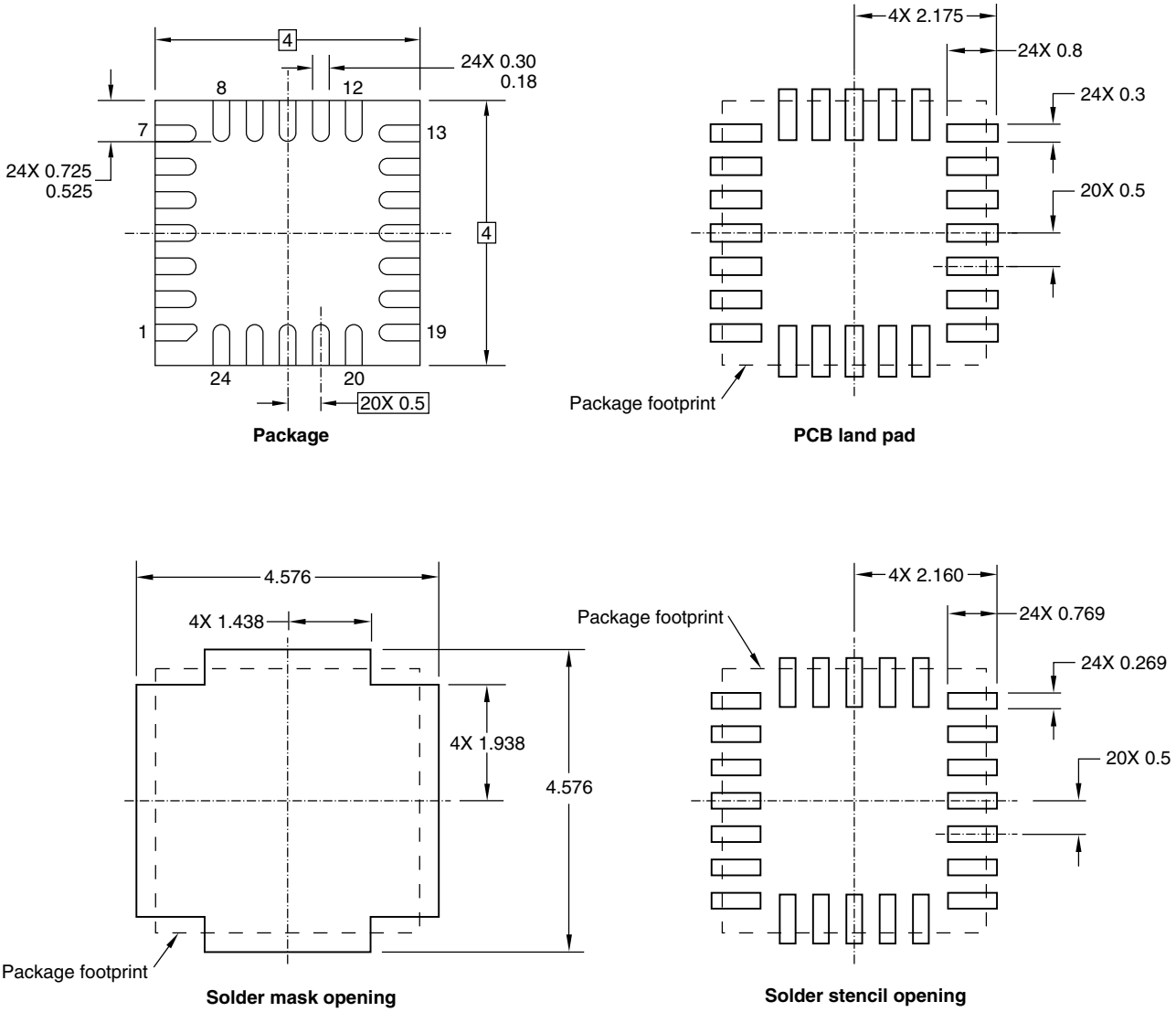


Figure 18. Footprint

8.2 Overview of Soldering Considerations

Information provided here is based on experiments executed on QFN devices. These experiments cannot represent exact conditions present at a customer site. Therefore, information herein should be used for guidance only. Process and design optimizations are recommended to develop an application-specific solution. With the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

- Stencil thickness is 100 or 125 µm.

- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.
- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Do not use a screw-down or stacking to mount the PCB into an enclosure. These methods could bend the PCB, which would put stress on the package.

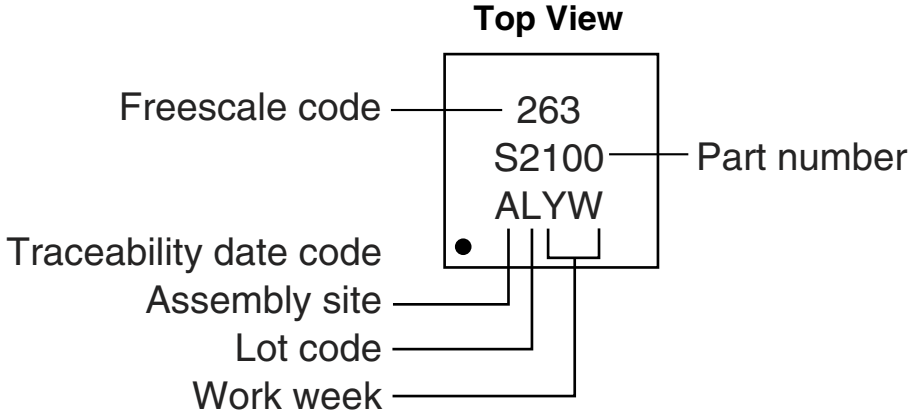
8.3 Halogen Content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembled package will contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

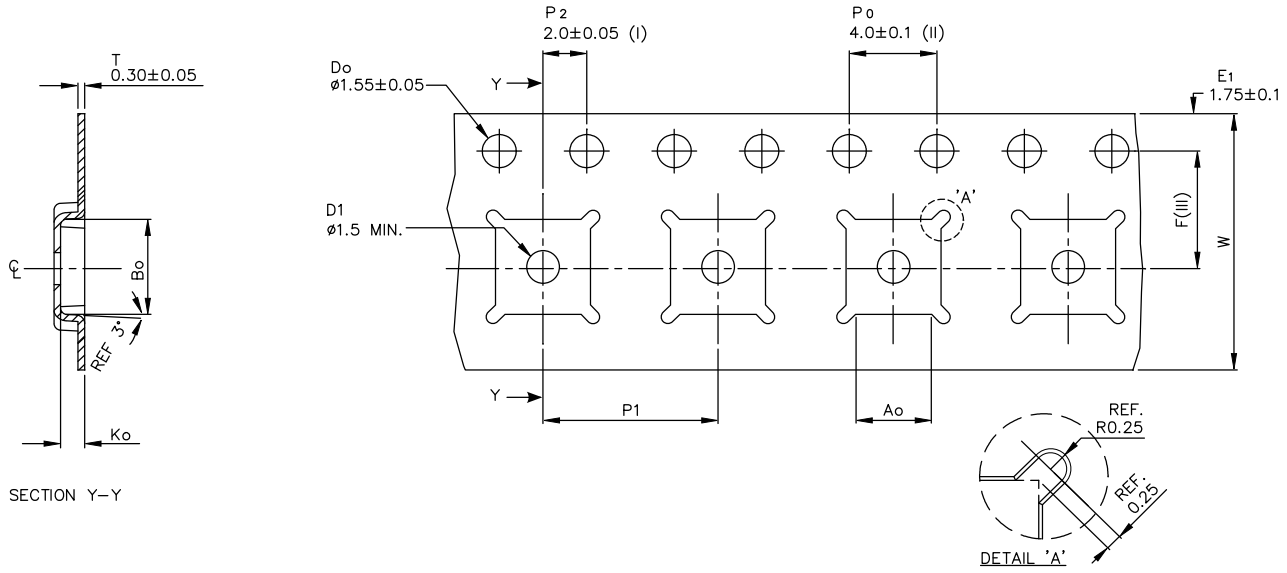
9 Package Information

The FXAS21000 platform uses a 24-lead QFN package, case number 2209-01.

9.1 Product Identification Markings



9.2 Tape and Reel Information



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.05
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
(V) Typical SR value Max 10^9 OHM/SQ
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Figure 19. Tape dimensions

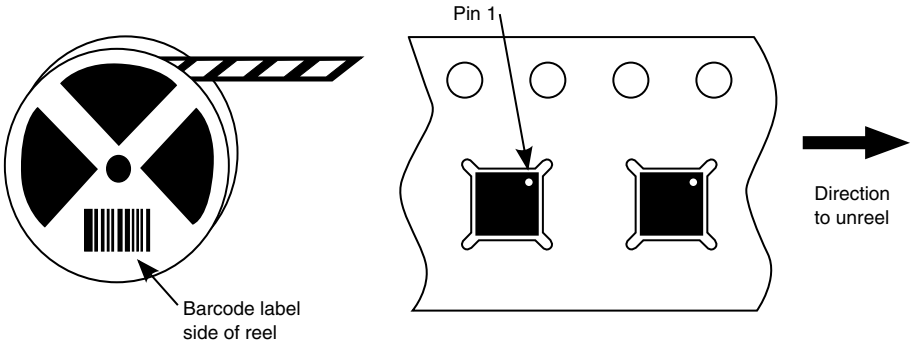
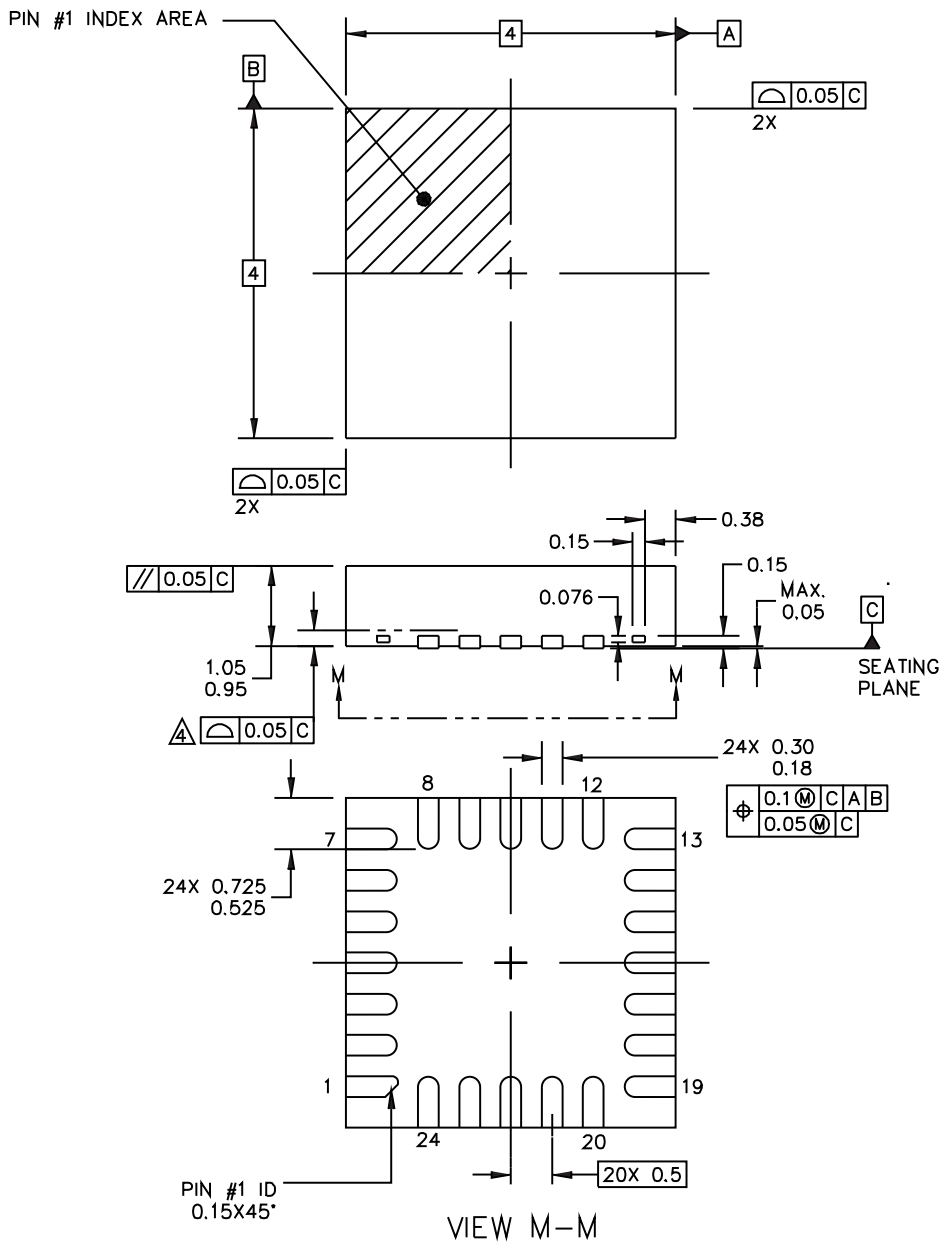


Figure 20. Tape and reel orientation

9.3 Package Description



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

This drawing is located at freescale.com.

10 Revision History

Revision number	Revision date	Description
1.0	09/2013	Initial release of document
1.1	10/2013	Register address map, Comments column, 5:0 was 7:2 (3 plcs) RT_THS register table, THS[6:0] was THS[6:3] Electrical Characteristics, Idd_{Rdy}, Typ, 4.8 was 3.8

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Document Number FXAS21000
Revision 1.1, 10/2013