PUSB2X4Y

ESD protection for high-speed interfaces

Rev. 1 — 5 November 2013 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as USB 2.0 ports against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for high-speed signal lines. It is encapsulated in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of 0.85 pF maximum. This configuration provides protection to downstream components from ESD voltages up to ±12 kV contact according to IEC 61000-4-2, level 4.

1.2 Features and benefits

- System ESD protection for USB 2.0
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±12 kV according to IEC 61000-4-2, level 4
- Line capacitance of 0.85 pF maximum for each channel

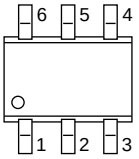
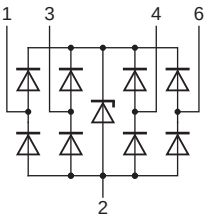
1.3 Applications

The device is designed for receiver and transmitter port protection in:

- Portable devices
- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	ESD protection for I/O signals		
2	ground		
3	ESD protection for I/O signals		
4	ESD protection for I/O signals		
5	n.c.		
6	ESD protection for I/O signals		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB2X4Y	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 3. Marking codes

Type number	Marking code[1]
PUSB2X4Y	PK*

[1] * = placeholder for manufacturing site code.

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	pins 1, 3, 4 and 6 to ground; IEC 61000-4-2, level 4			
		contact discharge	–12	+12	kV
		air discharge	–15	+15	kV
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA		6	-	9	V
I_{RM}	reverse leakage current	per channel; V_I = 5 V		-	-	1	μA
V_F	forward voltage	I_I = 1 mA		-	0.7	-	V
C_{line}	line capacitance	f = 1 MHz	[1]				
		V_I = 0 V		-	0.7	0.85	pF
		V_I = 2.5 V		-	0.55	0.75	pF
ΔC_{line}	line capacitance difference	f = 1 MHz; V_I = 2.5 V	[1]	-	-	0.1	pF
r_{dyn}	dynamic resistance	surge	[2]				
		positive transient		-	0.30	-	Ω
		negative transient		-	0.21	-	Ω
		TLP	[3]				
		positive transient		-	0.35	-	Ω
		negative transient		-	0.21	-	Ω
V_{CL}	clamping voltage	positive transient	[2]				
		I_{PP} = 4.5 A		-	3.8	-	V
		negative transient					
		I_{PP} = –5.2 A		-	–2.1	-	V

[1] This parameter is guaranteed by design.

[2] According to IEC 61000-4-5 (8/20 μs current waveform).

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.

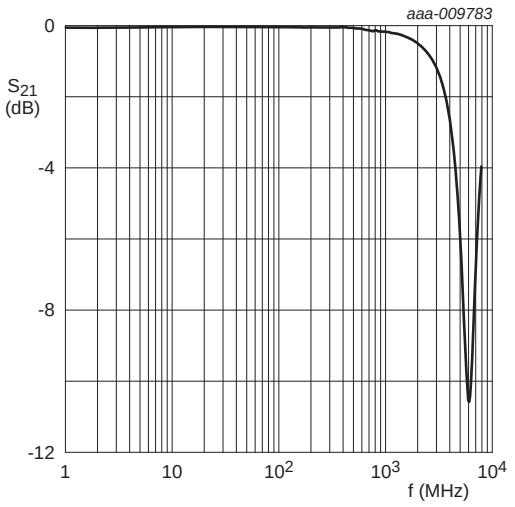


Fig 1. Insertion loss; typical values

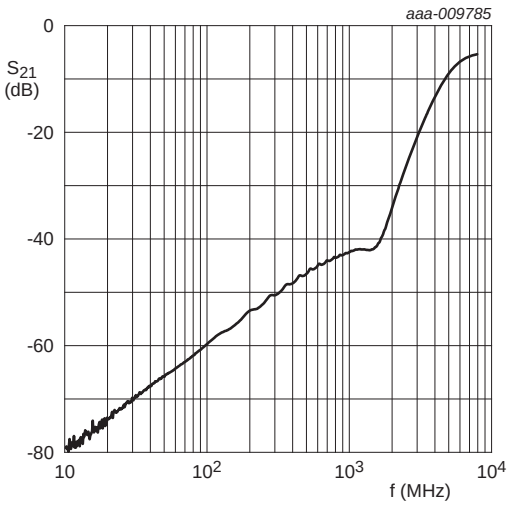
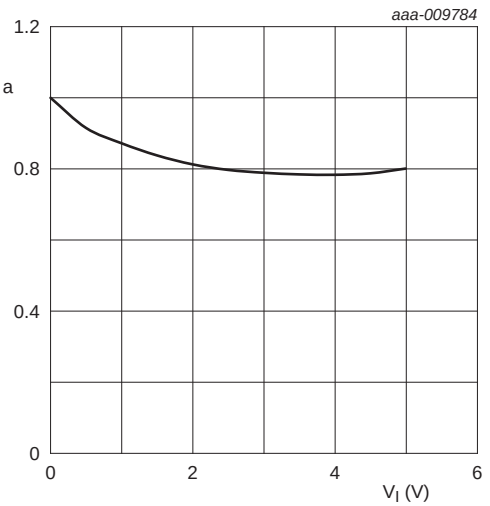
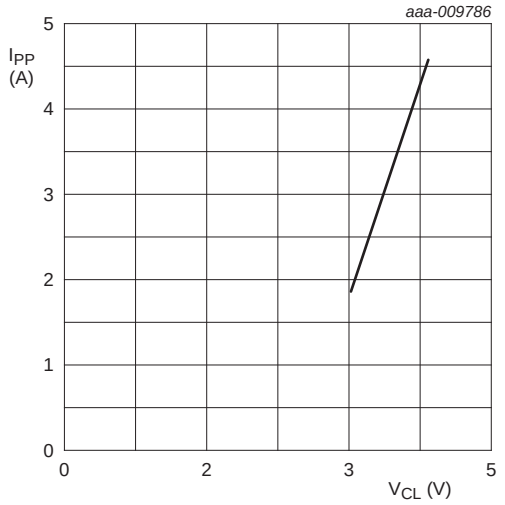


Fig 2. Crosstalk; typical values



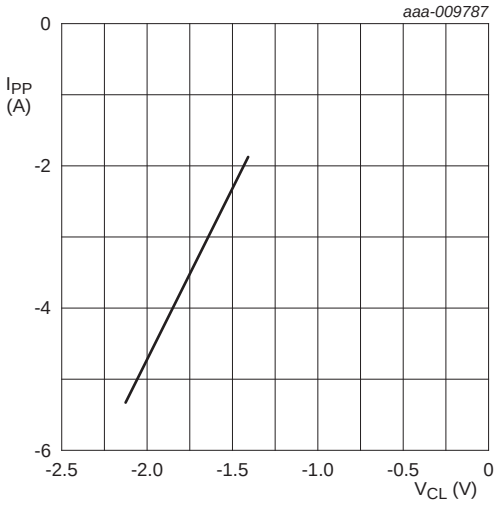
$$a = \frac{C_{line}}{C_{line(V_I = 0\ \mathrm{V})}}$$

Fig 3. Relative capacitance as a function of input voltage; typical values



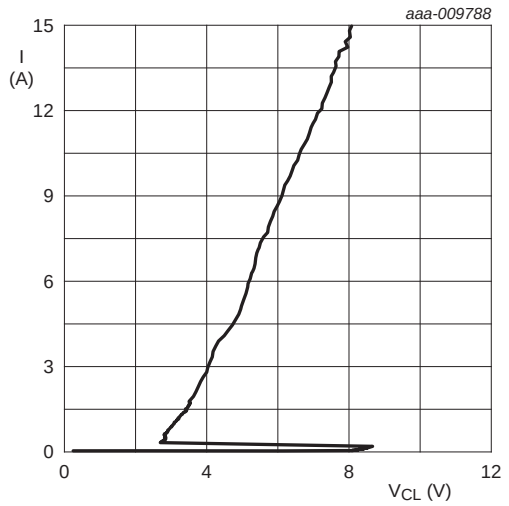
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 4. Dynamic resistance with positive clamping; typical values



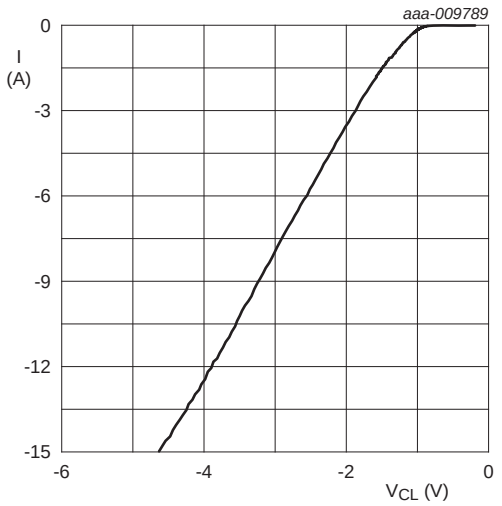
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 5. Dynamic resistance with negative clamping, typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 6. Dynamic resistance with positive clamping, typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure, which shows a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

7. Package outline

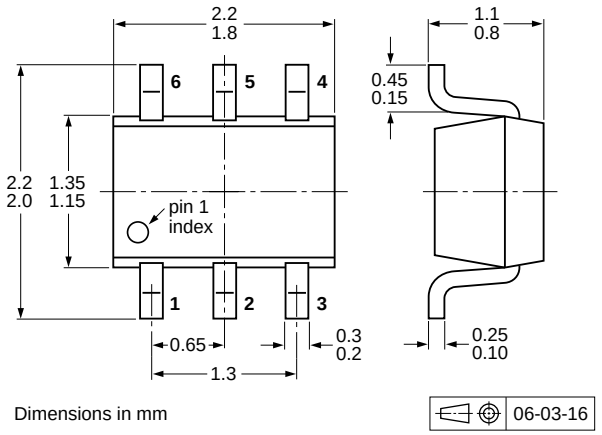


Fig 8. Package outline SOT363 (SC-88)

8. Soldering

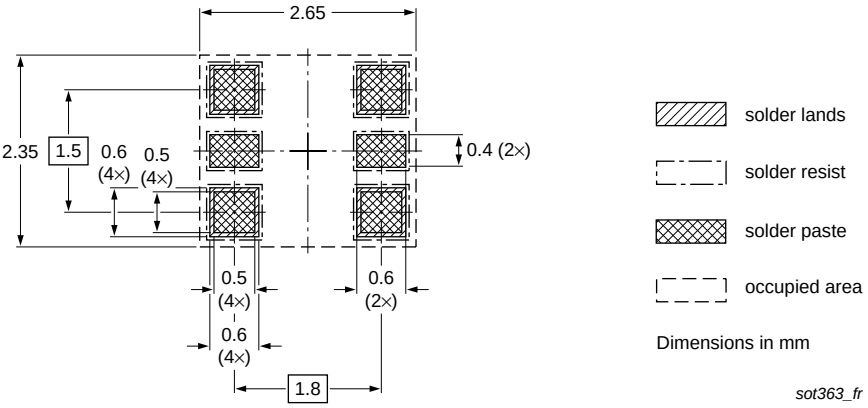


Fig 9. Reflow soldering footprint SOT363 (SC-88)

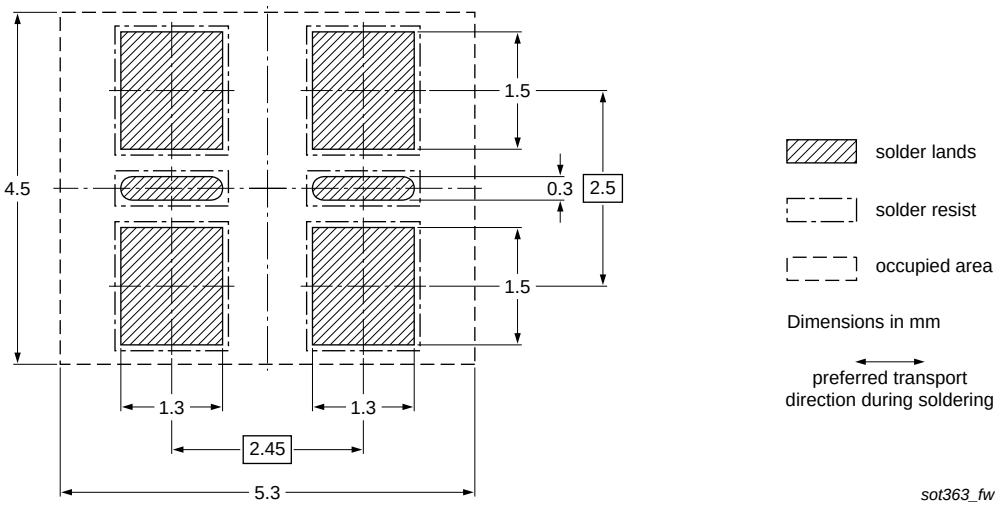


Fig 10. Wave soldering footprint SOT363 (SC-88)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB2X4Y v.1	20131105	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

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