STH180N10F3-2

N-channel 100 V, 3.9 mΩ, 180 A, H²PAK-2 STripFET™III Power MOSFET

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D
STH180N10F3-2	100 V	4.5 mΩ	180 A

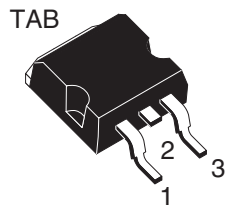
- Ultra low on-resistance
- 100% avalanche tested

Applications

- High current switching applications

Description

This device is an N-channel enhancement mode Power MOSFETs produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.



H²PAK-2

Figure 1. Internal schematic diagram

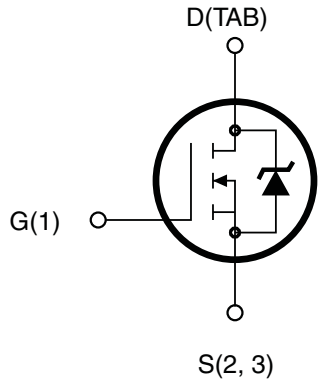


Table 1. Device summary

Order codes	Marking	Package	Packaging
STH180N10F3-2	180N10F3	H²PAK-2	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	180	A
I_D (1)	Drain current (continuous) at T_C=100°C	120	A
I_{DM} (2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_C = 25°C	315	W
	Derating factor	2.1	W/°C
dv/dt	Peak diode recovery voltage slope	20	V/ns
E_{AS} (3)	Single pulse avalanche energy	350	mJ
T_j T_{stg}	Operating junction temperature storage temperature	- 55 to 175	°C

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting Tj = 25 °C, I_D = 80 A, V_{DD} = 50 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	0.48	°C/W
Rthj-pcb(1)	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on FR-4 board, on 1inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS}= max rating, V_{DS}= max rating, @125°C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 60 A		3.9	4.5	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	6665 786 49	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 50 V, I_D = 120 A, V_{GS} = 10 V (see *Figure 14*)	-	114.6 38.8 31.9	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 50 V, I_D = 60 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 13*, *Figure 18*)	-	25.6 97.1 99.9 6.9	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		180 720	A A
V_{SD}(2)	Forward on voltage	I_{SD}=120 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=120 A, di/dt = 100 A/µs, V_{DD}=80 V, Tj=150°C (see *Figure 15*)	-	83.4 295.7 7.1		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

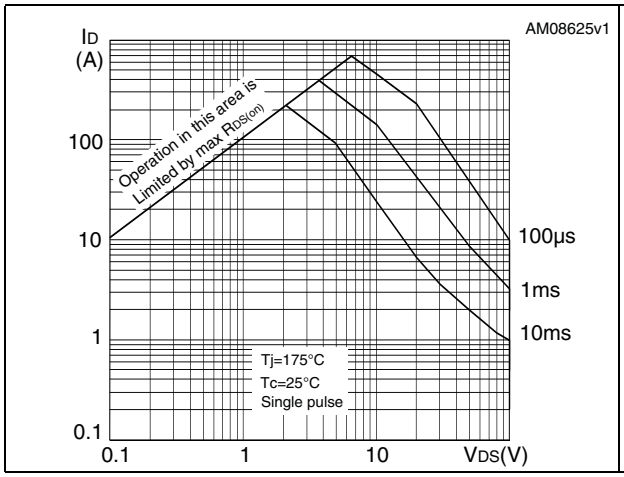


Figure 3. Thermal impedance

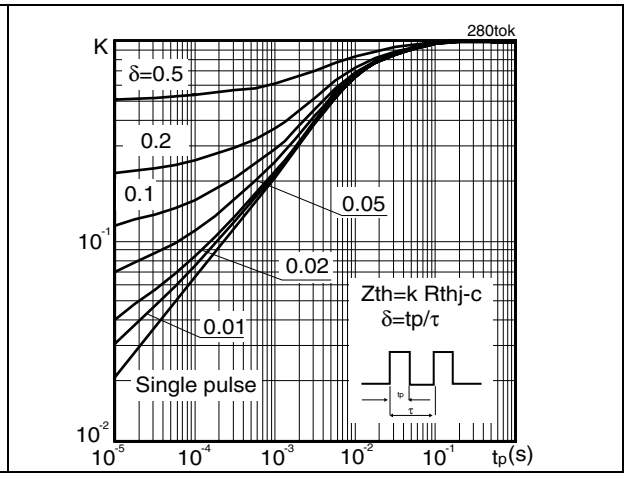


Figure 4. Output characteristics

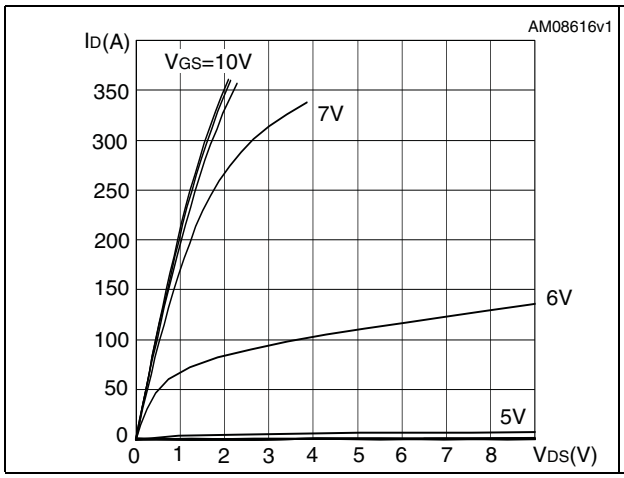


Figure 5. Transfer characteristics

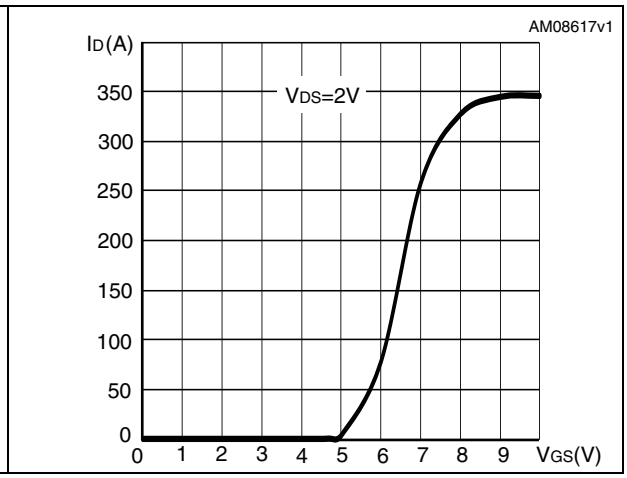


Figure 6. Normalized B_{VDSS} vs temperature

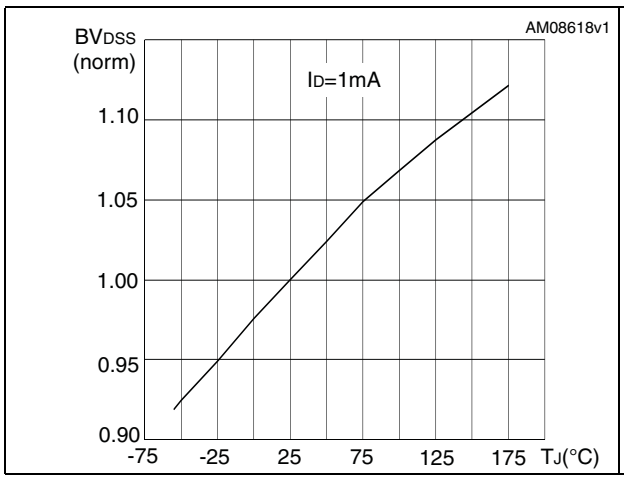


Figure 7. Static drain-source on resistance for H²PAK

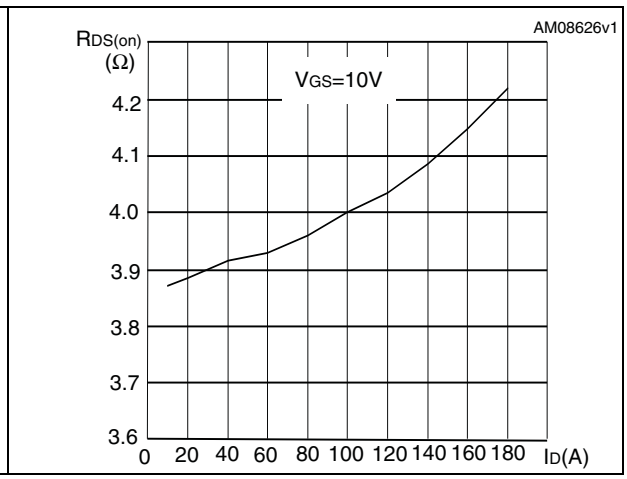


Figure 8. Gate charge vs gate-source voltage

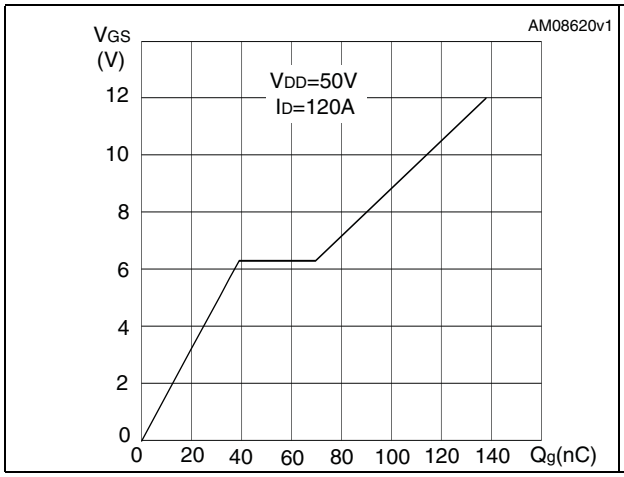


Figure 9. Capacitance variations

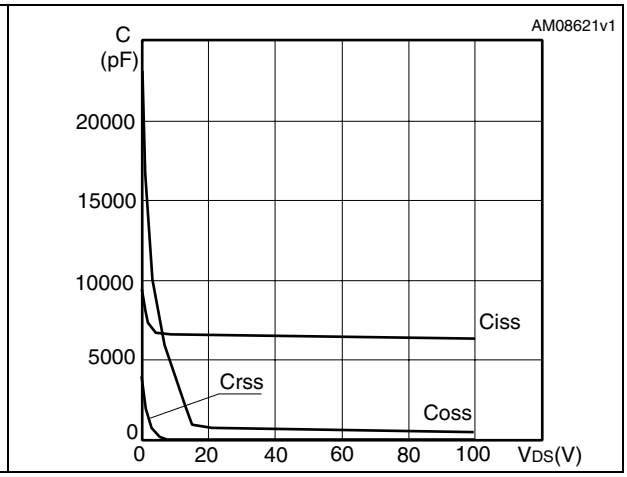


Figure 10. Normalized gate threshold voltage vs temperature

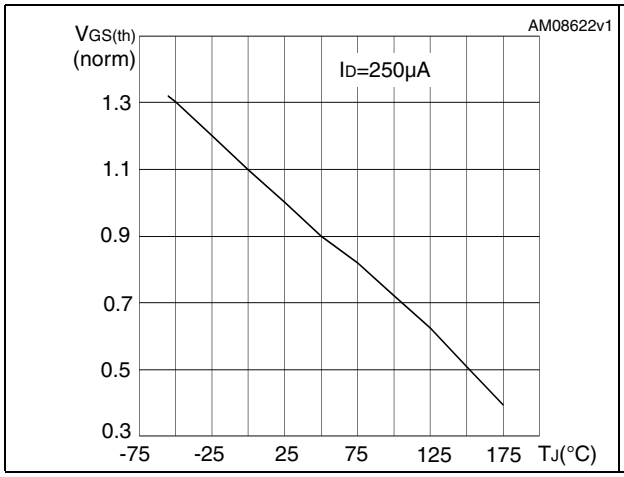


Figure 11. Normalized on resistance vs temperature

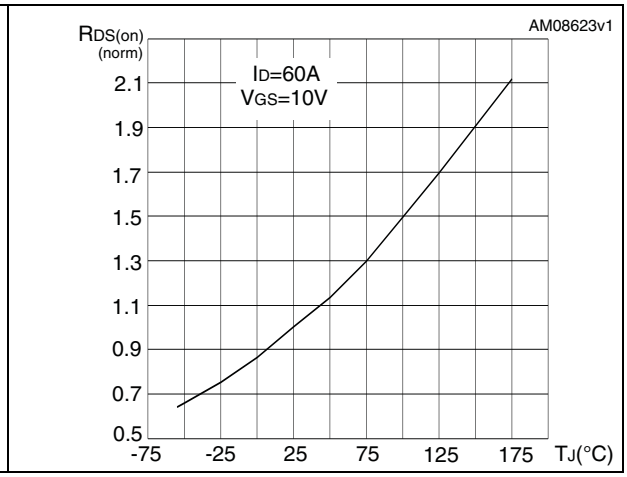
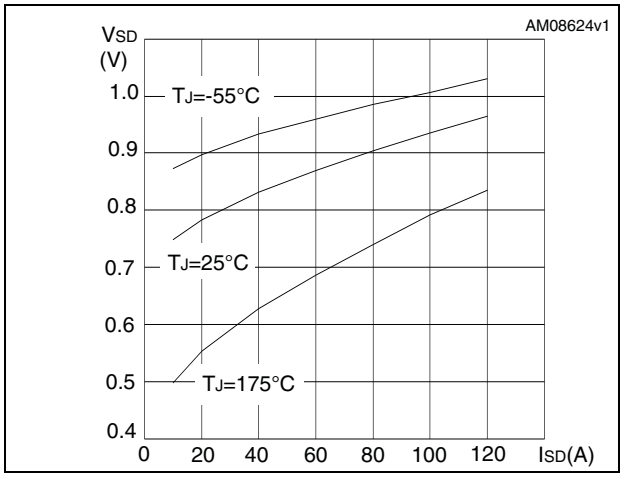


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

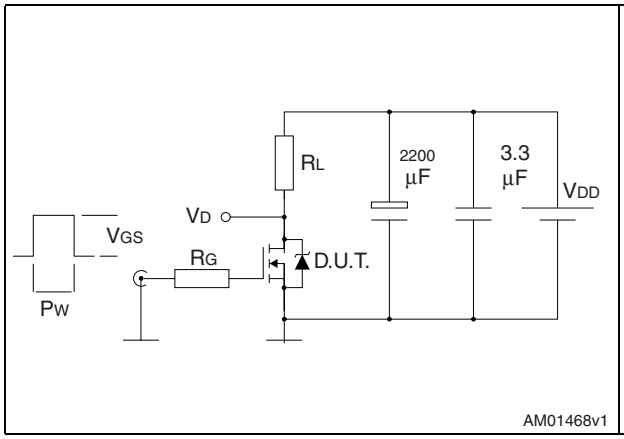


Figure 14. Gate charge test circuit

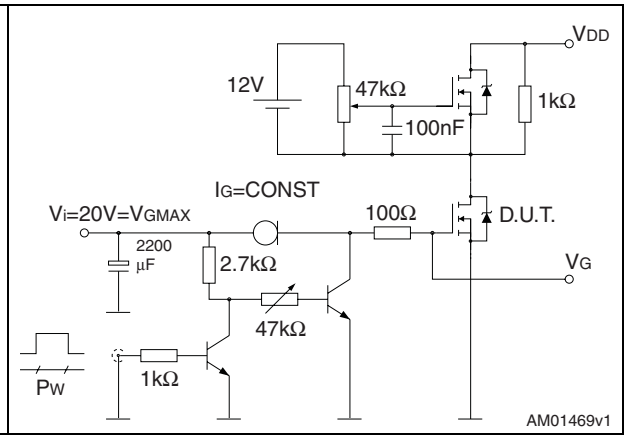


Figure 15. Test circuit for inductive load switching and diode recovery times

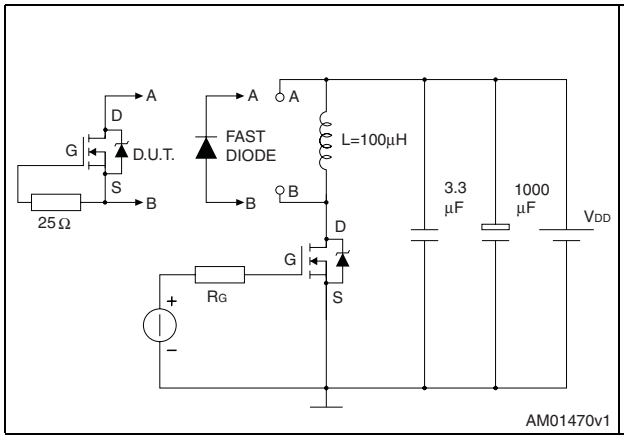


Figure 16. Unclamped inductive load test circuit

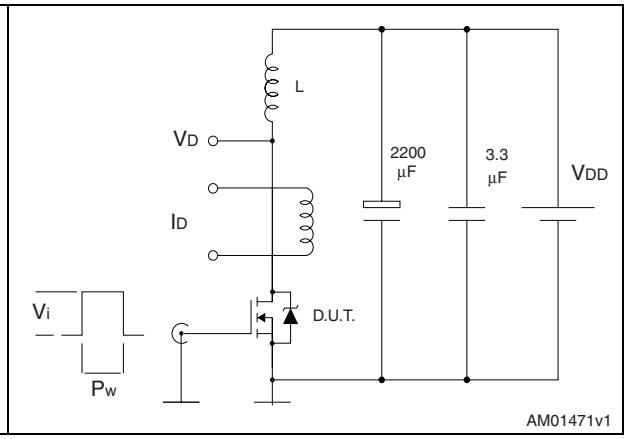


Figure 17. Unclamped inductive waveform

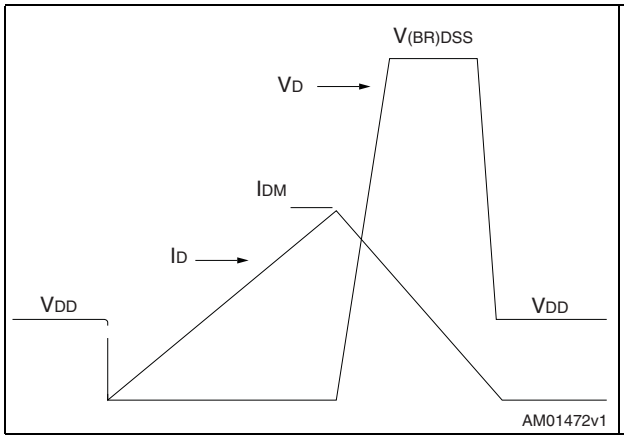
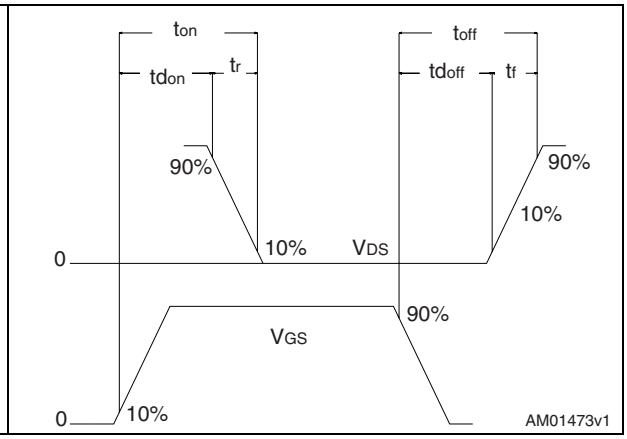


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 19. H²PAK-2 drawing

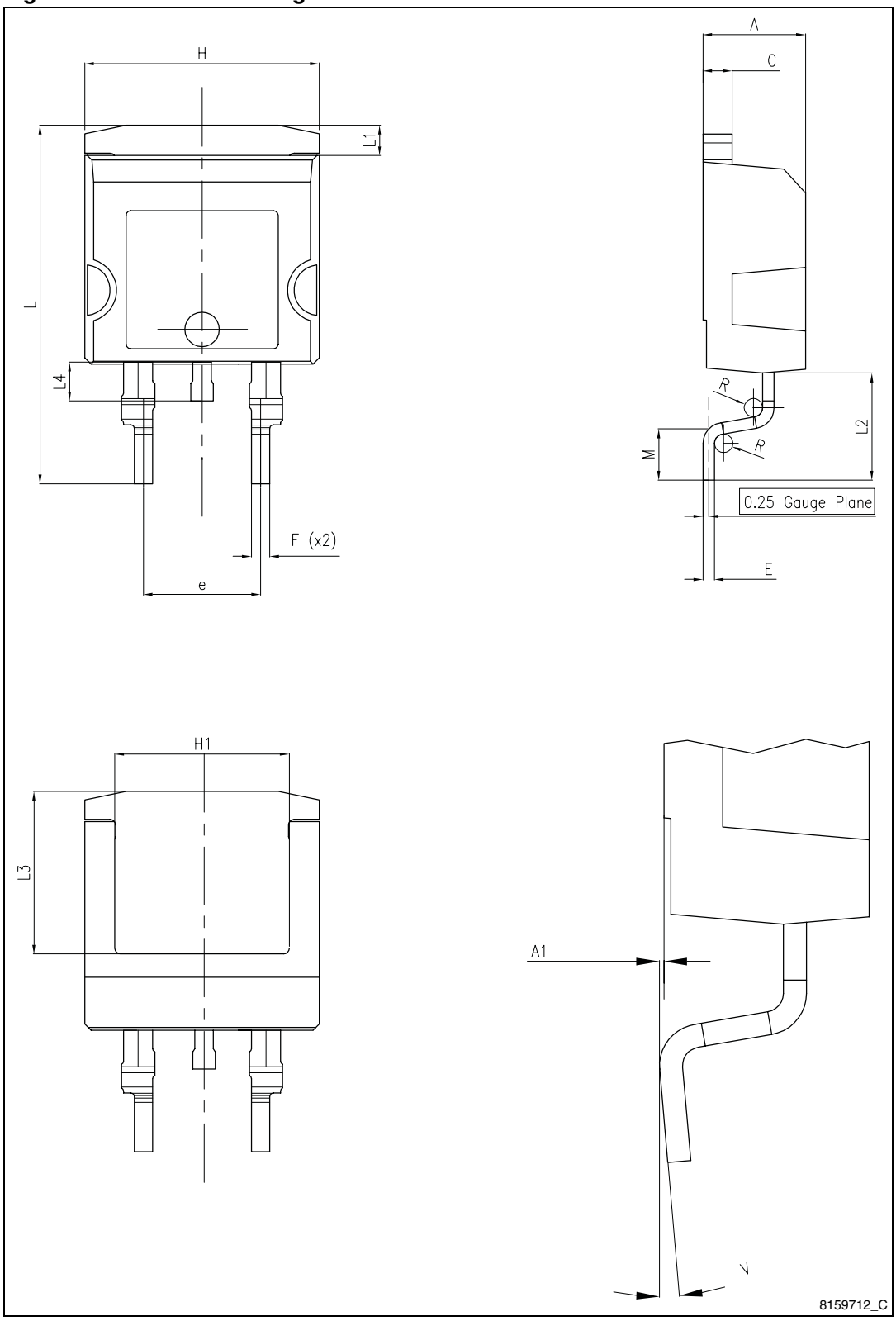
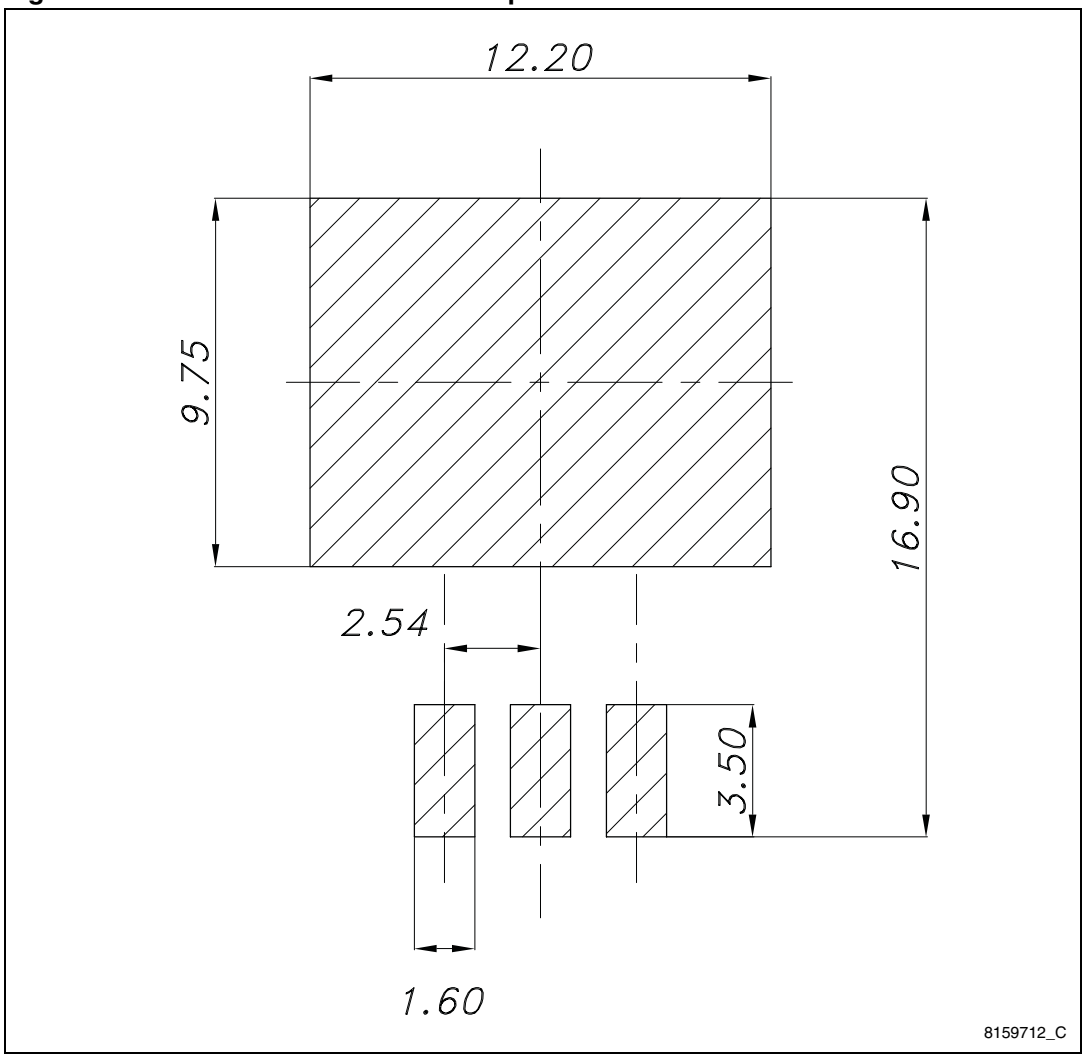


Figure 20. H²PAK-2 recommended footprint

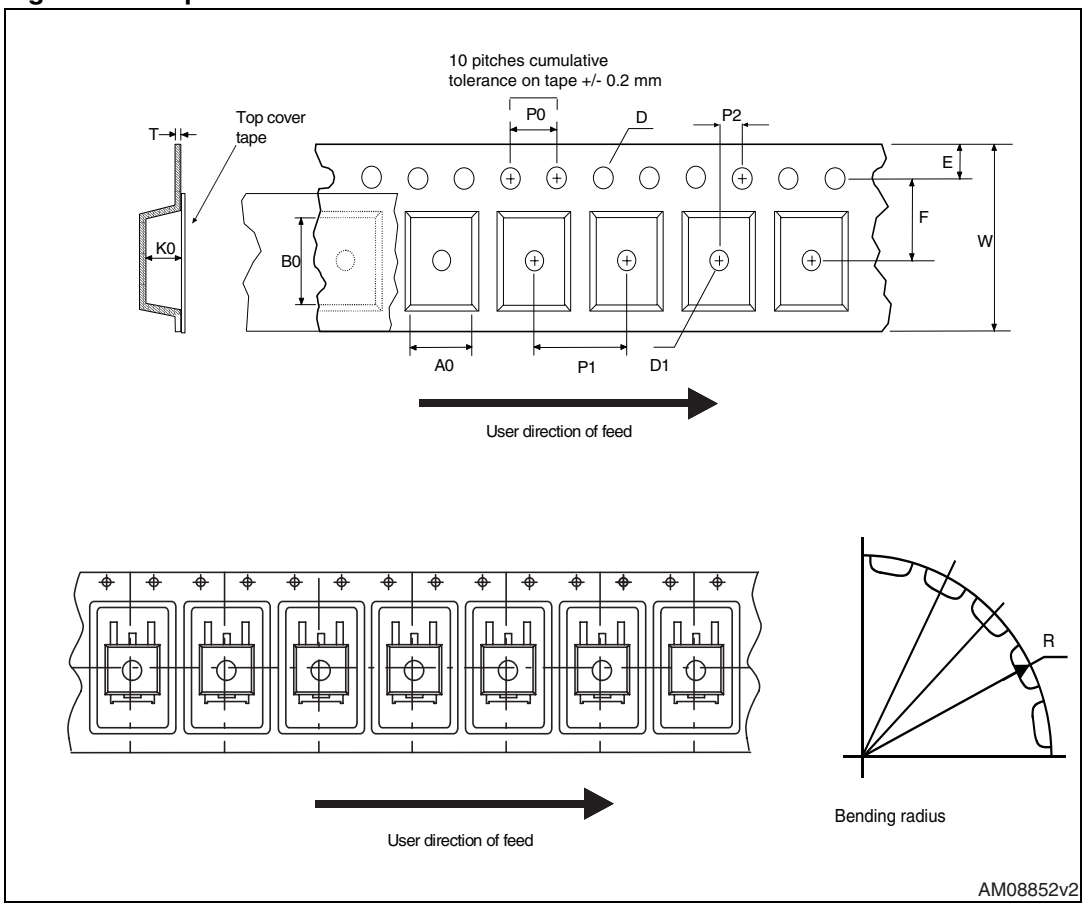


5 Packaging mechanical data

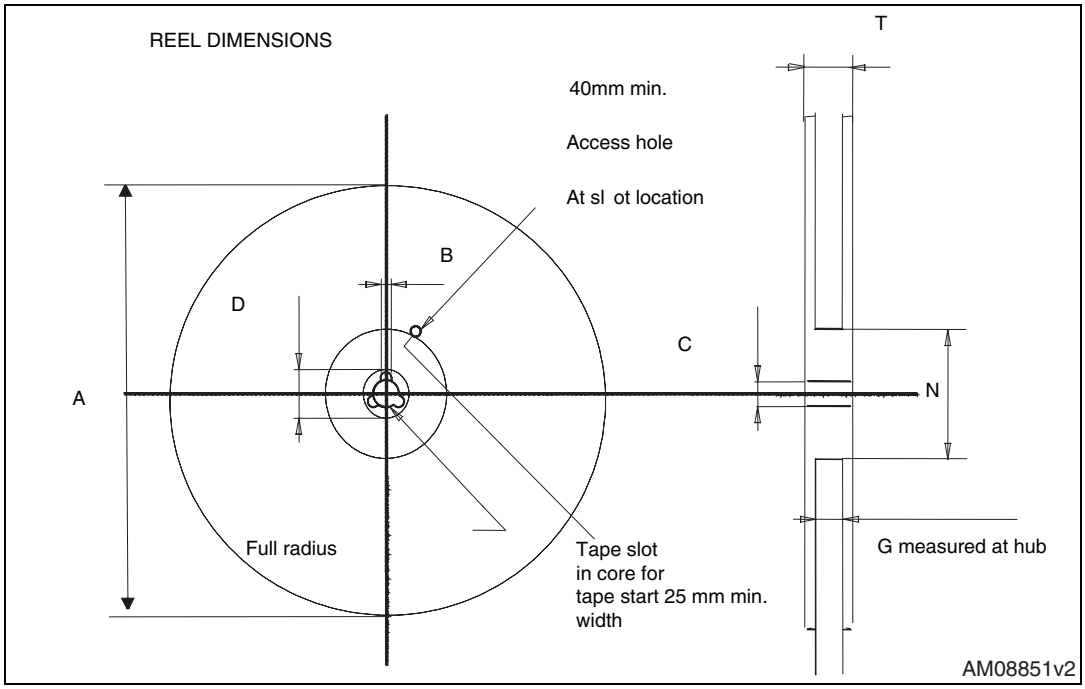
Table 9. H²PAK-2 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 21. Tape



Reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
18-Jul-2011	1	First version.

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