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T4240RDB Quick Start Guide

1 Introduction

The QorIQ T4240 reference system (T4240RDB) is a flexible system that supports the 24-virtual core T4240 processor. The T4240RDB main board is mounted in a 1U rack-mounted chassis. The T4240RDB supports clocking configuration flexibility to change the device frequency. Two expansion slots are also provided for adding standard PCIe cards. The T4240RDB comes with a Linux® board support package (BSP) that provides a comprehensive starting point for Linux development efforts.

The part number of the T4240 reference design board (RDB) system is T4240RDB-16GPA (for a board based upon T4240 Rev 1.0 silicon) and T4240RDB-PB (for a board based upon T4240 Rev 2.0 silicon).

After reading this document, you will be familiar with:

- Board configuration settings (frequency, boot location, and, T4240 or T4160 personality selection).
- How to get started and boot uboot and Linux.

Contents

2 References

The documents below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

- *T4240 QorIQ Integrated Multicore Communications Processor Family Reference Manual* (document T4240RM)
- *T4240 QorIQ Integrated Multicore Communications Processor Family Data Sheet* (document T4240)

3 Preparing board

The figure below shows the front panel of the T4240RDB.

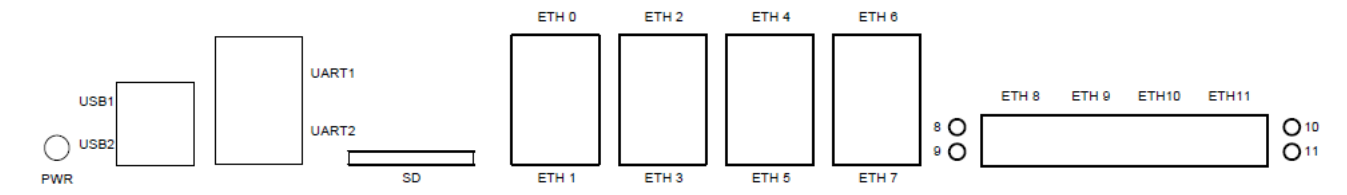

Figure 1. T4240RDB front panel

The steps to prepare the T4240RDB for use are:

1. Ensure that the power switch is off.
2. Set switch and jumper header settings.
3. Default Configuration: CPU: 1.666GHz, DDR: 1600MHz
4. Attach an RS-232 cable between the T4240RDB UART1 port and host computer.
5. Open a serial console tool on the host computer to communicate with the T4240RDB.
6. Configure the host computer's serial port with the following settings:
   - Data rate: 115200 bps
   - Number of data bits: 8
   - Parity: None
   - Number of stop bits: 1
   - Flow control: Hardware/None
7. Switch on the power button on the front side of the chassis. The board will boot and show the u-boot console messages.

```
U-Boot 2013.01-gecbda14-dirty (Jul 31 2013 - 11:06:06)


CPU0: T4240E, Version: 1.0, (0x82480010)
Core: E6500, Version: 1.0, (0x80400010)
Clock Configuration:
 CPU0:1666.667 MHz, CPU1:1666.667 MHz, CPU2:1666.667 MHz,
CPU3:1666.667 MHz,
 CPU4:1666.667 MHz, CPU5:1666.667 MHz, CPU6:1666.667 MHz, CPU7:1666.667
MHz,
 CPU8:1666.667 MHz, CPU9:1666.667 MHz, CPU10:1666.667 MHz,
CPU11:1666.667 MHz,
 CCB:666.667 MHz,
 DDR:800 MHz (1600 MT/s data rate) (Asynchronous), IFC:166.667 MHz
 FMAN1: 466.667 MHz
 FMAN2: 466.667 MHz
```

```
 QMAN: 333.333 MHz
 PME: 333.333 MHz
L1:      D-cache 32 kB enabled
 I-cache 32 kB enabled
Reset Configuration Word (RCW):
 00000000: 140c0019 0c101519 00000000 00400000
 00000010: 70701053 0044bc00 0c023000 0d000000
 00000020: 00000000 ee0000ee 00000000 000287fc
      00000030: 00000000 50000000 00000000 00000038
Board: T4240RDB, SERDES Reference Clocks: SERDES1=100MHz SERDES2=156.25MHz
SERDES3=100MHz SERDES4=100MHz
I2C: ready
SPI: ready
DRAM: Initializing....using SPD
Detected UDIMM 9JSF25672AZ-2G1K1
Detected UDIMM 9JSF25672AZ-2G1K1
Detected UDIMM 9JSF25672AZ-2G1K1
4 GiB left unmapped
     DDR: 6 GiB (DDR3, 64-bit, CL=11, ECC on)
 DDR Controller Interleaving Mode: 3-way 4KB
Flash: 128 MiB
L2: 2048 KB enabled
enable l2 for cluster 1 fec60000
enable l2 for cluster 2 feca0000
Corenet Platform Cache: 1536 KB enabled
Using SERDES1 Protocol: 28 (0x1c)
Using SERDES2 Protocol: 56 (0x38)
Using SERDES3 Protocol: 2 (0x2)
Using SERDES4 Protocol: 10 (0xa)
SRIO1: disabled
SRIO2: disabled
NAND: 2048 MiB
MMC: FSL_SDHC: 0
PCIe1: Root Complex, no link, regs @ 0xfe240000
PCIe1: Bus 00 - 00
PCIe3: Root Complex, no link, regs @ 0xfe260000
PCIe3: Bus 01 - 01
In: serial
Out: serial
Err: serial
Warning: SERDES2 expects reference clock 125MHz, but actual is 156.25MHz
Net: Fman1: Uploading microcode version 106.4.9
Fman2: Uploading microcode version 106.4.9
FM1@DTSEC1 [PRIME], FM1@DTSEC2, FM1@DTSEC3, FM1@DTSEC4, FM1@TGEC1,
FM1@TGEC2, FM2@DTSEC1, FM2@DTSEC2, FM2@DTSEC3, FM2@DTSEC4,
FM2@TGEC1, FM2@TGEC2
Hit any key to stop autoboot: 0
```

The system auto boots and shows the following Linux login screen.

```
Poky 9.0 (Yocto Project 1.4 Reference Distro) 1.4 t4240rdb ttyS0

t4240rdb login: root
root@t4240rdb:~# uname -a
Linux t4240rdb 3.8.13-rt9-g7a2b5bd-dirty #5 SMP Wed Jul 31 13:45:53 CST 2013
ppc64 GNU/Linux
root@t4240rdb:~#
```

4 SDK information

To access the SDK information on your Linux or Windows® based machine, follow these steps.

To mount an ISO image on a Linux based machine:

1. Locate the `QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso` image file in the SW image directory of the USB memory stick.

2. Copy the ISO file to your Documents folder or to your preferred location.
3. Open a new terminal using the keyboard shortcut, `Ctrl-Alt-T`.
4. Enter the following command at the terminal window:

```
$ sudo -i
```

5. Enter your Password.
6. Enter the following commands at the terminal window:
   a. `$ mkdir /mnt/QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso`
   b. `$ mount -o loop ISOPATH/QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso /mnt/QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso`

      Replace `ISOPATH` with the location of the ISO file.

   c. `$ mkdir ~/Documents/T4240_Documentation`
   d. `$ cp -R /mnt/QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso/* ~/Documents/T4240_Documentation`
7. Browse to the location where you extracted the ISO file and open `STARTHERE.html`.

To mount an ISO image on a Windows based machine:

1. Download and Install `7Zip`.
2. Locate the `QorIQ-SDK-V1.4-SOURCE-20130830-yocto.iso` image file in the SW image directory of the USB memory stick.
3. Copy the ISO file to your Documents folder or to your preferred location.
4. Right-click the ISO file and select **Extract Here** from the 7Zip context menu.
5. Browse to the location where you extracted the ISO file and open `STARTHERE.html`.

   The image below is a screenshot of STARTHERE.html page.

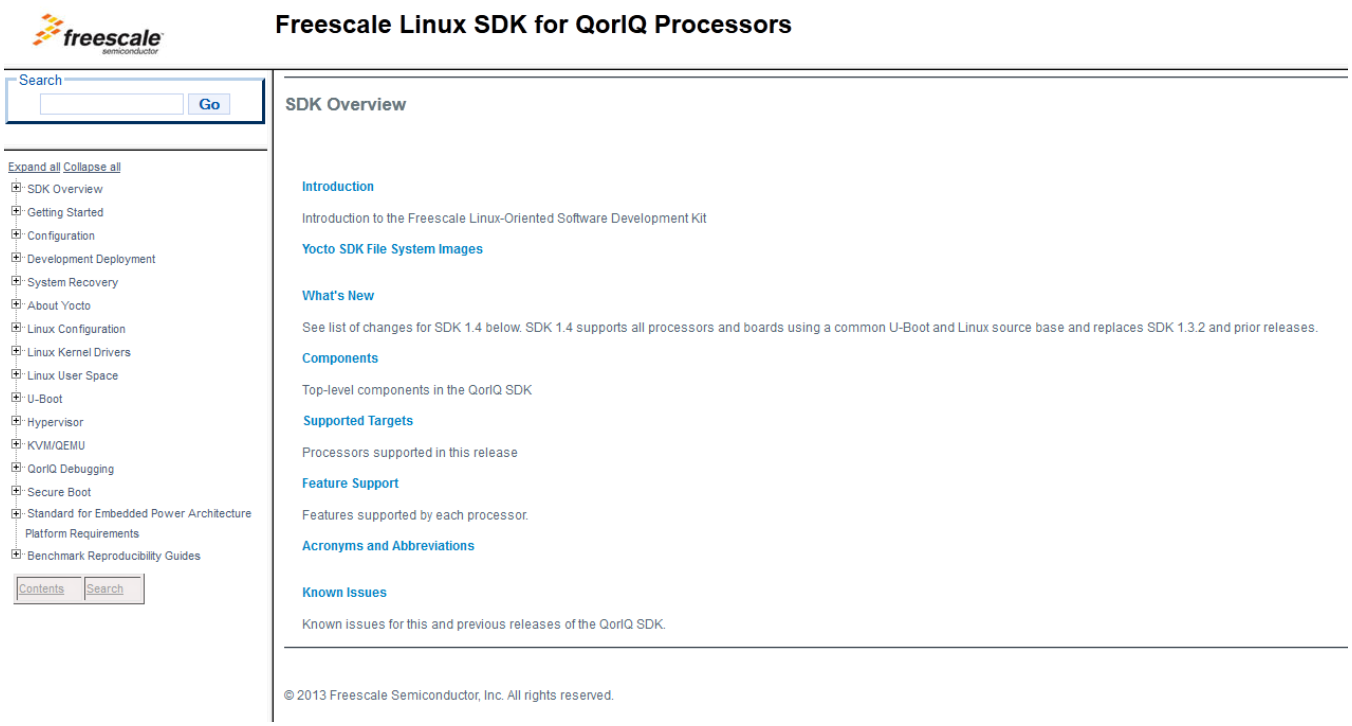

Figure 2. STARTHERE.html page

5 Removing the enclosure

To change switch or jumper settings, you need to open the board chassis. The steps to open the board chassis are:

1. Remove both screws from the top side of the chassis, as shown in the figure below.

Figure 3. Removing screws from top side of chassis

2. Remove both screws from the back side of the chassis, as shown in the figure below.

Figure 4. Removing screws from back side of chassis

3. Remove the top cover carefully.

6 System board interface

The figure below shows the top view of the T4240RDB system board interface.

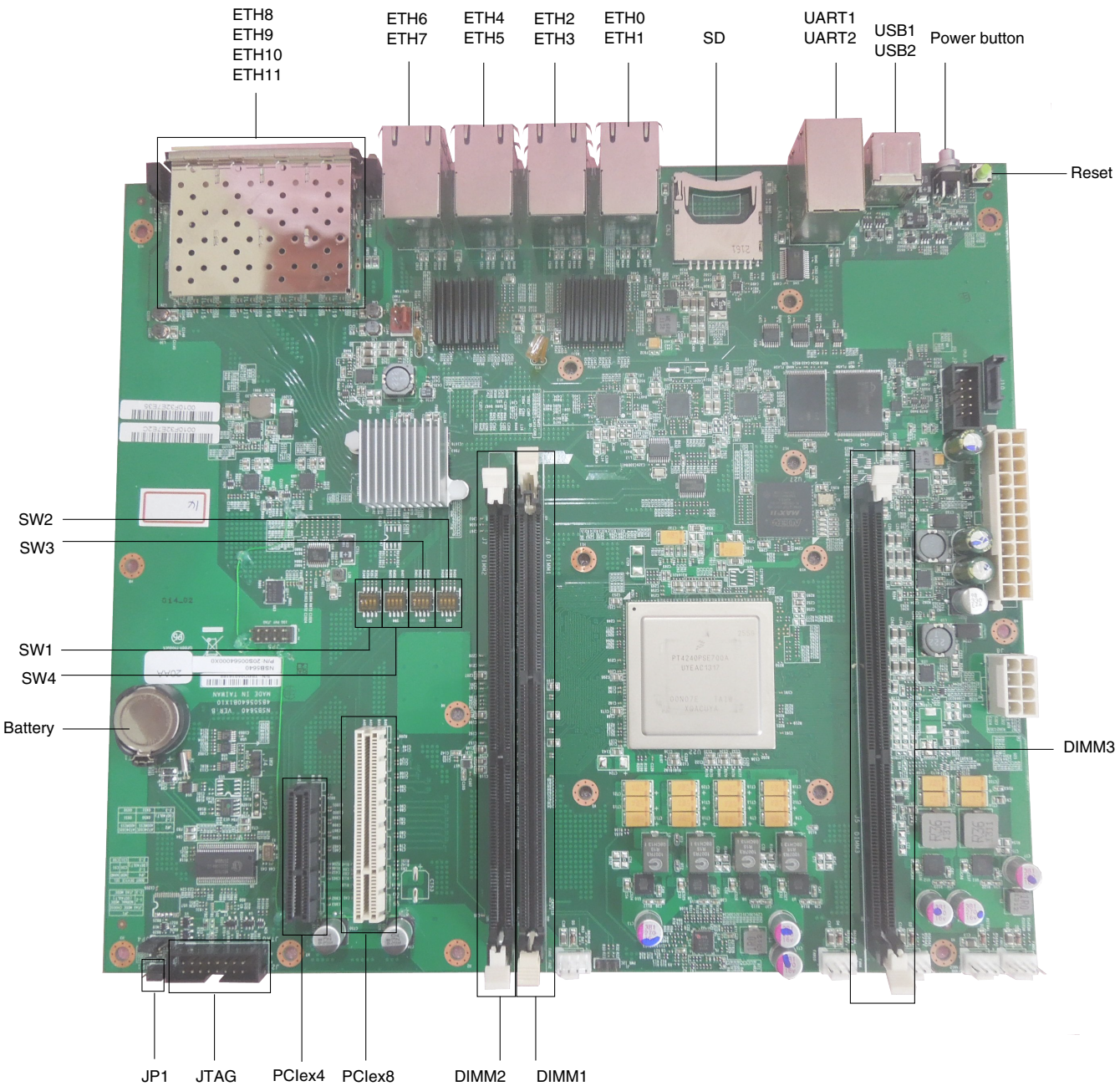

Figure 5. T4240RDB top view

6.1 Block diagram

The figure below shows a high-level block diagram of the T4240RDB.

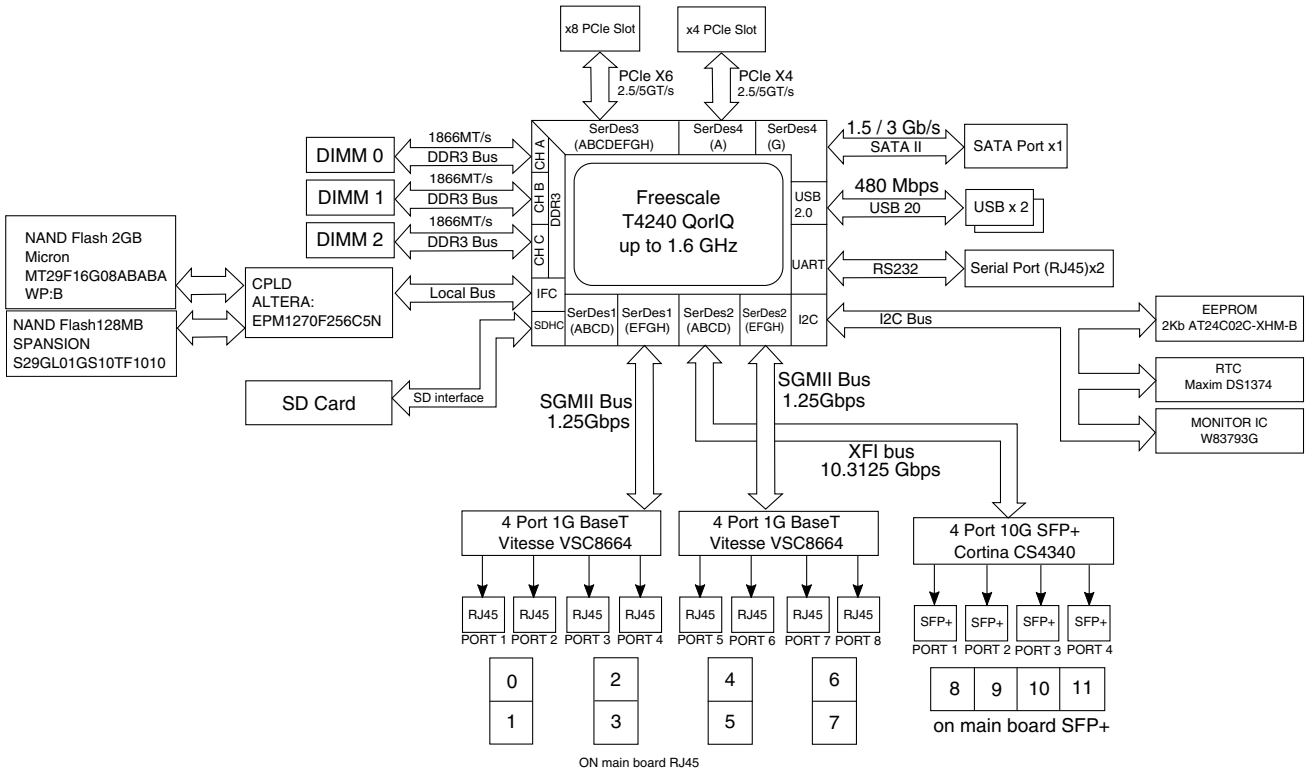

Figure 6. T4240RDB block diagram

6.2 Features

Some key features of the T4240RDB are:

- Freescale QorIQ Processing Platform
  - QorIQ T4240 Communications Processor with 24 virtual cores, 1.6 GHz
- Memory subsystem
  - DDR3 SDRAM
    - 3 DIMM slots; supports 2 GB per DIMM
    - Supports DDR3 UDIMM/RDIMM at 1600MT/s for T4240RDB-16GPA and supports 1866MT/s for T4240RDB-PB
  - NOR flash
    - 128 MB 16-bit NOR flash, SPANSION:S29GL01GS10TFI010
  - NAND flash
    - 2 GB SLC NAND flash, MICRON:MT29F16G08ABABAWP:B
  - 2 Kbit 24C02 I^2C EPPROM
  - SD connector to interface
- PCIe
  - PCIe-x4 connector
  - PCIe-x8 connector
- USB 2.0
  - One dual USB slot, connected to USB PHY

- Ethernet
  - ETH0 - ETH7: Connected to SGMII PHY - VSC8664
  - ETH8 - ETH11: Connected to XFI Quad SFP+ PHY CS4340
- UART
  - UART interface: Supports two UARTs up to 115200 bps for console display; dual RJ45 slot is used for the two UART ports
- Miscellaneous
  - LED
    - Power LED (green indicates power on; yellow indicates stand by)
    - Link LED (green indicates 1 Gbps and yellow indicates 10/100 Mbps) on each RJ45 ethernet connector
    - Active LED (green) on each RJ45 ethernet connector
  - JTAG for debugging
  - Reset: Hardware reset
  - I^2C
    - Serial EEPROM, for board identification
    - Real-time clock
- PCB
  - Power button is located at the front of the casing
  - Reset button is located inside of the casing
  - Power LED and Ethernet LED are located at the front of the casing
- Power
  - ATX Power Supply, 300W

6.3 Port map

The table below shows how ETH matches to Linux and Uboot.

Label on the Front Panel	Label in Linux	Label in Uboot
ETH0	Fm1-mac1	FM1@ DTSEC1
ETH1	Fm1-mac2	FM1@ DTSEC2
ETH2	Fm1-mac3	FM1@ DTSEC3
ETH3	Fm1-mac4	FM1@ DTSEC4
ETH4	Fm2-mac1	FM2@ DTSEC1
ETH5	Fm2-mac2	FM2@ DTSEC2
ETH6	Fm2-mac3	FM2@ DTSEC3
ETH7	Fm2-mac4	FM2@ DTSEC4
ETH8	Fm2-mac9	FM2@ TGEC1
ETH9	Fm2-mac10	FM2@ TGEC2
ETH10	Fm1-mac10	FM1@ TGEC2
ETH11	Fm1-mac9	FM1@ TGEC1

The image below shows the port map of T4240.

Figure 7. Port map

6.4 Known issues

The T4240RDB has the following known issues:

- XFI: Two 10 Gbps (ETH10, ETH11) are not working; other two 10 Gbps (ETH8 , ETH9) are working fine.

NOTE

This is a limitation of T4240 Rev 1.0 silicon, and will be resolved with Rev 2.0 silicon.

7 Default boot mode

In the T4240RDB, the boot loader, by default, executes from the NOR flash.

8 Switch settings

8.1 SW1 switch

The SW1 switch is used to control system clock (SYSCLK) and DDR reference clock (DDRCLK). The table below shows the SW1 settings for SYSCLK/DDRCLK ratio 4:1.

Table 2. SW1 Settings

4:1	CPU Speed	SYSCLK(MHz)	DDRCLK(MHz)
0000	1667	66.67	66.67
0001	1667	66.67	100
0010	1667	66.67	125
0011(Default)	1667	66.67	133.33
0100	1600	100	66.67
0101	1600	100	100
0110	1600	100	125
0111	1600	100	133.33
1000	X	125	66.67

Table continues on the next page...

Table 2. SW1 Settings (continued)

4:1	CPU Speed	SYSCLK(MHz)	DDRCLK(MHz)
1001	X	125	100
1010	X	125	125
1011	X	125	133.33
1100	1600	133.33	66.67
1101	1600	133.33	100
1110	1600	133.33	125
1111	1600	133.33	133.33

For an SW1 value in the table above, 0 indicates on and 1 indicates off.

8.2 SW2 switch

The SW2 switch is reserved for debug testing purposes and is currently not in use. For an SW2 value, 0 indicates on and 1 indicates off. The default SW2 value is 1111.

8.3 SW3 switch

The SW3 switch is reserved for RCW bank selection and is currently not in use. For an SW3 value, 0 indicates on and 1 indicates off. The default SW3 value is 1111.

Table 3. SW3 Settings

3:1	Reserved (RCW_BANK_SELECT 0~2
4	RCW_SRC_SELECT 0: RCW source from SD card 1: RCW source from EEPROM

8.4 SW4 switch

The table below shows the SW4 settings, where value 0 indicates on and value 1 indicates off.

Table 4. SW4 Settings

P1	Auto power mode 0: Normal power on 1: Normal power on/off (default)
P2	CFG_TESTSEL_B 0: T4160 mode 1: T4240 mode (default)

Table continues on the next page...

Table 4. SW4 Settings (continued)

P3	Reserved
P4	Reserved

9 Jumper settings

The jumper, JP1, is used to select JTAG mode. JP1 is shown in the figure below.

Figure 8. JP1

The table below shows the JP1 settings.

Table 5. JP1 Settings

JP1 Value	Mode
1-2	Normal mode (default)
2-3	JTAG mode

10 Revision history

This table summarizes revisions to this document.

Table 6. Revision history

Revision	Date	Description
Rev. 0	11/2013	Initial public release.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

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