CoreCommander

Reference Manual

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About this Manual

Introduction

This manual provides component details of the CoreCommander - an Embedded Development board allowing seamless IP Core integration.

Table below shows the revision history of board's reference manual.

Version	Date	Description
1.9	December 2011	• Updated Cyclone III EP3C25F256C8 Device's Architectural Feature and Value in Table 2.2
1.8	November 2011	• Modified Table 2.1
1.7	May 2009	• Added text to power up the the board from USB, External supply and Battery in the Power supply section.
1.6	April 2009	• Modified table 2.18. Replaced JP2.3 and JP2.4 with JP1.3 and JP1.4.
1.5	March 2009	• Modified FPGA Pin No. for u20_host_reset_n signal in Table 2.8. • Added u20_host_cs_n signal description in Table 2.8. • Modified FPGA Pin no for signal u20_otg_reset_n, in Table 2.9. • Added u20_otg_cs_n Signal description in Table 2.9. • Updated sdc_cmd signal direction. • Updated sdc_preset_n signal direction.
1.4	March 2009	• Modified Figure 2.1 • Renamed Power Supply Input Jumper (J2) to Power Supply (External/Battery) Input Jumper • Updated Jumper Description and Function Description in Table 2.19
1.3	February 2009	• Rectified FPGA Pin no. M11 to M15 for Key Down in table 3.3.

Version	Date	Description
1.2	February 2009	• Changed SD Card Pin No. in Table 2.14 SD Card Connector Pinout. • Changed Jumper Settiings in Table 2.18 • Replaced CON3 with CON1 in Table 3.2. LCD Display Pinout. • Updated FPGA Pin Nos. in Table 3.3 Pushbutton switch.
1.1	December 2008	Updated reference manual for CoreCommander board rev1b.
1.0	October 2008	First publication

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
- Bookmarks serve as an additional table of contents.
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Typographic Conventions

This reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: **Board Components, Featured Device.**
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: ***Figure 2-1. Cyclone III Embedded Development Board Components, Table 2-1. Cyclone III Embedded Development Board Components & Interfaces*.**
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
	The hand points to special information that requires special attention
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

Contents

1. About CoreCommander

General Description

The CoreCommander is an Embedded Development board allowing seamless IP Core integration and more. This board is packaged with the Cyclone III Embedded Development board and User Interface Board. The Cyclone III Embedded Development board includes Altera's Cyclone III FPGA to handle the programmable hardware development and is intended to be used by its users to implement IP Development acting as a low cost embedded platform. The User Interface board contains 1.7" TFT LCD and Navigation Keypad.

The CoreCommander provides a hardware platform that offers a unique opportunity to customize your development environment via expansion connectors and daughter cards as well as evaluate the feature rich, low-power Altera Cyclone III device.

For more functionality, the embedded development board can be expanded through daughter cards connected to the 40-pin, 36 GPIO connector. SLS and other Altera development kit partners has created GPIO daughter cards (with 1.3 MP CMOS Image Sensor, Fast Ethernet, 3.5" TFT LCD, etc) that allows you to expand the functionality of the board.

The main features of the CoreCommander are:

- Low-power consumption Altera Cyclone III EP3C25 chip in a 256-pin FineLine BGA (FBGA) package
- Expandable through 40-pin 36 GPIO connector
- 32-Mbyte SDRAM
- 8-Mbyte of CFI flash
- EPCS16 for configuration
- USB A type connector for USB- ULPI Interface
- USB Mini AB Type connector for USB-ULPI interface
- Micro SD connector for SD Card interface
- Two user LEDs
- 1.7" 128x160 pixel TFT LCD with GRAM (on User Interface Board)
- Six user programmable and one reset push-button switches (on User Interface Board)

The main advantages of the CoreCommander are:

- Facilitates a fast and successful FPGA design experience with helpful example designs and demonstrations.
- Directly configure and communicate with the Cyclone III device via JTAG header
- Active Serial configuration through EPCS16
- Low power consumption
- Cost-effective modular design

Figure 1-1. shows the CoreCommander angle view.

Figure 1-1. CoreCommander Angle View

Component Blocks

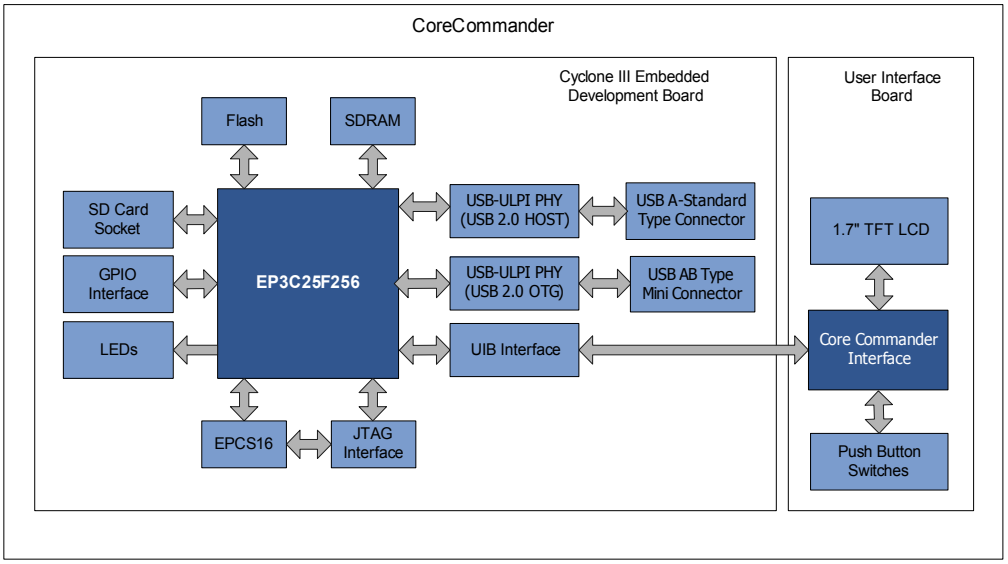
- Altera's EP3C25F256 FPGA (Cyclone III family) with lower migration support of following Cyclone III Family FPGA.
  - EP3C5F256
  - EP3C10F256
  - EP3C16F256
- 16-bit Memory Subsystem
  - 2MB Flash (Hardware Support up to 8MB)
  - 8MB SDRAM support (Hardware Support up to 32MB)
- USB 2.0 ULPI Interface (Optional)
  - High Speed Mode (480Mbit/Sec)
  - Full Speed Mode (12Mbit/Sec)
  - Low Speed Mode (1.5Mbit/Sec)
  - USB HOST
- USB 2.0 ULPI Interface (Optional)
  - High Speed Mode (480Mbit/Sec)
  - Full Speed Mode (12Mbit/Sec)
  - Low Speed Mode (1.5Mbit/Sec)
  - USB OTG
- Display
  - Active matrix TFT 1.7(Diagonal)" LCD Display
- Push button keypad for navigation and programmable input
- SD Card connector
- 16-Mbit Serial Configuration Prom (EPCS16SI16N)
- USB 2.0 Connectors
  - USB Standard A- Type connector
  - USB Mini AB connector
- General Purpose Digital Input/Output Connector
- Switches and LEDs
- System Reset Push button
- JTAG/Active Serial FPGA Programming Mode Selection
- LED indication for FPGA Programming Mode
- Clocking
  - 48.000 MHz Crystal Oscillator as a System Clock

- Power
  - USB Bus Power Input, 5V-1A
  - External Power Input, 5V-1A
  - Battery Power Input, 3.3V, 1A
- Mechanical
  - PCB Size is 4”X3” inches
  - Hand-held design

Block Diagram

Figure 1-2. below shows functional block diagram of the CoreCommander.

Figure 1-2. CoreCommander Functional Diagram



2. Cyclone III Embedded Development Board Components

This chapter provides operational and connectivity detail for the Cyclone III Embedded Development board's major components and interfaces.

The board schematic can be found at:
<*CoreCommander Installation Path*>**\board_design_files\schematics**

The default *Core Commander Installation Path* is **c:\sls\kits\corecommander**

For information on powering-up the CoreCommander and installing the demo software, refer to the *CoreCommander User Guide*.

Figure 2-1. shows the top view of the Cyclone III Embedded Development board.

Figure 2-1. Top View of the Cyclone III Embedded Development Board

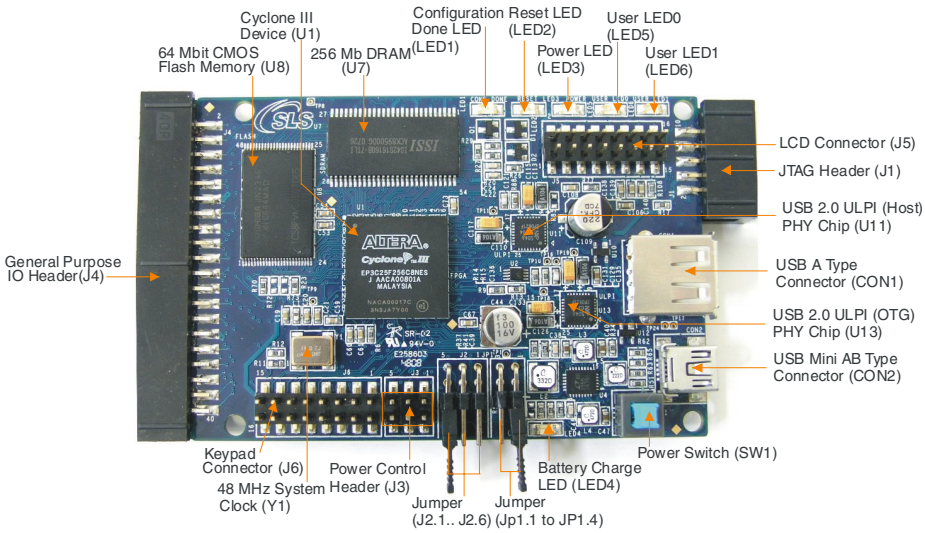


Figure 2-2. Back View of the Cyclone III Embedded Development Board

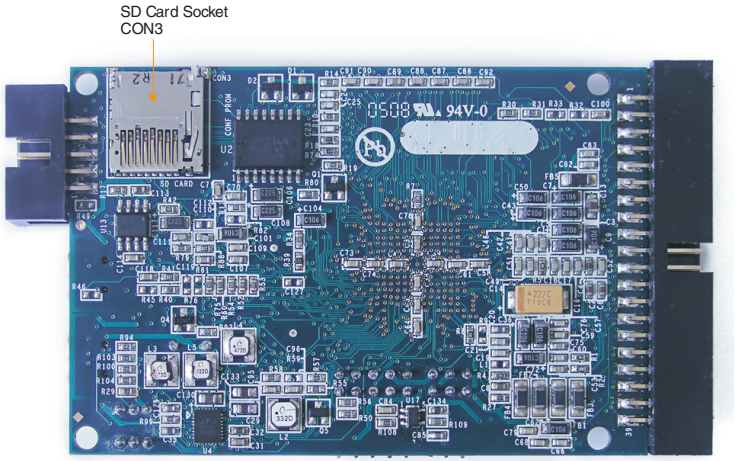


Table 2-1 describes the components and lists their corresponding board references.

Table 2-1. Embedded System Development Board Components & Interfaces

Type	Board Reference	Name	Description	Page
Featured Device				
FPGA	U1	Cyclone III Device	EP3C25F256-C8, 256-pin Fine-Line BGA (FBGA) package	8
Memory				
SDRAM	U7	256 Mb Synchronous DRAM	256 Mbit Synchronous DRAM	9
Flash	U8	64 Mb CMOS Flash Memory	64Mbit (8M × 8 BITS / 4M × 16 BITS) CMOS FLASH MEMORY	11
Configuration Memory	U3	16 Mb Serial Configuration Memory Device	16 Mbit Serial Configuration Memory Devices EPCS16	13
User Interfaces				
Output	LED1-LED5	LEDs	Config Done, on/Off Latching switches, Reset, two user LEDs	13

Table 2-1. Embedded System Development Board Components & Interfaces				
Type	**Board Reference**	**Name**	**Description**	**Page**
I/O	CON1, U11	USB A-Type Standard Connector	USB 2.0 Interface, USB-ULPI PHY	14
I/O	CON2, U13	USB AB-Type Mini Connector	USB 2.0 Interface, USB-ULPI PHY	14
I/O	J5	LCD Connector	Board-to-Board interface connector for LCD on User Interface Board	16
I/O	J6	Push Button Switch Connector	Board-to-Board interface connector for push button switches on User Interface Board	17
Input	J3	Control Function Header	Provides support for control functions	18
I/O	J1	JTAG Header	Jumper header to select which JTAG source the board uses, i.e., the JTAG header configuration or the USB JTAG configuration	19
I/O	CON3	SD Card Socket	Micro SD Card Socket	19
Expansion Interface				
I/O	J4	General Purpose I/O Header	36 General Purpose Digital Input/ Output Header	20
Clocks				
Oscillator	Y1	Crystal Oscillator	Various clock oscillators used for system clock or other dedicated devices	22
Power Supply				
Power Supply	U4, U5, U6	Power Supply Regulator	LTC3555, High Efficiency USB Power Manager and Triple Step Down DC/DC Converter and TPS 73025, TPS 73018 Texas Instruments' low-dropout linear regulator	22
Input	SW1	Power Switch	Switches the board's power on and off	24

Table 2-1. Embedded System Development Board Components & Interfaces				
Type	**Board Reference**	**Name**	**Description**	**Page**
Jumper	JP1	Power Supply Select Jumper	Jumper that selects power from available sources	24
Jumper	J2	Power Supply (External/ Battery) Input Jumper	Jumper that enables the input to the power supply circuitry	24

Featured Device

Cyclone III Device (U1)

The Cyclone III Embedded Development board features the EP3C25F256C8 device (U1) in a 256-pin FineLine BGA (FBGA) package

Table 2-2 lists Cyclone III EP3C25F256C8 device features.

Table 2-2. Cyclone III EP3C25F256C8 Device Features	
Architectural Feature	**Value**
Logic Elements	24,624
RAM	608Kbits
User I/Os	156
PLLs and banks	4 PLLs and 8 banks
Global Clock	20
Multipliers	132 9X9 Multipliers

Table 2-3 lists the Cyclone III EP3C25F256 device pin I/Os.

Table 2-3. Cyclone III Device Pin I/Os Count	
Board Component	**Pin I/Os**
SDR SDRAM	39 (3 + 36 shared)
Flash	42 (6 +36 shared)
USB 2.0 ULPI PHY Chip	13
USB 2.0 ULPI PHY Chip	13
Push button (User I/O + Reset)	7
LEDs	2 (1 + 1 shared)
LCD	13

Table 2-3. Cyclone III Device Pin I/Os Count	
Board Component	**Pin I/Os**
SD Card	7 (6 +1 shared)
GPIO	36
CLOCK	1
Total I/Os Used	155
Total EP3C25F256 pins	156
Unused I/Os	1 (Shared Configuration I/O)
Notes: (1) Total I/O count includes dual function and configuration I/Os	

Cyclone III device can be configured via the JTAG interface using an external programming cable.

Memory

The Cyclone III Embedded Development board includes the following memories:

- SDRAM
- Flash
- Serial Configuration Memory Device - EPCS16

SDRAM (U7)

This board has 256 Mb of Synchronous DRAM (SDRAM) 16 bit data bus. The target device is IS42S16160B-7, the target frequency is 143MHz and the target package is the 0.8mm pitch 54-pin TSOP.

The SDRAM interface signal names and "Type" in the table below shall be considered relative to Cyclone III device in so far as the I/O settings and direction. Table 2-4 shows the SDRAM signal name, corresponding FPGA pin, signal direction, type and board reference U7 SDRAM pin.

Table 2-4. SDRAM Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**U7 (SDRAM) Pin**
`tri_addr0`	D6	Output	+3.3V	23
`tri_addr1`	J15	Output	+3.3V	24

Table 2-4. SDRAM Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	U7 (SDRAM) Pin
tri_addr2	D1	Output	+3.3V	25
tri_addr3	F2	Output	+3.3V	26
tri_addr4	F1	Output	+3.3V	29
tri_addr5	C2	Output	+3.3V	30
tri_addr6	B1	Output	+3.3V	31
tri_addr7	A2	Output	+3.3V	32
tri_addr8	B3	Output	+3.3V	33
tri_addr9	A3	Output	+3.3V	34
tri_addr10	D5	Output	+3.3V	22
tri_addr11	B4	Output	+3.3V	35
tri_addr12	A4	Output	+3.3V	36
tri_data0	P16	Bidirectional	+3.3V	2
tri_data1	D16	Bidirectional	+3.3V	4
tri_data2	C16	Bidirectional	+3.3V	5
tri_data3	F15	Bidirectional	+3.3V	7
tri_data4	D15	Bidirectional	+3.3V	8
tri_data5	D14	Bidirectional	+3.3V	10
tri_data6	C14	Bidirectional	+3.3V	11
tri_data7	B13	Bidirectional	+3.3V	13
tri_data8	B6	Bidirectional	+3.3V	42
tri_data9	A6	Bidirectional	+3.3V	44
tri_data10	B7	Bidirectional	+3.3V	45
tri_data11	A7	Bidirectional	+3.3V	47
tri_data12	D9	Bidirectional	+3.3V	48
tri_data13	C9	Bidirectional	+3.3V	50
tri_data14	B11	Bidirectional	+3.3V	51
tri_data15	A11	Bidirectional	+3.3V	53
sdr_clk	B14	Output	+3.3V	38

Table 2-4. SDRAM Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**U7 (SDRAM) Pin**
sdr_cke	-	-	+3.3V	37
sdr_ba1	A10	Output	+3.3V	21
sdr_ba0	J2	Output	+3.3V	20
sdr_cs_n	B10	Output	+3.3V	19
sdr_ras_n	C8	Output	+3.3V	18
sdr_cas_n	C6	Output	+3.3V	17
sdr_we_n	B12	Output	+3.3V	16
tri_be_n1	F3	Output	+3.3V	39
tri_be_n0	G2	Output	+3.3V	15

FLASH (U8)

The board has a 64 MBit Toshiba flash memory device. The target device is a TC58FVM6T2AFT65 in a TSOP package with the CFI flash command support.

The table notes the signal required for the flash memory. Signal directions are relative to the FPGA as far as direction and signaling standard. Table 2-5 shows the Flash signal name, corresponding FPGA pin, signal direction, type and board reference U8 Flash pin.

Table 2-5. Flash Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**U8(Flash) Pin**
tri_addr1	J15	Output	+3.3V	25
tri_addr2	D1	Output	+3.3V	24
tri_addr3	F2	Output	+3.3V	23
tri_addr4	F1	Output	+3.3V	22
tri_addr5	C2	Output	+3.3V	21
tri_addr6	B1	Output	+3.3V	20
tri_addr7	A2	Output	+3.3V	19

Table 2-5. Flash Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	U8(Flash) Pin
tri_addr8	B3	Output	+3.3V	18
tri_addr9	A3	Output	+3.3V	8
tri_addr10	D5	Output	+3.3V	7
tri_addr11	B4	Output	+3.3V	6
tri_addr12	A4	Output	+3.3V	5
tri_addr13	A12	Output	+3.3V	4
tri_addr14	A5	Output	+3.3V	3
tri_addr15	B5	Output	+3.3V	2
tri_addr16	T4	Output	+3.3V	1
tri_addr17	N9	Input	+3.3V	48
tri_addr18	A14	Input	+3.3V	17
tri_addr19	P8	Input	+3.3V	16
tri_addr20	T12	Input	+3.3V	9
tri_addr21	J1	Input	+3.3V	10
tri_addr22	T13	Input	+3.3V	13
fl_oe_n	D8	Input	+3.3V	28
fl_ce_n	G1	Input	+3.3V	26
fl_we_n	K1	Input	+3.3V	11
fl_reset_n	E2	Input	+3.3V	12
tri_data0	P16	Bidirectional	+3.3V	29
tri_data1	D16	Bidirectional	+3.3V	31
tri_data2	C16	Bidirectional	+3.3V	33
tri_data3	F15	Bidirectional	+3.3V	35
tri_data4	D15	Bidirectional	+3.3V	38
tri_data5	D14	Bidirectional	+3.3V	40
tri_data6	C14	Bidirectional	+3.3V	42
tri_data7	B13	Bidirectional	+3.3V	44
tri_data8	B6	Bidirectional	+3.3V	30

Table 2-5. Flash Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**U8(Flash) Pin**
tri_data9	A6	Bidirectional	+3.3V	32
tri_data10	B7	Bidirectional	+3.3V	34
tri_data11	A7	Bidirectional	+3.3V	36
tri_data12	D9	Bidirectional	+3.3V	39
tri_data13	C9	Bidirectional	+3.3V	41
tri_data14	B11	Bidirectional	+3.3V	43
tri_data15	A11	Bidirectional	+3.3V	45

Serial Configuration Memory Device - EPCS16 (U3)

U3 is a serial configuration device (EPCS16) for the Cyclone III FPGA on Embedded Development board. Serial configuration devices are flash memory devices with a serial interface that can store configuration data for a Cyclone III device and reload the data into the device upon power-up or re-configuration. On the Cyclone III Embedded Development board, JTAG Indirect Configuration (JIC) scheme is used to configure Serial Configuration Memory Device.

User Interface

LEDs (LED1, LED2, LED3, LED4, LED5, LED6)

The board includes three board specific LEDs and two user programmable LEDs. Table 2-6 lists LEDs and its description.

Table 2-6. LEDs Description		
Reference	**LED Name**	**Description**
LED1	CONF_DONE	Illuminates when the FPGA is configured successfully
LED2	RESET	Illuminates when the board is in reset condition
LED3	Power LED	Illuminates when there is 5V power available from available sources

Table 2-6. LEDs Description		
Reference	**LED Name**	**Description**
LED4	Charging LED	Illuminates when the LTC3555 charged
LED5, LED6	User LEDs	User Programmable LEDs

Table 2-7 lists LEDs Pinout.

Table 2-7. LEDs Pinout				
Signal Name	**FPGA Pin Name**	**Direction**	**Type**	**Description**
as_conf_done	H14	Output	+3.3V	Configuration LED
fpga_reset_n	E2	Output	+3.3V	Reset LED
-	-	Output	+5V	Power LED
user_led0	F16	Output	+3.3V	User Programmable LED
user_led1	P15	Output	+3.3V	User Programmable LED

Board Specific LEDs (LED1, LED2, LED3)

The power LED illuminates when the board's power is on and working. The configuration done LED illuminates when the FPGA is programmed. The reset LED illuminates when the board is in reset state.

User LEDs (LED5, LED6)

Status and debugging signals are driven to the user LEDs from FPGA designs loaded into the Cyclone III device. There is no board-specific function for the user LEDs.

USB 2.0 ULPI PHY (U11, U13)

The ISP 1504 is a serial bus (USB) high-speed host and peripheral transceiver that is fully compliant with the Universal Serial Bus specification.

The ISP1504 can transmit and receive USB data as high speed (480MBit/s), full speed (12MBit/s) and low speed (1.5MBit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral and OTG devices.

The ISP1504 can interface to the link with digital I/O voltages in the range of 1.65V to 3.6V. The Table 2-8 shows the USB-ULPI PHY chip signal name, corresponding FPGA pin, signal direction, type and board reference U11 (USB ULPI PHY chip) pin.

Table 2-8. USB 2.0 ULPI PHY (USB 2.0 Host) Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	U12 (ULPI PHY) Pin
u20_host_d0	K15	Bidirectional	+3.3V	1
u20_host_d1	L16	Bidirectional	+3.3V	32
u20_host_d2	N15	Bidirectional	+3.3V	31
u20_host_d3	N16	Bidirectional	+3.3V	28
u20_host_d4	N14	Bidirectional	+3.3V	26
u20_host_d5	L13	Bidirectional	+3.3V	25
u20_host_d6	L14	Bidirectional	+3.3V	24
u20_host_d7	L15	Bidirectional	+3.3V	23
u20_host_dir	E15	Input	+3.3V	19
u20_host_nxt	E16	Input	+3.3V	21
u20_host_stp	K16	Output	+3.3V	20
u20_host_reset_n	J16	Output	+3.3V	17
u20_host_clk_out	B16	Input	+3.3V	27
u20_host_cs_n	C3	output	+3.3V	29

The Table 2-9 shows the USB-ULPI PHY chip signal name, corresponding FPGA pin, signal direction, type and board reference U13 (USB-ULPI PHY chip) pin.

Table 2-9. USB 2.0 ULPI PHY (USB 2.0 OTG) Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	U13 (ULPI PHY) Pin
u20_otg_d0	P9	Bidirectional	+3.3V	1
u20_otg_d1	R11	Bidirectional	+3.3V	32

Table 2-9. USB 2.0 ULPI PHY (USB 2.0 OTG) Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	U13 (ULPI PHY) Pin
u20_otg_d2	T11	Bidirectional	+3.3V	31
u20_otg_d3	R10	Bidirectional	+3.3V	28
u20_otg_d4	R13	Bidirectional	+3.3V	26
u20_otg_d5	P11	Bidirectional	+3.3V	25
u20_otg_d6	N11	Bidirectional	+3.3V	24
u20_otg_d7	N12	Bidirectional	+3.3V	23
u20_otg_dir	T9	Input	+3.3V	19
u20_otg_nxt	R9	Input	+3.3V	21
u20_otg_stp	R12	Output	+3.3V	20
u20_otg_reset_n	R16	Output	+3.3V	17
u20_otg_clk_out	T10	Input	+3.3V	27
u20_otg_cs_n	R14	Output	+3.3V	29

LCD Connector (J5)

LCD Connector, J5 is 16-pin board-to-board interface connector which connects to J1 header of User Interface Board. The pins of header J5 can be used for debugging purpose. Table 2-10 shows the LCD Connector signal name, corresponding FPGA pin, signal direction, and board reference, J5 pin.

Table 2-10. LCD Connector Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	LCD Connector (J5) Pin No.
+3.3V	-	-	+3.3V	1
gnd	-	-	-	2
gpio_a0	T15	Output	+3.3V	3
gpio_a1	E10	Output	+3.3V	4
gpio_a2	D11	Output	+3.3V	5
gpio_a3	C15	Output	+3.3V	6

Table 2-10. LCD Connector Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**LCD Connector (J5) Pin No.**
gpio_a4	E11	Output	+3.3V	7
gpio_a5	H15	Bidirectional	+3.3V	8
gpio_a6	H16	Bidirectional	+3.3V	9
gpio_a7	F13	Bidirectional	+3.3V	10
gpio_a8	F14	Bidirectional	+3.3V	11
gpio_a9	G15	Bidirectional	+3.3V	12
gpio_a10	G16	Bidirectional	+3.3V	13
gpio_a11	J14	Bidirectional	+3.3V	14
gpio_a12	J13	Bidirectional	+3.3V	15
gnd	-	-	-	16

Push Button Switch Connector (J6)

Push Button Switch Connector, J6 is 16-pin board-to-board interface connector which connects to J2 header of User Interface Board. The pins of header (J6) can be used for debugging purpose. Table 2-11 shows the Push Button Switch signal name, corresponding FPGA pin, signal direction, and board reference, J6 pin.

Table 2-11. Push Button Switch Connector Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**Push Button Switch Connector (J6) Pin**
+3.3V	-	-	+3.3V	1
gnd	-	-	-	2
gp_in0	M1	Input	+3.3V	3
gp_in1	M15	Input	+3.3V	4
gp_in2	M16	Input	+3.3V	5
gp_in3	A9	Input	+3.3V	6

Table 2-11. Push Button Switch Connector Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	Push Button Switch Connector (J6) Pin
gp_in4	B9	Input	+3.3V	7
gp_in5	A8	Input	+3.3V	8
gp_in6	B8	Input	+3.3V	9
gp_in7	T8	Input	+3.3V	10
gp_in8	R8	Input	+3.3V	11
gpio_a13	M10	Input	+3.3V	12
gpio_a14	L8	Input	+3.3V	13
gpio_a15	T7	Input	+3.3V	14
pb_reset_n	E2	Input	+3.3V	15
GND	-	-	-	16

Control Function Header (J3)

Control Function Header, J3 is 6-pin board-to-board interface connector which connects to J4 header of User Interface Board. The pins of header (J3) can be used for debugging purpose. Table 2-12 shows the Control Function Header signal name, corresponding FPGA pin, signal direction, and board reference.

Table 2-12. Control Function Header Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	Control Function Header (J3) Pin
VCC_SW	-	-	vcc_sw	1
en_ps	-	-	-	2
ntc	-	-	-	3
en_osc	-	-	-	4
vcc_bat	-	-	vcc_bat	5
gnd	-	-	gnd	6

JTAG Header (J1)

JTAG Header, J1 is used to configure FPGA Device on the Cyclone III Embedded Development board. Table 2-13 shows the JTAG Header signal name, corresponding FPGA pin, signal direction, and JTAG Header board reference, J1 pin.

Table 2-13. JTAG Header Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	J1 (JTAG Header) Pin
jtag_tck	H3	Input	+2.5V	1
GND	-	-	-	2
jtag_tdo	J4	Output	+2.5V	3
VCCA	-	-	+2.5V	4
jtag_tms	J5	Input	+2.5V	5
VCCA	-	-	+2.5V	6
NC	-	-	-	7
NC	-	-	-	8
jtag_tdi	H4	Input	+2.5V	9
GND	-	-	-	10

SD Card Socket (CON3)

The board includes one micro SD card socket and it features:

- Card push-in push-out ejection
- Card capturing mechanism prevents card from flying out at ejection.
- User-friendly mis-insertion prevention
- Robust structure protects against excess stress from above.
- Card is firmly locked in use for card fall-out prevention, but released when excessive pulling force is applied.
- Reliable two-point connection with double contacts
- Enhanced grounding for noise (EMI) reduction
- Normally closed card detection switch contributes to saving energy.
- Satisfies RoHS requirements.

Table 2-14 shows the SD Card signal name, corresponding FPGA pin, signal direction, type and board reference SD Card, CON3 pin.

Table 2-14. SD Card Connector Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	CON3 (SD Card) Pin
sdc_d0	A15	Bidirectional	+3.3V	7
sdc_d1	T14	Bidirectional	+3.3V	8
sdc_d2	C11	Bidirectional	+3.3V	1
sdc_d3	D12	Bidirectional	+3.3V	2
sdc_cmd	A13	Bidirectional	+3.3V	3
sdc_clk	R4	Output	+3.3V	5
sdc_preset_n	M2	Input	+3.3V	13

Expansion Interface

General Purpose I/O Header (J4)

There is a 40-pin header connector (J4), which can be used for general purpose I/O or debugging. Table 2-15 shows the General Purpose I/O header signal name, corresponding FPGA pin, signal direction, type and board reference J4 GPIO pin.

Table 2-15. General Purpose I/O Header Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	J4 (GPIO) Pin
gpio0	E6	Bidirectional	+3.3V	1
gpio1	E7	Bidirectional	+3.3V	2
gpio2	E8	Bidirectional	+3.3V	3
gpio3	E9	Bidirectional	+3.3V	4
gpio4	F8	Bidirectional	+3.3V	5
gpio5	F9	Bidirectional	+3.3V	6
gpio6	G5	Bidirectional	+3.3V	7
gpio7	K2	Bidirectional	+3.3V	8
gpio8	K5	Bidirectional	+3.3V	9

Table 2-15. General Purpose I/O Header Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	J4 (GPIO) Pin
gpio9	L1	Bidirectional	+3.3V	10
VCC_SW	-	-	+5V	11
GND	-	-	GND	12
gpio10	L2	Bidirectional	+3.3V	13
gpio11	L3	Bidirectional	+3.3V	14
gpio12	L4	Bidirectional	+3.3V	15
gpio13	N1	Bidirectional	+3.3V	16
gpio14	N2	Bidirectional	+3.3V	17
gpio15	P1	Bidirectional	+3.3V	18
gpio16	P2	Bidirectional	+3.3V	19
gpio17	R1	Bidirectional	+3.3V	20
gpio18	T2	Bidirectional	+3.3V	21
gpio19	T3	Bidirectional	+3.3V	22
gpio20	R3	Bidirectional	+3.3V	23
gpio21	P3	Bidirectional	+3.3V	24
gpio22	N3	Bidirectional	+3.3V	25
gpio23	T5	Bidirectional	+3.3V	26
gpio24	R5	Bidirectional	+3.3V	27
gpio25	N5	Bidirectional	+3.3V	28
VCC 3_3_2	-	-	+3.3V	29
GND	-	-	GND	30
gpio26	T6	Bidirectional	+3.3V	31
gpio27	R6	Bidirectional	+3.3V	32
gpio28	P6	Bidirectional	+3.3V	33
gpio29	N6	Bidirectional	+3.3V	34
gpio30	M6	Bidirectional	+3.3V	35
gpio31	R7	Bidirectional	+3.3V	36
gpio32	M7	Bidirectional	+3.3V	37

Table 2-15. General Purpose I/O Header Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**J4 (GPIO) Pin**
gpio33	L7	Bidirectional	+3.3V	38
gpio34	N8	Bidirectional	+3.3V	39
gpio35	M8	Bidirectional	+3.3V	40

Clocks

Crystal Oscillator (Y1)

The Cyclone III Embedded Development board has various clock oscillator to support number of IP blocks requiring different frequencies. A single 48-MHz (Y1) clock input can be used as a system clock, dedicated PLLs are used to distribute the Flash, SDRAM and other devices where as 19.2-MHz. Table 2-16 shows clocking circuitry pinout..

Table 2-16. Clocking Circuitry Pinout			
Signal Name	**FPGA Pin**	**Direction**	**Type**
osc_clk	E1	Input	+2.5V, 48-MHz

Power Supply

Power Supply Regulator (U4, U5, U6)

The power supply block distributes clean power from the 5 V input supply to the Cyclone III device through on-board high efficiency USB Manager and triple DC/DC regulators. To provide various voltage options, the board uses Linear Technologies' (LTC 3555) power manager (U4) and Texas Instruments' (TPS 73025, TPS 73018) low-dropout linear regulator (U5, U6). Board regulators are used to generate the voltages listed in Table 2-17 .

Table 2-17. Power Supply Regulators				
Output Voltage (V)	**MAX Current (A)**	**Regulator Board Reference**	**Regulator Part #**	**Where Used**
+3.3V	400 ma	U4	LTC3555	Cyclone III VCCIO, Configuration PROM, LCD Supply
+3.3V	400 ma	U4	LTC3555	Flash, SDRAM, two USB2.0 ULPI PHY, SD Card, GPIO, Push Button Keypad

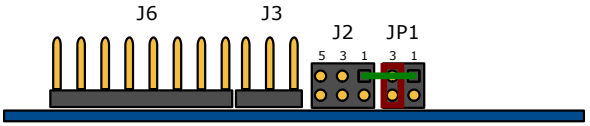
Table 2-17. Power Supply Regulators				
Output Voltage (V)	**MAX Current (A)**	**Regulator Board Reference**	**Regulator Part #**	**Where Used**
+1.2V	1A	U4	LTC3555	Cyclone III core supply
+2.5V	200 ma	U5	TPS73025	Cyclone III Analog supply
+1.8V	200 ma	U6	TPS73018	SN74AVC2T45DCUT

The board can be powered up by the following three options. Jumper selection is provided in the board for supply mode selection.

USB BUS Power Mode. Board can be powered up through USB Connector via USB Cable connected at host side. 5V, 500mA input supply from the host side will drive the entire board. If there is a current consumption budget for more than 500mA then the board has one additional dummy USB connector to get the total supply current 1A. The section below explains the procedure to power up the board from USB bus.

Connect the shorting link between JP1.3 and JP1.4 on the power input select jumper. The board is configured to be powered from the external supply. Now connect a shorting jumper (or a simple shorting wire) between JP1.1 and J2.1. See Figure 2-3. This will essentially connect VBUS from the USB Device on the CoreCommander board to the external supply input and power the board. This will also wire the VBUS of the USB device to the power distribution switch of the USB embedded host interface on the CoreCommander board.

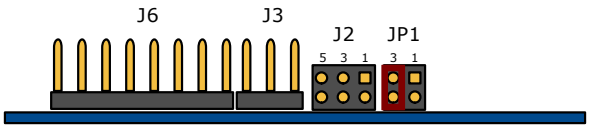
Figure 2-3. Power up the board from USB Device's VBUS



External Input Power Mode. Board can also be powered up through external regulated 5V, 500mA~1A. The section below explains the procedure to power up the board from USB bus.

Place the power select jumper on JP1.3-JP1.4 to configure the board to be powered from the external power supply. Supply a +5V, 500mA (min.) to J2.1 (+5V) and J2.2 (GND) from a bench top supply or by any other suitable means. This would power up the board from external supply.

Figure 2-4. Power up the Board from External Supply



Battery Input Power Mode. Board can be powered up through battery supply. Recommended Battery Voltage rating is +3.3V, 1A to operate the entire board. There is an extra facility to externally charge the System Battery via USB Bus Power. The section below explains the procedure to power up the board from battery.

If the USB device is not used in applications, the USB device won't get enumerated on the PC and hence it will be power-limited. To avoid voltage droop on the VBUS, it is recommended to use fully charged battery for such applications so that the board can get sufficient current from the battery and at the same time the VBUS from the USB embedded host remains within the acceptable limits.

Power Switch (SW1)

Power switch is used to power up the board from the selected power source configuration described below. See "Power Supply Select Jumper (JP1)" on page 24.

Power Supply Select Jumper (JP1)

Power supply select jumper selects power source from many available sources like USB Power, External Supply or Battery Supply. Table 2-18 shows jumper configuration to select particular source to power up the Cyclone III Embedded Development board. Power Supply Input Jumper (J2)

Table 2-18. Power Supply Select Jumper Settings	
Jumper Settings	**Power Source**
Short JP1.1 & JP1.2	USB-ULPI connector
Short JP1.3 & JP1.4	External 5V supply

Power Supply (External/Battery) Input Jumper

Power Supply Input jumper is used to feed power other than USB power supply to the Cyclone III Embedded Development board. Table shows configuration to feed power through external or battery supply.

Table 2-19. Power Supply Input Jumper Settings	
Jumpers	**Function**
J2.1 & J2.2	Input external supply VCC 5V to J2.1 and GND to J2.2.
J2.3 & J2.4	Input battery supply VCC 3.3V to J2.3 and GND to J2.4
Short J2.5 & J2.6	Battery's1 Thermister (NTC) input to temperature controlled battery charging

Note:
(1) Standard Li-Ion/Polymer battery can be used with this board. The battery supply feature is not tested yet in the current release.

3. User Interface Board Components

This chapter provides operational and connectivity detail for the User Interface board's major components and interfaces.

The board schematic can be found at:
*<CoreCommander Installation Path>***board_design_files\schematics**

Figure 3-1. shows the top view of the User Interface board.

Figure 3-1. Top View of the User Interface Board

Table 3-1 describes the components and lists their corresponding board references.

Table 3-1. User Interface Board Component and Interfaces

Type	Board Reference	Name	Description	Page
User Interfaces				
Display	CON1	LCD Display	1.7” 160x128 pixel TFT LCD with GRAM	27
I/O	J1	LCD Interface Header	LCD Interface Board-to-Board Header	28
Input	SW1-SW7	Push Button Switch	User programmable and reset push button switches	28
Input	J2	Push Button Switch Interface Header	User programmable and reset push button Board-to-Board Header	29
Input	J4	Control function Header	Provides support for control functions	18
Input	J3	GPIO Header	Provides GPIO interface	29
Power Supply				
Power Supply	U1	LCD Backlight Supply	3.3 V to 5V converter to supply power to LCD back light	30
Power Supply	J5	Power Supply Header	Used for battery supply header	

User Interface

LCD Display (CON1)

The board provides a 1.7” TFT-LCD with 160x128 pixel resolution. It is mounted on the 22-pin FPC connector CON1. Table 3-2 shows the LCD signal name, corresponding FPGA pin, signal direction, type and board reference CON1 LCD pin.

Table 3-2. LCD Display Pinout

Signal Name	FPGA Pin	Direction (FPGA)	Type	CON1 (LCD) Pin
LCD_CS_N	A14	Output	+3.3V	7
LCD_RS	D11	Output	+3.3V	9
LCD_WR_N	C15	Output	+3.3V	10
LCD_RD_N	E11	Output	+3.3V	11
LCD_D0	J13	Bidirectional	+3.3V	19
LCD_D1	J14	Bidirectional	+3.3V	18
LCD_D2	G16	Bidirectional	+3.3V	17
LCD_D3	G15	Bidirectional	+3.3V	16
LCD_D4	F14	Bidirectional	+3.3V	15
LCD_D5	F13	Bidirectional	+3.3V	14
LCD_D6	H16	Bidirectional	+3.3V	13
LCD_D7	H15	Bidirectional	+3.3V	12
LCD_RESET_N	E10	Output	+3.3V	8

LCD Interface Header (J1)

LCD interface header (J1) connects LCD Display of User Interface board to the Cyclone III Embedded Development board through the LCD Connector (J5) of the host board. As this header directly connects to LCD Connector J5 of the base board, for pin description refer "LCD Connector Pinout" on page 16.

Push Button Switches (SW1-SW7)

SW1-SW7 are momentary-contact push-button switches and are used to provide stimulus to designs on the Cyclone III Embedded Development board. Each switch is connected to the general-purpose I/O pin with the pull-up resistor. The device pin will see logic '0' when each switch is pressed. Figure 3-1. displays the push button switches.

Table 3-3 shows the Push Button Switches signal name, corresponding FPGA pin, signal direction, type and board reference Push Button Switches connector pin.

Table 3-3. Push Button Switches (SW1-SW7) Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**SW#**
KEY_UP	M1	Input	+3.3V	SW1
KEY_DOWN	M15	Input	+3.3V	SW2
KEY_RIGHT	M16	Input	+3.3V	SW3
KEY_LEFT	A9	Input	+3.3V	SW4
KEY_ENTER	B9	Input	+3.3V	SW5
KEY_BACK	A8	Input	+3.3V	SW6
PB_RESET_N	E2	Input	+3.3V	SW7

Push Button Switch Interface Header (J2)

Push Button Switch Interface header (J2) connects Push Button Switches of the User Interface board to the Cyclone III Embedded Development board through the Push Button Switch Connector (J6) of the host board. As this header directly connects to J6 of the base board for pin description refer "Push Button Switch Connector Pinout" on page 17.

GPIO Header (J3)

The 8 pin GPIO header (J3) provides GPIO interface which can be used for general purpose I/O or debugging. Table 3-4 lists the GPIO pinouts.

Table 3-4. General Purpose I/O Header Pinout				
Signal Name	**FPGA Pin**	**Direction (FPGA)**	**Type**	**J3 (GPIO) Pin**
vcc_3_3	-	-	+3.3V	1
gp_in6	B8	Bidirectional	+3.3V	2
gp_in7	T8	Bidirectional	+3.3V	3
gp_in8	R8	Bidirectional	+3.3V	4
gpio_13	M10	Bidirectional	+3.3V	5
gpio_14	L8	Bidirectional	+3.3V	6
gpio_15	T7	Bidirectional	+3.3V	7
GND	-	-	GND	8

Power Supply

LCD Backlight Supply (U1)

REG71055, Texas Instruments Buck -Boost Charge Pump (U1) is used to generate 5V for 1.7” LCD back light. The 3.3V input to U1 is provided from LCD Interface Header (J1).