USB 2.0 On-The-Go (ULPI) Snap On Board

Reference Manual

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The IP was not developed for or intended for use in any specific customer application. The firmware/software of the device may have to be adapted to the specific intended modalities of use or even replaced by other firmware/software in order to ensure flawless function in the respective areas of application.

Performance data may depend on the operating environment, the area of application, the configuration, and method of control, as well as on other conditions of use; these may deviate from the technical specifications, the Design Guide specifications, or other product documentation. The actual performance characteristics can be determined only by measurements subsequent to integration.

The reference designs were tested in a reference environment for compliance with the legal requirements applicable to the reference environment.

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About this Manual

Introduction

This manual provides component details of the USB 2.0 On-The-Go (ULPI) Snap On board.

Table below shows the revision history of board's reference manual.

Version	Date	Description
1.4	November 2008	Updated document with new Snap On Board photograph and added the details of P-Channel switch.
1.3	May 2008	Updated features section
1.2	March 2008	Changed pictures of the board.
1.1	December 2007	Changed pin configuration of Santa Cruz Headers J1 and J2
1.0	October 2007	First Publication of the Reference Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
- Bookmarks serve as an additional table of contents.
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Typographic Conventions

This reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: **Board Components, Featured Device.**
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: **Figure 2-1. USB 2.0 (SCUSB20UL) Snap On Board Components, Table 2-1. USB 2.0 (SCUSB20UL) Snap On Board Components & Interfaces.**
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
	The hand points to special information that requires special attention
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

Contents

1. Introduction

The USB 2.0 On-The-Go (ULPI) Snap On board is designed to provide connectivity between USB 2.0 Host / OTG controller and USB 2.0 Device / OTG IP core. The Snap On board provides a fast, versatile, and easy-to-use communication path for data exchange between the device and host.

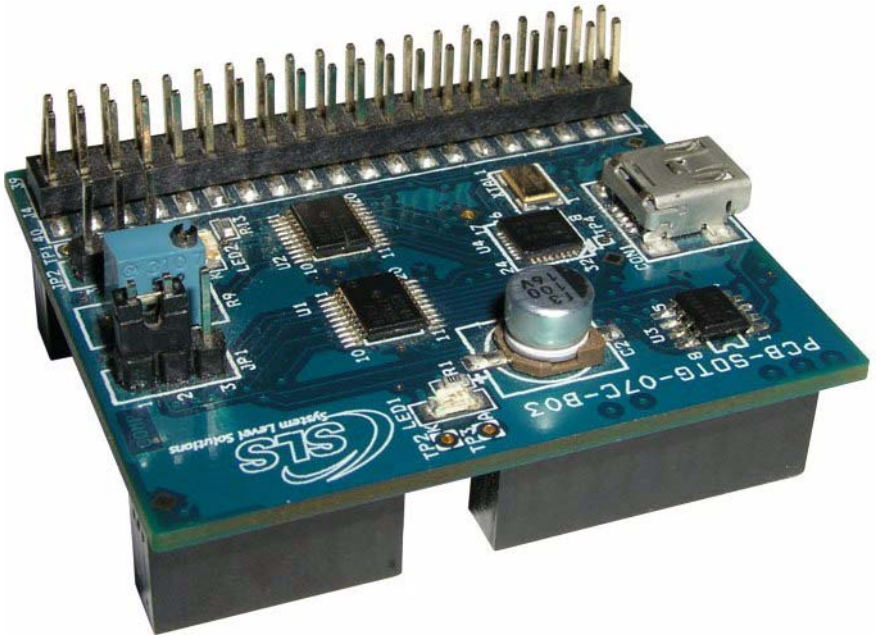
Features

The USB 2.0 On-The-Go (ULPI) Snap On board is featured with:

- ULPI PHY Chip - NXP ISP1504
- Supports Low Speed (1.5 Mbps), Full Speed (12Mbps) and High Speed (480Mbps) USB operation
- Provides 8-bit, 60MHz bi-directional databus interface
- Fully compatible with:
  - USB Specification Rev. 2.0
  - On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2
  - UTMI+Low Pin Interface (ULPI) Specification Rev. 1.1
- USB Mini AB-type connector
- Dedicated crystal for providing clock to the PHY chip
- A current limited External V_{BUS} Power Switch with thermal shutdown
- One power LED and one user LED
- Standard Santa Cruz interface and GPIO interface support

Figure 1-1. shows the USB 2.0 On-The-Go (ULPI) Snap On board angle view.

Figure 1-1. USB 2.0 - On-The-Go (ULPI) Snap On Board Angle View



The board works seamlessly with SLS USB 2.0 IP cores. For more information, visit http://www.slscorp.com/pages/ipusb2sls.php

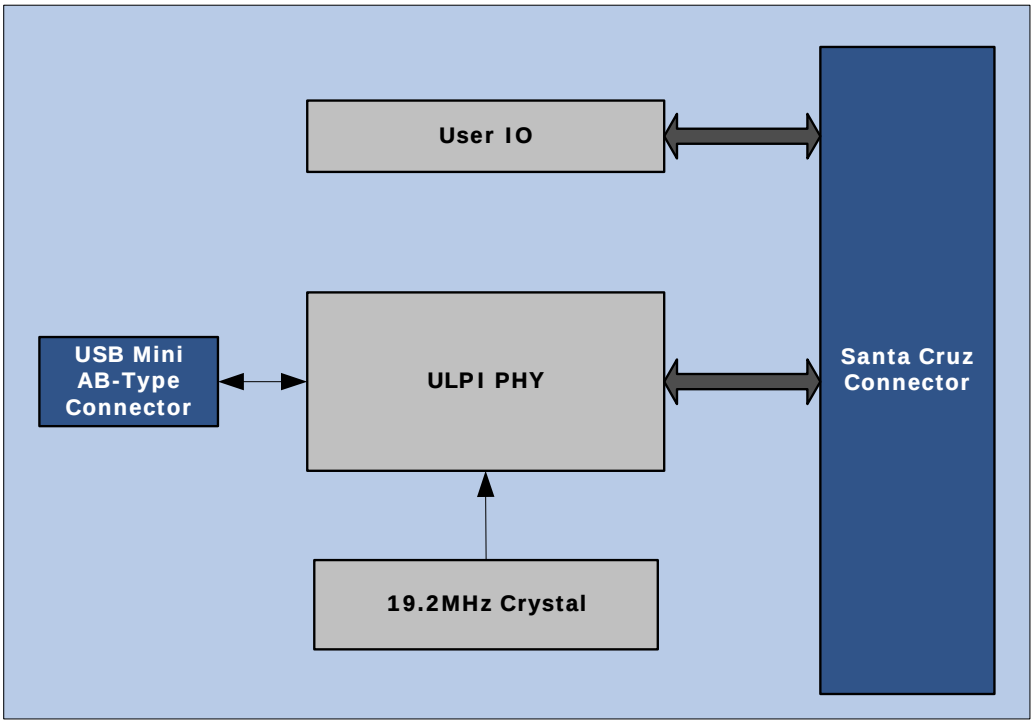
Block Diagram

USB 2.0 On-The-Go (ULPI) Snap On board includes following components:

- USB Mini AB-type Connector
- PHY Chip (Physical Layer Transceiver),
- SMD Crystal of 19.2 MHz for PHY chip
- Power LED (LED1)
- User LED (LED 2)
- Level Shifter (U1, U2)
- V_{BUS} Power Switch (U3)
- Header (M), J4
- Headers (F), J1,J2,J3

The three headers J1, J2, J3 are female headers on USB2.0 snap on board which snaps on santacruz connectors. Figure 1-2. below shows functional diagram of the board.

Figure 1-2. USB 2.0 - On-The-Go (ULPI) Snap On Board Functional Diagram



Next chapter explains overview of all the board components.

2. Board Components

This section contains brief overview of the important components on the USB 2.0 On-The-Go (ULPI) Snap On board. Figure 2-1. below shows the components on the Snap On board.

Figure 2-1. USB 2.0 - On-The-Go (ULPI) Snap On Board - Components

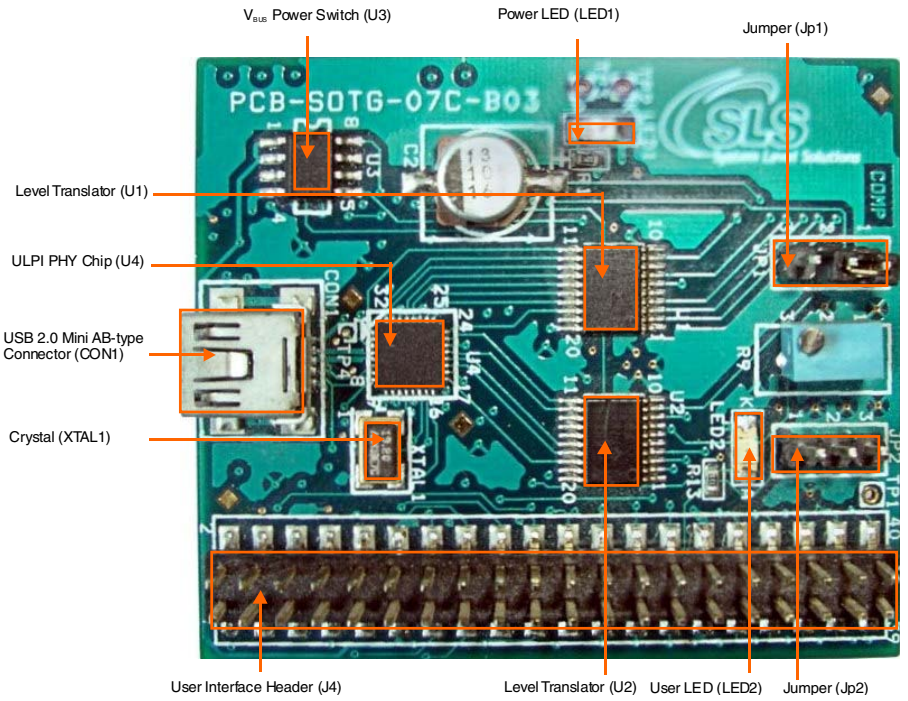


Table 2-1 lists summary of the USB 2.0 - On-The-Go Snap On Board' components.

Table 2-1. USB 2.0 - On-The-Go (ULPI) Snap On Board Components & Interfaces

Board Reference	Name	Description	Page
Featured Device			
U4	ISP1504	ULPI (USB2.0 High Speed Universal Serial Bus On the Go Transceiver Interface) -- PHY Chip	6
User Interfaces			
CON1	USB 2.0 Connector	One USB 2.0 OTG Mini Connector (AB-Type).	8
Level Shifter & Switches			
U1, U2	Level Shifter	Used to protect USB OTG Phy chip.	9
U3	V_{BUS} Power Switch	A current limited External V_{BUS} Power Switch with thermal shut-down	9
Expansion Connectors			
J1, J2, J3	Expansion Prototype Connector	These are the three female connectors used for mounting daughter card (In this case its USB2.0 Snap On Board) on the Development Kit having standard Santa Cruz short expansion male interface.	10
General Purpose User I/O Connectors			
J4	User Interface Header	All the unused pins of SantaCruz connector are taken out for the user to use it for any other applications like debug or use it as standard I/O.	12
LEDs			
LED1	USB Power LED	Power LED, indicates 3.3V supply present on the board.	13
LED2	User LED	User can use this LED to indicate any I/O Signals or debugging	13
Clocks			
XTAL1	Crystal	Generates 19.2MHz clock as an input for PHY Chip.	13

Table 2-1. USB 2.0 - On-The-Go (ULPI) Snap On Board Components & Interfaces			
Board Reference	Name	Description	Page
Jumpers			
JP1	Jumper	Used for selection of Decoupling capacitor for USB OTG Host configuration or Device configuration	13
JP2	Jumper	Used for selection of internal charge pump or external charge pump circuit	13

Featured Device

PHY Chip (U4)

The ISP1504 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver that is fully compliant with Universal Serial Bus Specification Rev. 2.0, On-The-Go supplement to the USB 2.0 specification Rev. 1.2 and UTMI+ Low pin interface (ULPI) specification rev. 1.1.

The ISP1504 can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to USB host, peripheral and OTG devices.

Features

- Fully compatible with:
  - Universal Serial Bus Specification Rev. 2.0
  - On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2
  - UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1
- Interfaces to host, peripheral and OTG device cores; optimized for portable devices or system ASICs with built-in USB OTG device core
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
  - Integrated 5 V charge pump; also supports external charge pump or 5 V VBUS switch
- Flexible system integration and very low current consumption, optimized for portable devices

- Full industrial grade operating temperature range from -40 º C to +85 º C
- 4 kV ElectroStatic Discharge (ESD) protection at pins DP, DM, ID, VBUS and GND
- Available in a small HVQFN32 (5 mm ´ 5 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

The Figure 2-1. displays the PHY Chip on the board.

The PHY chip is an ideal choice for physical layer transceiver of USB 2.0 applications. Table 2-2 displays PHY Chip signals with its type & functionality.

Table 2-2. PHY Chip Signals

Pin #	Pin Name	Type	Pin Function
1	DATA0	I/O	Pin 0 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
2,22,30	VCCIO1/2/3	I/O	I/O supply rail
3	RREF	AI/O	Resistor reference
4	DM	AI/O	Data minus (D–) pin of the USB cable
5	DP	AI/O	Data plus (D+) pin of the USB cable
6	FAULT	I	Input pin for the external VBUS digital over current or fault detector signal plain input; 5 V tolerant
7	ID	I	Identification (ID) pin of the mini-USB cable plain input; TTL level
8	CPGND	Ground	Charge pump ground
9	C_B	AI/O	Flying capacitor pin connection for the charge pump
10	C_A	AI/O	Flying capacitor pin connection for the charge pump
11	VCC	Power	Input supply voltage or battery source
12	PSW_N	OD	Active LOW external VBUS power switch or external charge pump enable open-drain; 5 V tolerant
13	VBUS	AI/O	VBUS pin of the USB cable 5 V tolerant
14	REG3V3	Power	3.3 V regulator output
15	XTAL1	AI	Crystal oscillator or clock input
16	XTAL2	AO	Crystal oscillator output

Table 2-2. PHY Chip Signals

Pin #	Pin Name	Type	Pin Function
17	RESET_N	I	Active LOW, asynchronous reset input plain input
18	REG1V8	P	1.8 V regulator output
19	DIR	O	ULPI direction signal slew-rate controlled output (1 ns)
20	STP	I	ULPI stop signal plain input; programmable pull up
21	NXT	O	ULPI next signal slew-rate controlled output (1 ns)
23	DATA7	I/O	Pin 7 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
24	DATA6	I/O	Pin 6 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
25	DATA5	I/O	Pin 5 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
26	DATA4	I/O	Pin 4 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
27	CLK	O	60 MHz clock output when a crystal is attached; requires 60 MHz clock input when the crystal is not attached slew-rate controlled output (1 ns); plain input
28	DATA3	I/O	Pin 3 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
29	CS_N	I	Active LOW chip select plain input
31	DATA2	I/O	Pin 2 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
32	DATA1	I/O	Pin 1 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down

User Interface

This section describes user interface which includes USB 2.0 Mini AB type connector.

USB Mini AB-Type Connector (CON1)

USB2.0 Snap On board incorporates USB mini AB-type connector connected with PHY chip. Figure 2-1. displays the USB mini AB-type connector.

Pin mapping of connector with PHY chip is shown in Table 2-3

Table 2-3. USB Mini AB-Type Connector to PHY Chip Connection

Connector Pin #	Signal	PHY Chip Pin #
1	VBUS	--
2	D-	4
3	D+	5
4	GND	--

Level Shifter & P-Channel Switch

This section describes the level shifter and P-Channel switch used on the USB 2.0 On-The-Go Snap On Board.

Level Shifter (U1, U2)

As USB OTG Phy chip I/O Compatibility is +3.3V, to make I/O Communication compatible with Santa Cruz I/O which has +5V logic level, level shifters are used. Level shifters down the voltage level of Santa Cruz I/O and protect USB OTG Phy chip. Figure 2-1. displays Level Shifters U1 and U2.

V_{BUS} Power Switch (U3)

The board has MAX890L smart, low-voltage, P-channel, MOSFETpower switch intended for high-side load-switching applications. This switch operates with inputs from +2.7V to +5.5V, making it ideal for both +3V and +5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperatures.

The MAX890L's maximum current limit is 1.2A. The current limit through the switch is programmed with a resistor from SET to ground. The quiescent supply current is a low 10µA. When the switch is off, the supply current decreases to 0.1µA.

The MAX890L is available in an 8-pin SO package. Figure 2-1. displays V_{BUS} Power Switch (U3).

Expansion Connectors

This section describes the expansion connectors on the USB 2.0 On-The-Go Snap On Board.

Expansion Prototype Connectors (J1,J2,J3)

Headers J1, J2, and J3 collectively form the standard-footprint called Santa Cruz short expansion headers (female), which are 14 pins, 40pins and 20pins respectively. These are mechanically stable connections that can be used for mounting daughter card (USB 2.0 On-The-Go Snap On Board) on to any Development Kit having standard Santa Cruz short expansion male interface.

The expansion prototype connector interface includes

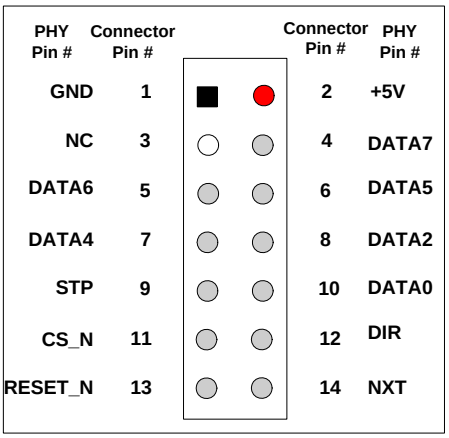
- 74 pins for prototyping (Out of which 43 I/O pins connect to user I/O pins and 3 dedicated clock pins on the Cyclone device)
- An Active LOW Power On Reset signal
- Five regulated 3.3V power-supply pins (1A total max load)
- One regulated 5V power-supply pin. (1A total max load)
- Numerous ground connections

The output logic level on the expansion prototype connector pins is 5 volts.

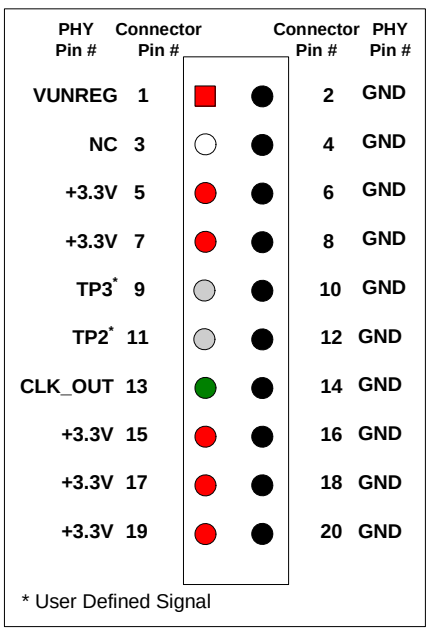
Figure 2-2. shows the pin description of the connectors J1, J2 & J3.

Figure 2-2. Pin Description of Expansion Prototype Connector-J1,J2,J3

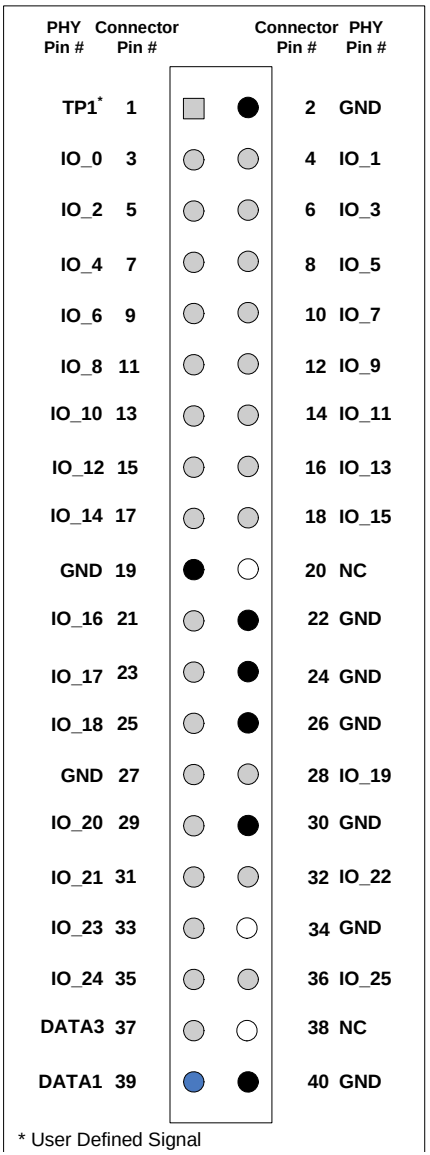
J1



J2



J3



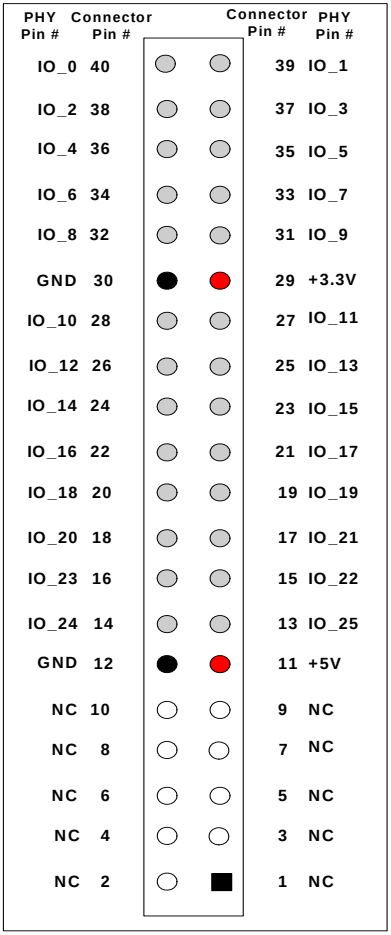
General Purpose User I/O Connectors

This section describes the general connector on the USB 2.0 On-The-Go Snap On Board.

User Interface Header (J4)

There is one User Interface Header J4 (20x2) on USB 2.0 On-The-Go Snap On Board as displayed in Figure 2-1. The unused pins of the Santa Cruz header are taken on this headers so that one can use these pins while debugging the core.

Figure 2-3. User Interface Header (J4)



LEDs

This section describes the LEDs on USB 2.0 On-The-Go Snap On Board.

Power LED (LED1)

The USB 2.0 On-The-Go Snap On Board has 1power LED (LED1) as shown in
Figure 2-1. When LED1 is “ON”, indicates 3.3Vsupply present on the board.

User LED (LED2)

The USB 2.0 On-The-Go Snap On Board has 1 general purpose user LED (LED2) as shown in Figure 2-1. User can use this LED2 as an indication of any required output.

Clocks

This section describes the clock used on the USB 2.0 On-The-Go Snap On Board.

Crystal (XTAL1)

The USB 2.0 On-The-Go Snap On Board includes 19.2 MHz Crystal which is used to provide reference clock for PHY chip. Crystal clock input is on pin no 15 and Crystal clock output is on pin 16 of PHY Chip. Figure 2-1. displays Crystal.

Jumpers

This section describes the jumpers used on the USB 2.0 On-The-Go Snap On Board.

Jumper (JP1)

Used for selection of Decoupling capacitor for USB OTG Host configuration or Device configuration. Figure 2-1. displays Jumper JP1 on the board.

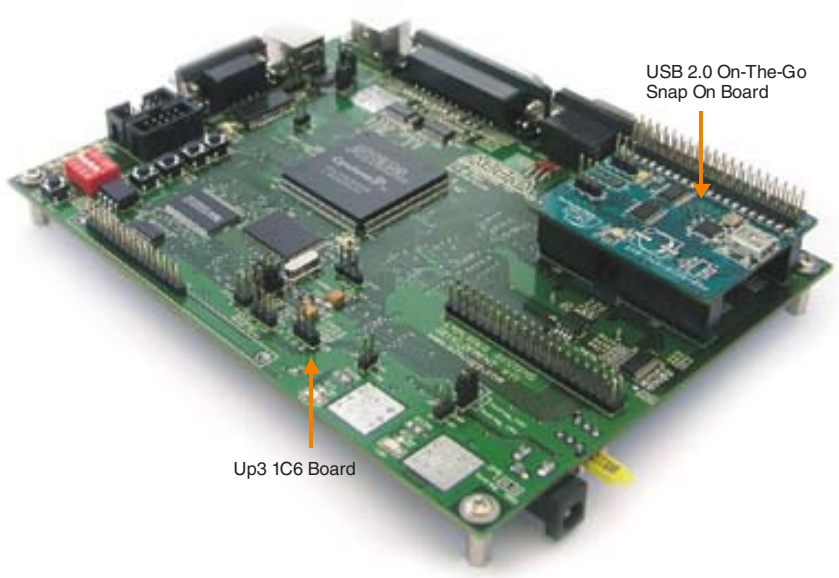
Jumper (JP2)

Used for selection of internal charge pump or external charge pump circuit. Figure 2-1. displays Jumper JP2 on the board.

3. Signal Mapping

The three (F) headers (J1,J2,J3) on USB 2.0 Snap On board snaps on to three (M) Santa Cruz headers (J2,J4,J3) of UP3 Education kit as shown in Figure 3-1.

Figure 3-1. Connection of USB 2.0 - On-The-Go (ULPI) Snap On Board with UP3 Education kit



Mapping PHY Pins with Core I/O

Table 3-1 shows the PHY Signals with Core I/O.

Table 3-1. Mapping PHY Signals with Core I/o

PHY Chip Signal	Header Pin #	Core Signals
CLK_OUT	J3.13	usb_clk
RESET	J1.13	Reset

Table 3-1. Mapping PHY Signals with Core I/o		
PHY Chip Signal	Header Pin #	Core Signals
DATA0	J1.10	Data[0]
DATA1	J2.39	Data[1]
DATA2	J1.8	Data[2]
DATA3	J2.37	Data[3]
DATA4	J1.7	Data[4]
DATA5	J1.6	Data[5]
DATA6	J1.5	Data[6]
DATA7	J1.4	Data[7]
STP	J1.9	Stp
NXT	J1.14	Nxt
DIR	J1.12	Dir
cs_n	J1.11	Cs_n

Unused Pin Mapping

Header (M) Pin Mapping to Header (F) Connector

Table 3-2 below shows the pin mapping to santa cruz connector.

Table 3-2. Header Pin Mapping to Santa Cruz Connector		
Header Pin (F) #	Header Pin (M) #	I/O
J2.3	J4.40	gpio_0
J2.4	J4.39	gpio_1
J2.5	J4.38	gpio_2
J2.6	J4.37	gpio_3
J2.7	J4.36	gpio_4
J2.8	J4.35	gpio_5
J2.9	J4.34	gpio_6
J2.10	J4.33	gpio_7
J2.11	J4.32	gpio_8
J2.12	J4.31	gpio_9

Table 3-2. Header Pin Mapping to Santa Cruz Connector

Header Pin (F) #	Header Pin (M) #	I/O
J2.13	J4.28	gpio_10
J2.14	J4.27	gpio_11
J2.15	J4.26	gpio_12
J2.16	J4.25	gpio_13
J2.17	J4.24	gpio_14
J2.18	J4.23	gpio_15
J2.21	J4.22	gpio_16
J2.23	J4.21	gpio_17
J2.25	J4.20	gpio_18
J2.28	J4.19	gpio_19
J2.29	J4.18	gpio_20
J2.31	J4.17	gpio_21
J2.32	J4.16	gpio_22
J2.33	J4.15	gpio_23
J2.35	J4.14	gpio_24
J2.36	J4.13	gpio_25